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Introduction

Step up/down converters exhibit a number of interesting properties that make them attractive for different applications. The key feature of these converters is the ability to operate with a wide range of input voltages, which can be lower or higher with respect to the output voltage. Low voltage battery powered devices such as PDAs make use of the flexibility of these converters to fully exploit Li-Ion batteries [1]. Automotive applications need a power conversion stage that is able to supply different loads with a regulated voltage while withstanding severe line transients due to battery voltage fluctuations [2]. As an example [3], typical requirements for an automotive stereo system power supply are an input voltage varying in the range $10V - 40V$ and a regulated output voltage of $15V$. Stand-alone PV systems [4], [5] also benefit from the use of step up/down converters. Indeed, a stand alone PV system almost invariably requires the use of battery for energy storage to supply the load when the power from the PV panel is either absent or too low. Hence, the ability to follow the charge profile of the battery is mandatory. On the other end, the use of Maximum Power Point Tracking (MPPT) algorithms require the input voltage of the PV converter to vary, in order to match the characteristic of the panel.
The simplest step up/down power converters are the buck-boost and the flyback [3], [38], [39]. Low components count, well understood dynamics properties and easy implementation using commercially available ICs are the main advantages of these converters. Due to the presence of a transformer in the power stage, flyback converters can be easily turned into an isolated power sup-

ply. Hence, they are widely used to realize power factor correctors (PFC) [6]-[7]. The possibility to add multiple secondary windings to the transformer allows to realize multiple outputs and auxiliary power converters in more complicated supplies [8]. Buck boost converters are used in applications where the input voltage needs to be inverted, and in LED lighting applications [9]. However, both converters also suffer from some drawbacks. The most obvious limitation is that both the input and the output capacitors have to sustain a high frequency pulsating current. In both converters, the input voltage source is periodically disconnected, as in a buck converter. This requires the addition of bulky input capacitors (usually electrolytics) and possibly the use of an input inductance to reduce the harmonic content injected towards the source. The output load is also periodically disconnected from the power supply, as in a boost converter. Big output capacitors and/or additional filters are required to match load specifications and to reduce noise. Among other step up/down power supply topologies, the SEPIC (Single Ended Primary Inductance Converter) and the Cuk converter (so named after its inventor) are gaining widespread acceptance in the literature and in the market. Both converters are characterized by the presence of an input inductance, which reduces the RMS content of the input capacitor current. For a given application, the use of SEPIC or Cuk converters instead of a flyback converter may allow the reduction of the size and capacitance of the input capacitors. Hence, although both SEPIC and Cuk converters make use of an additional inductor and of an additional capacitor if compared with flyback or buck-boost, the reduced size of input and output filters may allow to obtain comparable power densities [3]. Also, with respect to the flyback converter, stress on the power components is reduced. For low and medium power applications, a complete AC/DC power supply with PFC can be realized using the SEPIC and the Cuk converter [10], [11], [12], [19], [20]. Multiple outputs power supplies can also be realized [8]. The Cuk converter has the additional benefit of an output inductance which is directly connected to the load, as in a buck converter. Applications of the Cuk

converter to drive LED loads are numerous, both in DC/DC and in AC/DC applications [13]. As the output inductance is directly supplying the load, the need for an output capacitance is minimized in LED lighting applications. This imply an extremely fast dynamic responses to load transients, thereby allowing the use of high frequency dimming techniques to control the LED power output [15]-[16]. PV systems based on the SEPIC [4] take advantage of the presence of the input inductance to reduce the PV panel current ripple while minimizing the size of input filters. Both in LED lighting and PV applications the reduction of the size and value of input and output capacitance is a crucial point. This is because the PV panel is a power source with an estimated lifetime of more than 20 years, while LED estimated lifetime goes up to 100.000 hours, compared with a life cycle of 2.000 hours of conventional light sources [14]. The expected lifetime of a complete LED lighting system, or of a PV system, is then conditioned by the power conversion apparatus. From this point of view, the replacement of electrolytic capacitor with more resistant ceramic ones is of great importance, as the former often constitute the weakest elements of the power stage [16], [17], [21].

The four switch non inverting buck boost topology is also gaining popularity in step up/down applications [1], [18]. However, it requires at least two control switches and two diodes. One of the control switch needs an high side driver (as in conventional buck boost). Four control switches and two high side drivers are needed in its synchronous rectifier realization.

One of the major drawbacks of SEPIC and Cuk converters lies in their complicated fourth-order dynamic behavior [26], [49], [50]. The design of such converters guaranteeing stable dynamic behavior in presence of a wide input voltage range may be a challenging task, especially if Peak Current Control (PCC) is applied [41], [46]-[48]. PCC [38], [39] is widely used because of its beneficial effects in terms of the rejection of line disturbances, and because it tends to simplify the dynamic of the controlled converter. Due to a feedforward effect of the input voltage in the current loop, peak current controlled converters exhibits a fast re-

sponse with respect to line transients events. This makes the use of this control strategy attractive for a great number of applications, *e.g.* automotive applications. Another important feature is that PCC implements a cycle-by-cycle limitation of the current peak in the control switch. Hence, potential overload and short circuit conditions are detected by the current controller without the use of additional external circuitry. Paralleling converters for current sharing purposes is also easily accomplished using PCC. PCC is also suitable to realize PFCs up to several hundreds Watt [10]. Accurate modelling of the current loop is needed to properly design stable current controlled converters [27]-[37]. Some simplifying assumptions found in literature [38], [46] may lead to unpredicted instability phenomena if applied to current controlled fourth-order converters [42]-[44], [47], [48], [52].

In this dissertation, both large signal and small signal averaged models of SEPIC and Cuk converters are analyzed. A novel refined small signal model of the peak current controller is derived to remove some approximations usually found in literature when dealing with fourth-order step up/down converters. A numerical investigation of PCC-SEPIC stability boundaries with respect to line voltage variations and to the value of power stage passive components is presented. Such investigation is done using a complete averaged small signal model of the converter. Based on the results, possible design guidelines to obtain both a stable PCC-SEPIC and a desired dynamic behavior with respect to line transients are given. A reduced-order small model of peak current controlled SEPIC and Cuk converter is also proposed. The use of such model allows to derive analytical stability boundaries for both converters, and to further highlight the joint impact of power stage passive components and of the current controller characteristics on stability. Impact of losses on stability predictions is also discussed. Comparisons with complete full order models are given for both SEPIC and Cuk. Simulations and experimental verifications prove the validity of the results.

The dissertation is organized as follows. In chapter 1, a review of SEPIC and Cuk topologies is given, together with comparisons

with flyback and buck boost and a brief overview of PCC technique. In Chapters 2 and 3, the small signal model of PCC SEPIC is derived. A new and refined model for the current controller is discussed and a new reduced-order model is presented. Stability boundaries for PCC SEPIC are derived. The small signal model and the analytical stability boundaries for PCC-Cuk are derived in Chapter 4. In Chapter 5, experimental validations that supports the proposed results are given.

Chapter 1

A review of step up/down converters and of Peak Current Control

1.1 Step up/down converters

Schematics of flyback, buck boost, SEPIC and Cuk converters are shown in Fig. 1.1 - Fig. 1.4. Parasitics elements are neglected. The blue and red arrows highlight continuous and discontinuous current paths respectively. Notice that the input current is considered continuous. This is true in the hypothesis that a sufficient amount of inductance is present on the line. As this assumption is a worst case condition for the sizing of input capacitors, it is usually assumed to be valid when designing a converter without precise knowledge of the source and line impedance.
In the hypothesis of converters running in Continuous Conduction Mode (CCM), the steady state voltage conversion ratio M can be expressed in terms of the control switch Q nominal duty cycle $D = \frac{t_{on}}{T_s}$, where T_s is the switching period and t_{on} is the fraction of the switching period during which the control switch is in its on state. Imposing Volt-second balance on the inductors, and neglecting losses, ideal voltage conversion ratio can be easily derived. Results for the flyback, buck-boost, Cuk and SEPIC

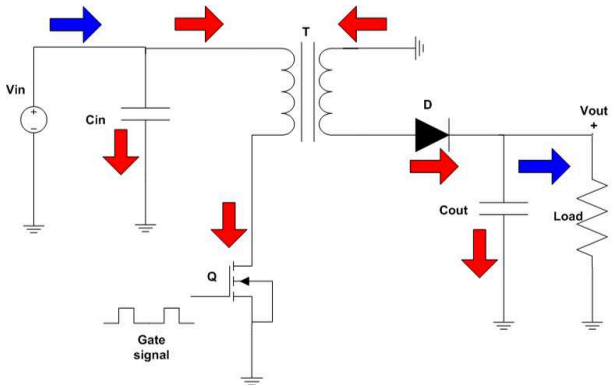

Figure 1.1 Schematic of flyback converter

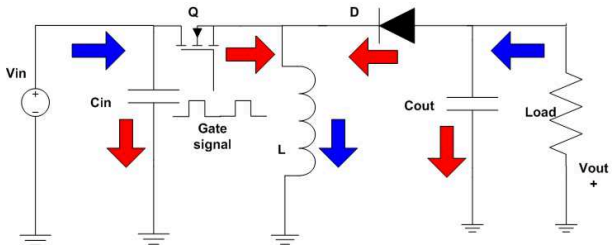

Figure 1.2 Schematic of buck boost converter

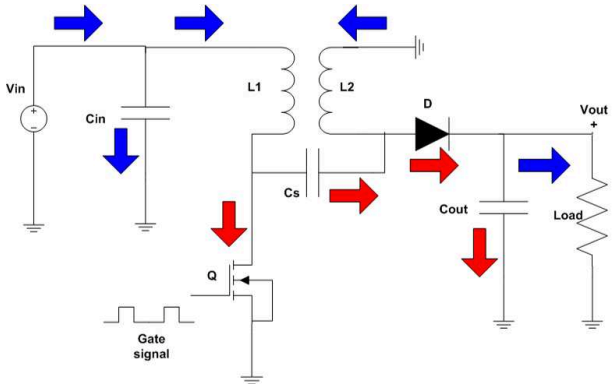

Figure 1.3 Schematic of SEPIC converter

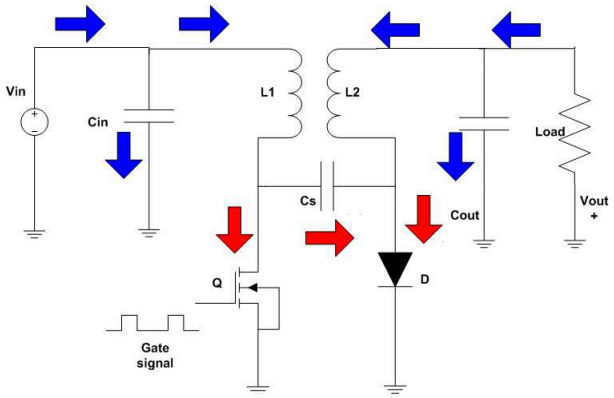

Figure 1.4 Schematic of Cuk converter

converters are summarized in table 1.1. The minus sign in buck boost and Cuk voltage conversion ratio imply that the polarity of the output voltage is inverted with respect to the input voltage. n is the secondary to primary turns ratio of the flyback transformer. For lossless converters, input and output power are equal.

Table 1.1 Ideal voltage conversion ratio M

Flyback converter	$n\frac{D}{1-D}$
Buck-boost converter	$-\frac{D}{1-D}$
Cuk converter	$-\frac{D}{1-D}$
SEPIC converter	$\frac{D}{1-D}$

It follows that:

$$\frac{I_{in}}{I_{out}} = \frac{V_{out}}{V_{in}} = M.$$

The voltage V_{off} across power switches during the off state is equal to $V_{in} + V_{out}$ for buck boost, SEPIC and Cuk converters. For the flyback converter, the voltage across the control switch is $V_{off,Q} = V_{in} + V_{out}\frac{1}{n}$, while the voltage across the diode is $V_{off,D} = nV_{in} + V_{out}$. Notice that resonances due to parasitics reactive elements may cause the instantaneous voltage across the switches to rise well above the nominal V_{off} values, thus increasing the voltage stress. This is a relevant issue in the flyback converter, where resonances among the leakage inductances of the power transformer and the stray capacitances of silicon devices and of the transformer may cause severe voltage peaks on the switches during commutations. In SEPIC and Cuk converters, the instantaneous voltage stress is reduced due to the beneficial effects of the coupling capacitance C_s. The average voltage V_s across capacitance C_s is

$$V_s = V_{in},$$

for the SEPIC converter, and

$$V_s = V_{in} + V_{out},$$

for the Cuk converter. For all converters, the average control switch current is equal to the average input current I_{in}, and the average diode current is equal to I_{out}. In SEPIC and Cuk converters, I_{in} and I_{out} are also equal to the average currents flowing in the input and output inductors respectively. It is useful to define the quantity I_{on} as the sum of the input and output average currents: $I_{on} = I_{in} + I_{out}$.

1.2 Peak current control

Peak Current Control (PCC) is widely used in DC/DC converters operating at fixed switching frequency f_s. With this type of control, the peak of the control switch current is regulated via an analog comparator during each switching period. For basic buck, boost and buck-boost converters, the control switch current i_s is identical to the current that flows into the inductor during its charging phase. Hence, the control switch current has a finite positive slope that depends on the inductance value and on the voltage applied to the inductor during the on-time. In SEPIC and Cuk converters, the control switch current is equal to the sum of the inductors currents during t_{on}. PCC has the benefit of very simple implementation: first, an external clock turns on the control switch at the beginning of each switching period. The controller then turns off the switch when its current reaches a reference value. Such reference value is almost always derived from some other variable of the converter that needs to be regulated to a predetermined value (*e.g.* the input current or the output voltage). Fig. 1.5 shows a typical application of PCC to a SEPIC converter, where the output voltage is regulated. As shown in Fig. 1.5, the switch current is translated into a voltage, V_{sns}, using a transducer having gain A_s. The simplest way to implement this scheme is using a sensing resistor. V_{sns} is then compared to the signal $v_c - v_{ramp}$. The control signal v_c is related to the error signal between the actual output voltage and a predetermined set point. Hence, PCC can be modelled as a double control loop scheme,

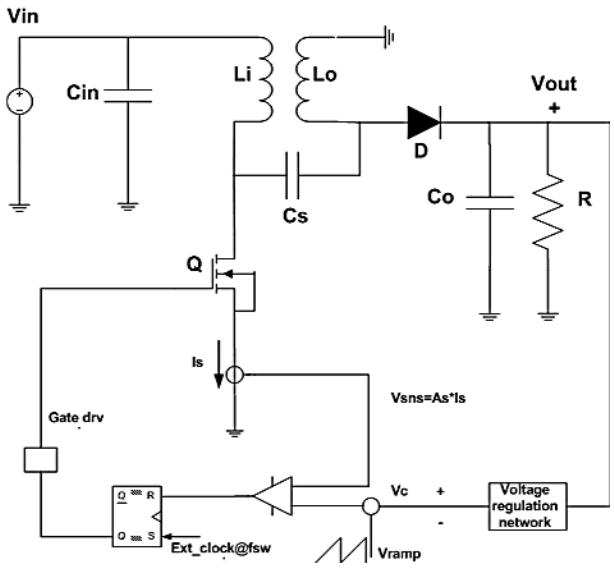

Figure 1.5 Peak Current Controlled SEPIC

where an inner loop, the *current loop*, and an outer loop, the *voltage loop*, can be identified. As widely reported in literature, the control loop is inherently unstable for duty ratios $D > 0.5$. To stabilize the current loop, the ramp signal v_{ramp} is subtracted to v_c [27]-[38]. This procedure is usually referred to as "ramp compensation". To explain the unstable behavior of the current loop, signals v_c and V_{sns} are represented in Fig. 1.6, for a converter operating in Continuous Conduction Mode (CCM) without ramp compensation. The trapezoidal waveform represents V_{sns}. The slope M_1 is proportional to the inductor current slope during $t_{on} = DT_s$, via the current sensor gain A_s. The inductor current during the off time of the control switch is also represented, scaled by the same gain A_s. In steady-state operation, the volt-second balance on the inductor imply that $M_1 D = M_2(1 - D)$ is satisfied. Fig. 1.7 show what happens to the inductor current waveform when a perturbation is present. As the control switch is turned on at the beginning of each switching period by the external clock signal, perturbations in the inductor current determine oscillations on the value of the duty cycle D. In [38], a simple geometrical

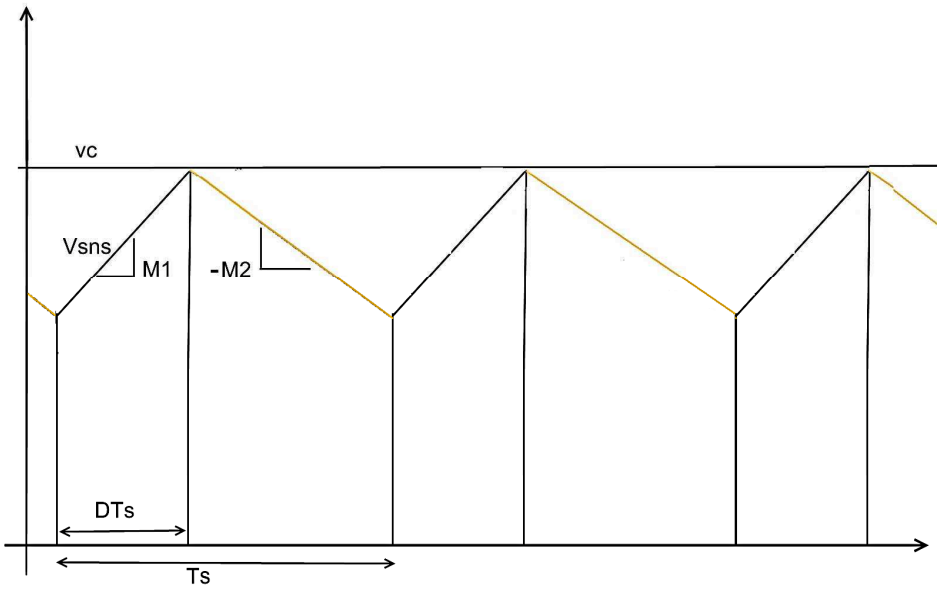

Figure 1.6 Control voltage v_c and sensed voltage V_{sns} in PCC without ramp compensation

procedure is used to demonstrate that the oscillations in the duty cycle value tend to decrease if $D < 0.5$, while $D > 0.5$ will cause oscillations to increase indefinitely. This phenomenon is usually referred to as "subharmonic oscillations", as the frequency of duty cycle oscillations is equal to $\frac{f_s}{2}$. The same waveforms with the addition of ramp compensation are shown in Fig. 1.8. The slope $-M_a$ determines the amplitude of the voltage ramp. The ramp compensation technique allows to increase the maximum value of D below which stability of the current loop is ensured. Indeed, if

$$\frac{M_a}{M_2} > 0.5, \tag{1.1}$$

the current loop is stable for any value of D [38]. The increase of M_a above the minimum value (1.1) allows to reduce the settling time of the duty cycle oscillations. As noise is always present in switched converters, the use of a compensating ramp is recommended also when the converter always operates with $D < 0.5$,

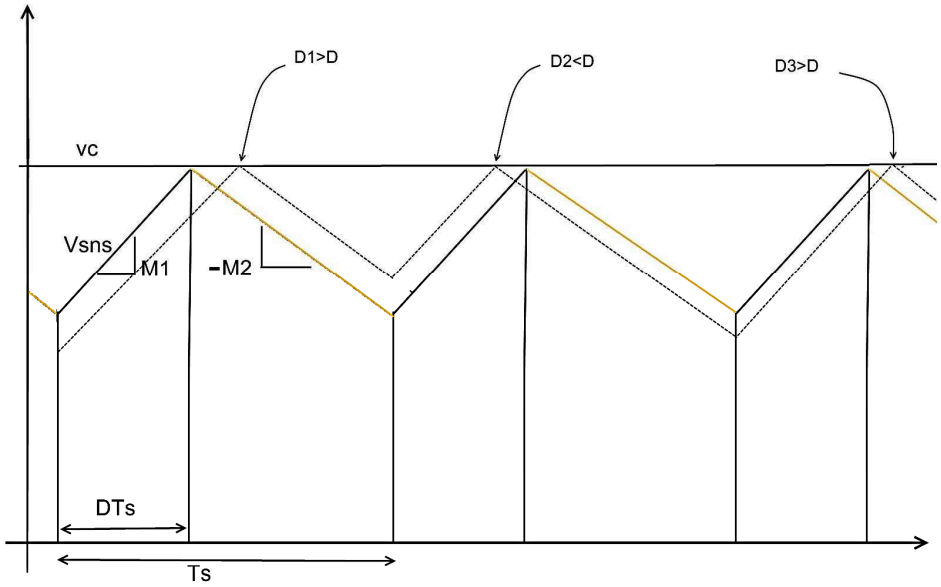

Figure 1.7 Subharmonic oscillations in PCC without ramp compensation

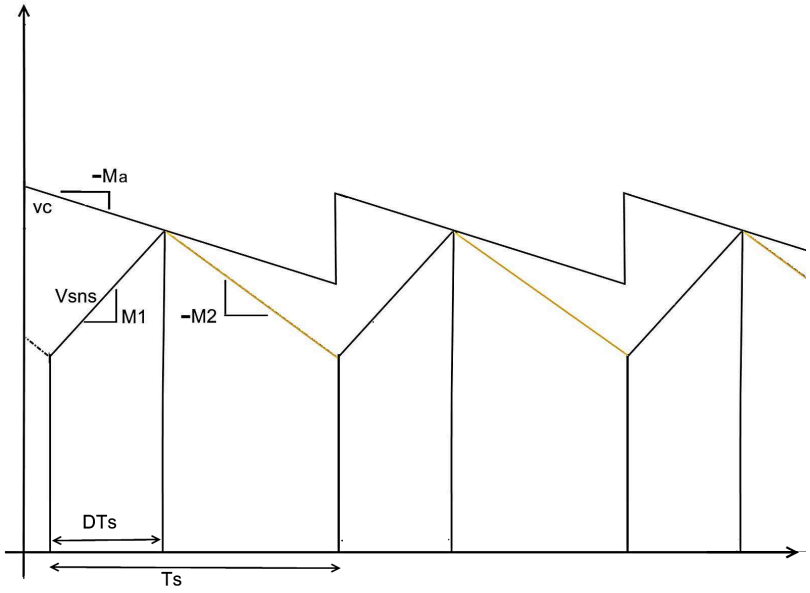

Figure 1.8 Control voltage v_c and sensed voltage V_{sns} in PCC with ramp compensation. Voltage V_{ramp} is subtracted from v_c

to damp the duty cycle oscillations around its nominal operating value.

1.2.1 Current loop small signal models

A major benefit of PCC is that its application tends to simplify the dynamics of the controlled converter. The reason for this is that the peak of the inductor current is forced to follow the control signal v_c. Under the simplifying hypothesys that the inductor current ripple can be neglected, this means that the average value of the inductor current equates the control signal v_c, scaled by the gain A_s. Hence, at low frequencies (well below the swicthing frequency), the inductor of a current controlled converter can be represented as a voltage-controlled current source. Considering a second order converter such as the buck or the boost converter, application of peak current control makes the control-to-output gain appear as a first order transfer function, where only the pole due to the output capacitor is present instead of a complex conjugate pole pair due to the interaction between the inductor and the output capacitor. However, as the inductor current actually differs from its peak value, the second pole due to the inductor is still present and acting at frequencies between $\frac{f_s}{6}$ and $\frac{2f_s}{3}$ [28]. The presence of two real poles instead of a complex conjugate pole pair helps the design of the outer voltage loop compensation. Although in [28] and [38] small signal linear models of current programmed converters are given, such models do not allow to predict the subharmonic oscillations at $\frac{f_s}{2}$. Due to the presence of an analog comparator and of a Set-Reset Flip Flop (see Fig. 1.5) in the current loop, peak current control is essentially a sample and hold system, where the value of the switch current i_s is sampled with frequency f_s. As a result, modelling the current loop with the usual averaging techniques leads to inaccuracies in the predicted frequency response around the Nyquist frequency [36]. Extensions of the averaged model to include sampling effects in the usual continuous time model of PCC are given in [29]-[31]. The sampling effect is accounted for by inserting a delay block

in the current loop. The discrepancies in the models proposed in literature are essentially due to where this delay block is inserted in the current loop. An analysis of the discrepancies among these models is given in [27] and [32]. Although the models resulting from [29]-[31] may predict quite different behaviors in the high frequency range, results below the Nyquist frequency are almost identical. Accurate sampled data models of the current loop may be obtained, *e.g.* [36]. However the results, while quite useful in a CAD based environement, may not give easy-to-handle design equations readily available for the designer. It should also be noted that the accuracy of averaged models of the power converter itself is reduced above the Nyquist frequency. In this dissertation, as the object of the investigation are phenomena located well below the Nyquist frequency, the sampling effect is neglected, and the model proposed in [38] is adopted. According to [38], the small signal relationship between the duty cycle $\hat{d}$ and the control signal $\hat{v}_c$ is:

$$\hat{d} = \frac{1}{M_a T_s}(\hat{v_c} - A_s \hat{i}_L - \frac{D^2 T_s}{2}\hat{m}_1 - \frac{(1-D)^2 T_s}{2}\hat{m}_2). \qquad (1.2)$$

Variable $\hat{i}_L$ may represent the inductor current in converters with a single inductor, *e.g* the buck converter, of the linear combination of inductors currents. Quantities $\hat{m}_1$ and $\hat{m}_2$ are related to the small signal variations of the voltage across the inductor (or across the inductors) during the charging and discharging phases respectively. As $\hat{m}_1$ and $\hat{m}_2$ are linear combinations of input and output voltages and of voltages across capacitors of the converters, they can be regarded as the combination of input variables and state variables of the LTI model of the converter. $\hat{i}_L$ is also a linear combination of state variables. The block diagram shown in Fig. 1.9 represents the small signal model of a generic DC/DC converter with peak current control. $\hat{x}$ is the state vector of the LTI model of the converter. The inner current loop and the outer voltage loop can be easily identified. Note that the output voltage is included in the state vector $\hat{x}$. This is striclty true only if the parasitic ESR of the output capacitor is neglected, so that the

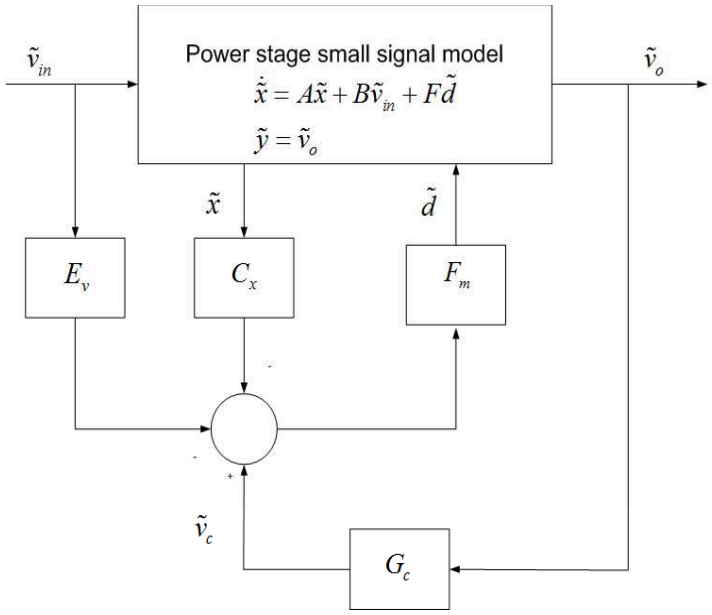

Figure 1.9 Small signal model of peak current controlled DC/DC converter

output capacitor voltage v_{Co} is coincident with the output voltage v_o. However, losses of power components are usually neglected when deriving expressions for $\hat{m}_1$ and $\hat{m}_2$ [27]-[36]. The quantity F_m is usually referred to as the current loop gain, and it is independent from the topology of the controlled converter. C_x and E_v are vectors of coefficients that relates the input voltage and the state vector to the duty cycle.

Chapter 2

Small Signal Model of PCC SEPIC

Stability analysis and linear control design of PWM dc-dc switching regulators are commonly based on small-signal low-frequency averaged and linearized ac models of power converters and controllers. State-Space Averaging (SSA), PWM Switch and circuit averaging techniques [22], [23], [38], [39] are mostly used to derive such models. Deep discussions on the stability analysis of current-mode controllers is found in power electronics literature [27]-[36]. Stability issues regarding SEPIC are among the most puzzling ones in the context of dc-dc switching regulators. It is well known [24], [25], [49], [50] that the open loop SEPIC small-signal duty-to-output voltage gain G_{vd} exhibits two resonant peaks, due to the presence of two couples of complex conjugates poles. Moreover, G_{vd} is characterized by a couple of complex zeros that can be located either in the Right Half Plane (RHP) or in the Left Half Plane (LHP), and by the real RHP zero typical of boost-derived dc-dc converters. Studies regarding specifically the PCC-SEPIC stability have been presented [41]-[46], highlighting that the PCC-SEPIC is more prone to instability when it operates in boost mode with high voltage conversion ratio. In particular, [41] shows that for a given SEPIC design there may exists a threshold for the input voltage V_{in} below which instability occurs and that stability

is recovered if the ratio between the output inductance L_o and the input inductance L_i is increased. In the following, the open loop SEPIC small signal model properties are reviewed, and a refined small signal model of the current controller is presented. In chapter 3, a novel reduced-order lossless model that allows to derive analytical stability conditions for PCC-SEPIC is proposed. The impact of losses on stability is also discussed. A complete small signal model that includes the aforementioned refined control law is derived. The impact of the power stage reactive components on PCC-SEPIC dynamics is highlighted through the use of a numerical procedure. The role of the coupling capacitor in ensuring both stability and good dynamic performances in presence of line transients events is investigated. The application of a damping technique [51] based on an additional resistance-capacitance branch is shown.

2.1 SEPIC open loop small signal model

Fig. 2.1 shows the schematic of a PCC-SEPIC. Assuming that the converter is operating in Continuous Conduction Mode (CCM), the small-signal linearized ac model of the switching cell can be obtained by means of circuit averaging, SSA technique or PWM-switch model [22], [23], [38], [39] applied to the two-port model based on variables v_1, v_2, i_1, i_2:

$$v_1 = \begin{cases} R_{ds} i_L & t \in [0, DT_s[\\ v_s + v_o + V_d + R_d i_L & t \in [DT_s, T_s[\end{cases} \tag{2.1}$$

$$v_2 = \begin{cases} v_s + v_o - R_{ds} i_L & t \in [0, DT_s[\\ -V_d - R_d i_L & t \in [DT_s, T_s[\end{cases} \tag{2.2}$$

$$i_1 = \begin{cases} i_L & t \in [0, DT_s[\\ 0 & t \in [DT_s, T_s[\end{cases} \tag{2.3}$$

$$i_2 = \begin{cases} 0 & t \in [0, DT_s[\\ i_L & t \in [DT_s, T_s[\end{cases} \tag{2.4}$$

Let us denote with $\langle x \rangle$ the local average of the generic switching

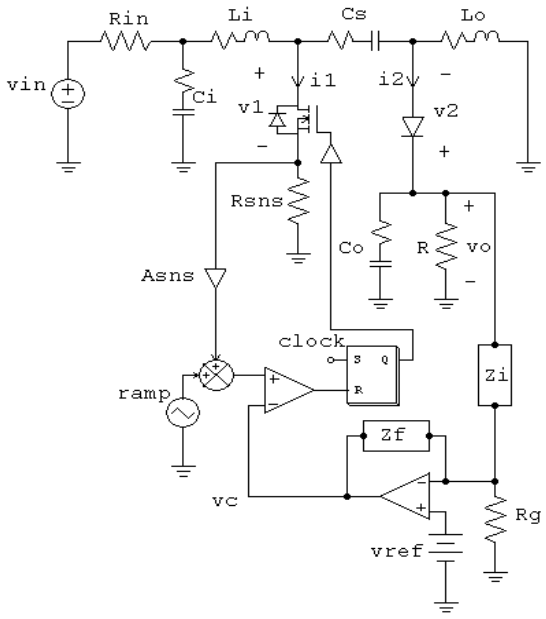

Figure 2.1 PCC SEPIC schematic

cell variable $x(t)$ over the switching period T_s [39]:

$$\langle x \rangle = \frac{1}{T_s} \int_{t-T_s}^{t} x(\tau) d\tau. \tag{2.5}$$

By definition, $\langle x \rangle$ is still a function of time. The integral operator acts as a low-pass filter on the variable $x(t)$, removing the harmonic content at the switching frequency. If the converter output voltage is well regulated and if i_L and v_s can be considered constant over the switching period T_s [38], the application of (2.5) to (2.1)-(2.4) yields the average large signal model of the switching cell:

$$\langle i_1 \rangle = d i_L \tag{2.6}$$

$$\langle i_2 \rangle = d' i_L \tag{2.7}$$

$$\langle v_1 \rangle = d R_{ds} i_L + d'(v_s + v_o + V_d + R_d i_L) \tag{2.8}$$

$$\langle v_2 \rangle = d[v_s + v_o - R_{ds} i_L] - d'(V_d + R_d i_L) \tag{2.9}$$

where $d' = 1 - d$. Equations (2.6)-(2.9) can be used to derive $\langle v_1 \rangle$ and $\langle i_2 \rangle$ as a function of $\langle v_2 \rangle$ and $\langle i_1 \rangle$:

$$\langle i_2 \rangle = \frac{d'}{d} \langle i_1 \rangle \tag{2.10}$$

$$\langle v_1 \rangle = \frac{d'}{d} \langle v_2 \rangle + R_{eq}(d) \langle i_1 \rangle + \frac{d'}{d} V_d \tag{2.11}$$

where

$$R_{eq}(d) = \frac{R_{ds}}{d} + \frac{d'}{d^2} R_d \tag{2.12}$$

Assuming steady-state operation, $\langle x \rangle$ is a constant value: $\langle x \rangle = X$. The DC values of the switching cell variables in steady state are given by:

$$I_2 = \frac{D'}{D} I_1 \tag{2.13}$$

$$V_1 = \frac{D'}{D} V_2 + R_{eq}(D) I_1 + \frac{D'}{D} V_d \tag{2.14}$$

Note that I_1 and I_2 are equal to the DC input current and to the DC output current of the converter respectively, *i.e.*:

$$I_1 = I_{in}, I_2 = I_{out}. \tag{2.15}$$

It follows:

$$I_L = I_{in} + I_{out} = I_1 + I_2 = I_{on}. \tag{2.16}$$

Perturbing and linearizing (2.10) and (2.11) the small signal linear model of the switching cell is then obtained:

$$\hat{i}_2 = \frac{D'}{D}\hat{i}_1 - \hat{d}I_{eq}, \tag{2.17}$$

$$\hat{v}_1 = \frac{D'}{D}\hat{v}_2 + R_{eq}(D)\hat{i}_1 - \hat{d}V_e, \tag{2.18}$$

where $\hat{x}$ represents the ac component of the variable x and:

$$I_{eq} = \frac{I_{on}}{D},$$
$$V_e = \frac{2DV_1 - V_2(1-2D) - V_d(1-2D) + (R_d - R_{ds})I_1}{D^2}.$$

Equations (2.17)-(2.18), together with the equations of the linear time-invariant part of the circuit, provide the open loop ac small signal model of the SEPIC shown in Fig. 2.2.
Note that (2.17) and (2.18) are the result of a first-order approximation of (2.10) and (2.11) [38]. Hence, to obtain the lossless (ideal) small signal model of the switching cell it is necessary to neglect parasitics elements in (2.10) and (2.11) and then to apply the small signal approximation. The removal of parasitics elements in (2.17) and (2.18) will cause incorrect results. The ideal ac small signal model is given by:

$$\hat{i}_2 = \frac{D'}{D}\hat{i}_1 - \hat{d}I_{eq}, \tag{2.19}$$

$$\hat{v}_1 = \frac{D'}{D}\hat{v}_2 - \hat{d}V_{eq}, \tag{2.20}$$

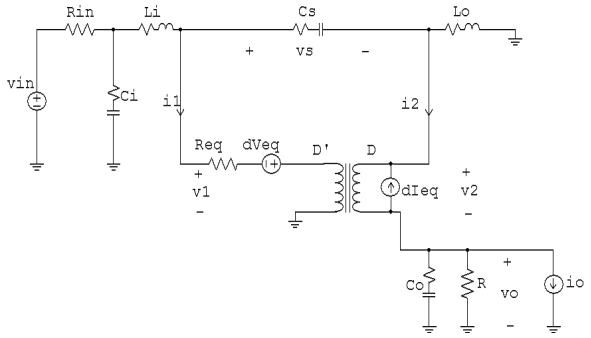

Figure 2.2 Open loop SEPIC small signal model

where:

$$V_{eq} = \frac{V_{off}}{D}.$$

In the following, to simplify notation, the generic large signal averaged variable $\langle x \rangle$ will be denoted as x.

The ac variations of the duty cycle $\hat{d}$ are considered an input of the model. The independent current generator $\hat{i_o}$ shown in Fig. 2.2 is used to determine the output impedance of the circuit, and to evaluate the impact of fluctuations in the output current due to external causes on the output variables of the model. In the frequency domain, relationships among the input variables $\hat{d}(s)$, $\hat{v}_{in}(s)$, $\hat{i}_o(s)$ and the output variables $\hat{i}_L(s)$, $\hat{v}_s(s)$, $\hat{v}_o(s)$ are expressed in compact form by means of the small-signal transfer functions:

$$\hat{i}_L(s) = G_{id}(s)\hat{d}(s) + G_{ig}(s)\hat{v}_{in}(s) + G_{io}(s)\hat{i}_o(s), \tag{2.21}$$

$$\hat{v}_s(s) = G_{sd}(s)\hat{d}(s) + G_{sg}(s)\hat{v}_{in}(s) + G_{so}(s)\hat{i}_o(s), \tag{2.22}$$

$$\hat{v}_o(s) = G_{vd}(s)\hat{d}(s) + G_{vg}(s)\hat{v}_{in}(s) + G_{vo}(s)\hat{i}_o(s). \tag{2.23}$$

As the small signal model is linear, each of these transfer functions can be easily determined. As an example,

$$G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)}\Big|_{\hat{v}_{in}(s)=0,\hat{i}_o(s)=0} = \frac{N_{vd}(s)}{Den(s)}.$$

From network theory it is known that the polynomial $Den(s)$ is the same for all the transfer functions, as it depends on the characteristics of the network itself.
In Voltage Mode Control (VMC), control design is usually based on the duty-to-output gain $G_{vd}(s)$. As the SEPIC exhibits a fourth-order dynamics, a general expression for $G_{vd}(s)$ is:

$$G_{vd}(s) = \frac{N_{vd}(s)}{Den(s)} = \frac{n_0 + n_1 s + n_2 s^2 + n_3 s^3 + n_4 s^4}{d_0 + d_1 s + d_2 s^2 + d_3 s^3 + d_4 s^4}. \tag{2.24}$$

Neglecting all parasitics, coefficients of $N_{vd}(s)$ are [42]:

$$\begin{aligned} n_0 &= -V_o R^2 D'^2, \\ n_1 &= V_o R D^2 L_i, \\ n_2 &= n_0 C_s (L_i + L_o), \\ n_3 &= V_o R D C_s L_i L_o, \\ n_4 &= 0. \end{aligned} \tag{2.25}$$

As shown in [26], G_{vd} is characterized by a real Right Half Plane zero (RHPZ) and by a couple of complex conjugate zeros. The application of the Routh Hurwitz criterion [40] to the coefficients (2.25) shows that such zeros can be located in the Right Half Plane or in the Left Half Plane (LHP), depending on the ratio L_r between the output inductance and the input inductance values. Indeed, if $L_r > M$, the complex zeros are LHP. As an example, consider a SEPIC converter with the following specifications: $V_{in} = 3V$, $V_{out} = 3.6V$, $R_{LOAD} = 2.4\Omega$, $f_s = 150kHz$, and let be $L_i = 6.8\mu H$, $L_o = 22\mu H$, $C_o = 270\mu F$, $C_s = 2.2\mu F$. In Fig. 2.3, the duty-to-output gain G_{vd} is shown. Two resonant peaks can be observed. The resonant peak around 20kHz is due to the couple of complex LHP zeros located close to a couple of complex poles. For the same converter, with $L_i = L_o = 6.8\mu H$, G_{vd} is shown in Fig. 2.4. Although the high frequency resonant peak is almost non-existent, the 360 degree phase shift around 20kHz clearly indicates that the complex conjugate zeros are located in the Right Half Plane.

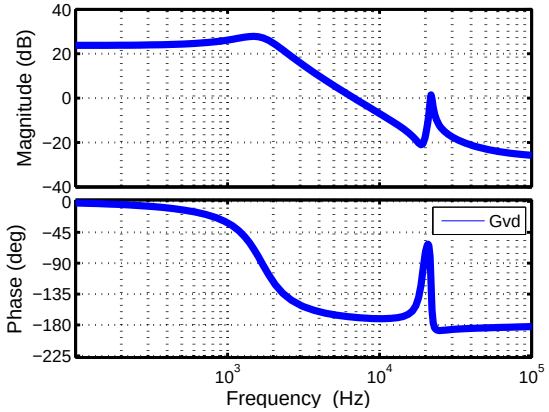

Figure 2.3 Open loop SEPIC G_{vd}. $V_{in} = 3V, V_{out} = 3.6V, R_{LOAD} = 2.4\Omega, L_i = 6.8\mu H, L_o = 22\mu H, C_s = 2.2\mu F, C_o = 270\mu F, f_s = 150kHz$

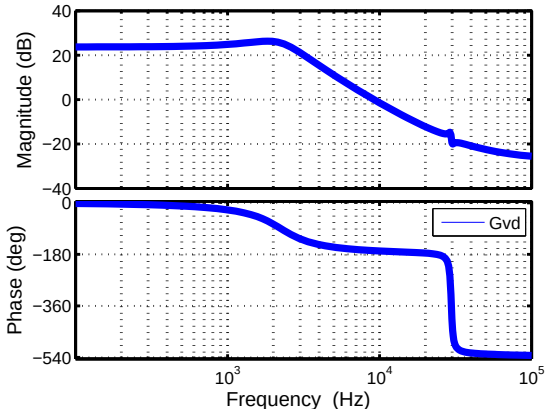

Figure 2.4 Open loop SEPIC G_{vd}. $V_{in} = 3V, V_{out} = 3.6V, R_{LOAD} = 2.4\Omega, L_i = L_o = 6.8\mu H, C_s = 2.2\mu F, C_o = 270\mu F, f_s = 150kHz$

2.2 Closing the current loop

As shown in Fig. 1.9, in current mode control the duty cycle d is a function of the state variables of the converter and of the control input v_c. The average large signal total inductor current for PCC-SEPIC is:

$$i_L = \frac{1}{A_s}\left[v_c - m_a d T_s - \frac{m_1 d^2 T_s}{2} - \frac{m_2 d'^2 T_s}{2}\right] \tag{2.26}$$

where m_a is the slope of the compensation ramp of the current mode control, A_s is the gain of the current sensor and

$$m_1 = A_s\left[\frac{v_{in}}{L_i} + \frac{v_s}{L_o}\right] \tag{2.27}$$

$$m_2 = -A_s\left[\frac{v_{in} - v_s - v_o}{L_i} - \frac{v_o}{L_o}\right]. \tag{2.28}$$

The quantities m_1 and m_2 are proportional to the total inductor current slope during subintervals $[0, DT_s]$ and $[DT_s, T_s]$, respectively. As the compensation ramp is usually generated inside the control IC, it is reasonable to assume that it is constant: $m_a = M_a$ [38]. Small signal models of PCC-SEPIC often used in literature *e.g.*, [42],[46], are obtained assuming $v_s = v_{in}$ in (2.27), (2.28). The small signal model of the current loop is than obtained by perturbing and linearizing (2.26):

$$\hat{d} = \frac{1}{M_a T_s}\left[\hat{v}_c - A_s\hat{i}_L - \frac{\hat{m}_1 D^2 T_s}{2} - \frac{\hat{m}_2 D'^2 T_s}{2}\right], \tag{2.29}$$

$$\hat{m}_1 = A_s\left[\frac{\hat{v}_{in}}{L_{eq}}\right], \tag{2.30}$$

$$\hat{m}_2 = A_s\left[\frac{\hat{v}_o}{L_{eq}}\right], \tag{2.31}$$

where L_{eq} is the parallel of the input and output inductances. This leads to the following simplified expression of CTO gain:

$$G_{vc} = \frac{F_m G_{vd}}{1 + F_m(A_s G_{id} + F'_v G_{vd})}, \tag{2.32}$$

where:

$$F_m = \frac{1}{M_a T_s}, \tag{2.33}$$

$$F_v' = \frac{A_s T_s D'^2}{2L_{eq}}. \tag{2.34}$$

As shown in [42], an approximated sufficient condition for (2.32) having no RHP poles is:

$$L_r = \frac{L_o}{L_i} > \frac{V_o}{V_{in}}. \tag{2.35}$$

Indeed, the open loop gains G_{id} and G_{vd} can be rewritten as:

$$G_{id} = \frac{N_{id}(s)}{Den(s)}, \tag{2.36}$$

$$G_{vd} = \frac{N_{vd}(s)}{Den(s)}. \tag{2.37}$$

From Fig. 2.2 and combining (2.16) with (2.17)-(2.18), G_{id} can be expressed as:

$$G_{id} = \frac{G_{vd}(s)}{(1-D)Z_o(s)} + \frac{I_{out}}{(1-D)^2}, \tag{2.38}$$

where $Z_o(s)$ represent the parallel of the output capacitor C_o with the load resistance R. Hence,

$$N_{id} = \frac{(1-D)N_{vd}(s)(1+sRC_o) + RI_{out}Den(s)}{(1-D)^2 R}. \tag{2.39}$$

Equations (2.36) - (2.39) lead to the following expression for G_{vc}:

$$G_{vc} = \frac{F_m N_{vd}(s)}{Den(s)(1+\frac{F_m A_s I_{out}}{1-D}) + F_m N_{vd}(s)(\frac{A_s(1+sRC_o)}{R} + F_v')} \tag{2.40}$$

The polynomial $Den(s)$ has no RHP solutions, as it is the denominator of the open loop transfer functions. Moreover, F_m,

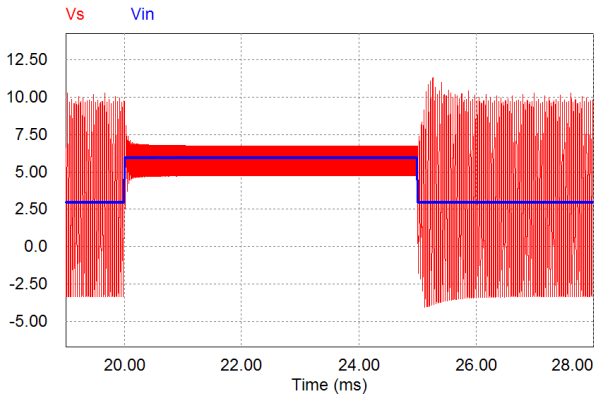

Figure 2.5 PSIM simulation of the coupling capacitor voltage response to a stepwise line transient. $L_i = 6.8\mu H$,$L_o = 10\mu H$, $C_s = 2.2\mu F$,$F_m = 10V^{-1}$

F_v', I_{out}, A_s are positive quantities. Hence, a sufficient condition that guarantees that (2.40) has no RHPPs is to ensure that the polynomial N_{vd} has no RHP solutions. This leads to the stability condition (2.35). It is expected that fulfilling condition (2.35) should ensure that the closed current loop PCC-SEPIC is stable for whatever value of the modulator gain F_m. In [42] it was shown that this is not true. Indeed, (2.35) is not fully reliable, as it hides the effect of coupling capacitor on PCC-SEPIC stability. As an example, consider a PCC-SEPIC converter designed to fulfill the following specifications: $V_{in_{min}} = 3V$, $V_{in_{max}} = 6V$, $V_{out} = 3.6V$, $I_{out} = 1.5A$, $f_s = 150kHz$. Let be $L_i = 6.8\mu H$, $L_o = 10\mu H$, $C_o = 270\mu F$, $ESR_{Co} = 16m\Omega$, $C_s = 2.2\mu F$, $F_m = 10.4V^{-1}$. The maximum voltage conversion ratio is $M_{max} = \frac{V_{out}}{V_{in,min}} = 1.2$. Hence, as $L_r = 1.42$, condition (2.35) should ensure that the converter is stable for any F_m and C_s. Fig. 2.5 shows the simulated response of the converter under study to a line transient. The wide oscillations of the voltage across the coupling capacitor clearly show that the converter is unstable. Increasing the coupling capacitor value to $6.8\mu F$ allows to obtain stable behavior, with the same value of current modulator gain F_m. This is shown in Fig. 2.6. Hence, it is clear that the stability of the PCC SEPIC is conditioned by the value of the coupling capacitance.

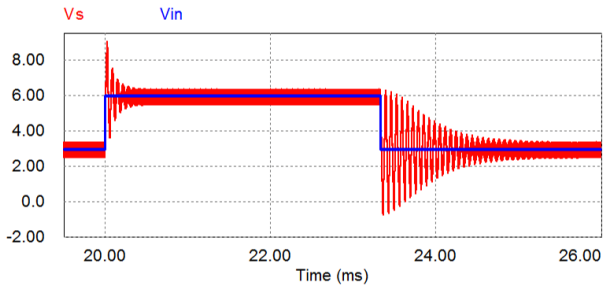

Figure 2.6 PSIM simulation of the coupling capacitor voltage response to a stepwise line transient. $L_i = 6.8\mu H$,$L_o = 10\mu H$, $C_s = 6.8\mu F$,$F_m = 10V^{-1}$

2.2.1 A refined current loop small signal model for the SEPIC

Removing the assumption $v_s = v_{in}$ in (2.27), (2.28), the quantities $\hat{m}_1$ and $\hat{m}_2$ are given by:

$$\hat{m}_1 = A_s \left[\frac{\hat{v}_{in}}{L_i} + \frac{\hat{v}_s}{L_o} \right], \tag{2.41}$$

$$\hat{m}_2 = -A_s \left[\frac{\hat{v}_{in} - \hat{v}_s - \hat{v}_o}{L_i} - \frac{\hat{v}_o}{L_o} \right]. \tag{2.42}$$

Substituting (2.41)-(2.42) in (2.29), the small signal model of the current controller is obtained:

$$\hat{d} = \frac{1}{M_a T_s} \left[\hat{v}_c - A_s \hat{i}_L - F_i \hat{v}_{in} - F_s \hat{v}_s - F_v \hat{v}_{out} \right] \tag{2.43}$$

where:

$$\begin{aligned} F_i &= \frac{A_s}{2f_s}\left(\frac{D^2}{L_i} - \frac{D'^2}{L_i}\right), \\ F_s &= \frac{A_s}{2f_s}\left(\frac{D'^2}{L_i} + \frac{D^2}{L_o}\right), \\ F_v &= \frac{A_s D'^2}{2f_s L_{eq}}. \end{aligned} \tag{2.44}$$

The resulting Control-To-Output (CTO) voltage gain is given by:

$$G_{vc} = \frac{F_m G_{vd}}{1 + F_m(A_s G_{id} + F_s G_{sd} + F_v G_{vd})}. \tag{2.45}$$

The linearized small signal CTO transfer function (2.45) allows the use of analysis techniques developed for linear systems to investigate PCC-SEPIC stability. As stated in chapter 1, the complex pole pair associated with the peak current mode sampling effect [30]-[32] is neglected, as it acts outside the frequency range of interest.

Chapter 3

PCC SEPIC stability boundaries

In this chapter, an analytical stability boundary for PCC-SEPIC derived from a simplified expression of the input-to-coupling capacitor voltage gain will be illustrated. Also, the exact CTO gain (2.45) of PCC-SEPIC will be numerically analyzed to validate the prediction of the analytical stability boundary.

3.1 Analytical stability boundaries of PCC-SEPIC

CCM PCC-SEPIC current loop (CL) stability analysis makes use of the open loop circuit model shown in Fig. 2.2. The importance of the voltage across the coupling capacitor can be clarified considering the slopes of SEPIC input and output inductors currents (2.27), (2.28) : the higher the difference between v_{in} and v_s, the higher the unbalance of voltages across the two inductors and then the higher the amplitude of oscillations of inductor currents and of coupling capacitor voltage during transients. The small signal model of the power stage (2.17)-(2.18) and of the current mode controller (2.43) allow deriving the closed-current loop transfer functions of the converter. Even though each of these functions

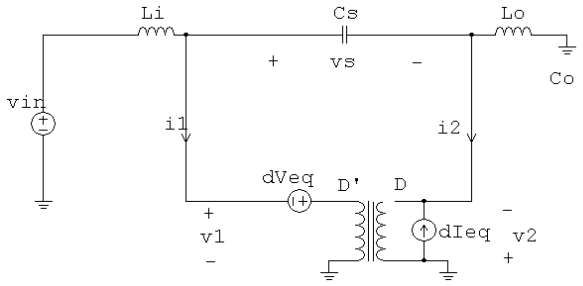

Figure 3.1 Reduced order model of PCC-SEPIC converter power stage.

might be used to evaluate the CL stability, some of them have a quite involved analytical expression. However, some approximations allow isolating the dominant dynamics conditioning stability. As stated in chapter 1, section 1.2.1, using current mode control the low-frequency complex pole pair is split in two real poles, f_{p1} and f_{p2}, associated to the output capacitor and to the inductors respectively. $As f_{p1}$ and f_{p2} are LHP poles, conditions for PCC-SEPIC CL stability can be obtained by analyzing the SEPIC second complex pole pair. This is located at $f_{p_{res}}$ (usually in the range of some tens of kHz) and it is related to the interaction among the inductors and the coupling capacitor. To this aim, the closed-current loop input-to-coupling capacitor voltage gain G_{icc} is considered. Note that the name G_{icc} is introduced to avoid confusions with the open loop input-to-coupling capacitor voltage gain G_{sg}. The coupling capacitor voltage tracks the input voltage from DC up to $f_{p_{res}}$. Hence, the effect of f_{p1} is negligible on G_{icc}. This means that if the output voltage is well regulated the impact of low frequency perturbation of the output voltage on the coupling capacitor voltage can be neglected. Thus, switching off the independent current source $\hat{i_o}$ the small signal model in Fig. 2.2 is modified as shown in Fig. 3.1. Substituting the Laplace transform of the control law (2.43), the reduced order G_{icc} is obtained:

$$G_{icc} = \frac{n_0 + n_1 s + n_2 s^2}{d_0 + d_1 s + d_2 s^2 + d_3 s^3}. \tag{3.1}$$

Neglecting all parasitics elements, coefficients d_i are:

$$\begin{aligned} d_0 &= F_m A_s R^2 V_{in} V_{off}^3 \\ d_1 &= K R^2 V_{in}^3 L_o \\ d_2 &= d_0 C_s (L_i + L_o)(1 - \frac{F_s L_{eq} M}{R A_s C_s}) \\ d_3 &= L_i L_o C_s R^2 V_{in} V_{off}^2 \end{aligned}$$

where:

$$K = V_{off}^2 \frac{F_m}{V_{in}} (\frac{A_s}{R} M + F_s)(1 - \frac{L_i}{L_o} M) + 1 + \frac{L_i}{L_o} M^2$$

The application of the Routh-Hurwitz criterion [40] to the denominator of (3.1) yields the stability conditions summarized in Table 3.1 [52]: where:

Table 3.1 Stability conditions for PCC-SEPIC current loop

$L_r > M$		
$C_{s_{min}} < C_s < C_{s_{min}}/\alpha$	$F_{m_{crit}} > 0$	stable if $F_m > F_{m_{crit}}$
$C_s > C_{s_{min}}/\alpha$	$F_{m_{crit}} < 0$	stable ($F_m > 0$ always)
$L_r < M$		
$C_{s_{min}} < C_s < C_{s_{min}}/\alpha$	$F_{m_{crit}} < 0$	unstable ($F_m > 0$ always)
$C_s > C_{s_{min}}/\alpha$	$F_{m_{crit}} > 0$	stable if $0 < F_m < F_{m_{crit}}$

$$C_{s_{min}} = \frac{F_s L_{eq} I_{out}}{A_s V_{in}}. \tag{3.2}$$

$$F_{m_{crit}} = \frac{(\frac{V_{off}}{V_{in}})^2 \frac{1}{1+L_r} \frac{1}{1-\frac{C_{s_{min}}}{C_s}} - 1 - \frac{M^2}{L_r}}{\frac{V_{off}^2}{V_{in}} (\frac{A_s I_{out}}{V_{in}} + F_s)(1 - \frac{M}{L_r})}. \tag{3.3}$$

$$\alpha = 1 - \frac{(\frac{V_{off}}{V_{in}})^2}{(1 + L_r)(1 + \frac{M^2}{L_r})}.$$

It can be demonstrated that $0 < \alpha < 1$. As a first novel result provided by the new model, the value of the coupling capacitance must be greater than $C_{s_{min}}$ to guarantee PCC-SEPIC stability. Moreover, (3.3) may represent either a lower or an upper boundary for F_m depending on the value of L_r. Also, (3.3) is positive or negative depending on C_s. The worst-case condition for the design of the coupling capacitor in a given application is easily derived from (3.2). Indeed, the minimum value of the coupling capacitance increase with the load current and with the reduction of the input voltage. Table 3.1 highlights that design solutions where $L_r > M$ should be preferred, as $F_{m_{crit}}$ represents a minimum value for the current modulator gain, and there exist conditions that guarantee the stability of the current loop regardless of F_m value. For example, let us consider a PCC-SEPIC with the following specifications: $V_{in_{min}} = 4V$, $V_{in_{max}} = 24V$, $V_{out} = 5V$, $I_{out} = 1A$, $f_s = 100kHz$. Let be $L_i = 56\mu H$ and $L_o = 150\mu H$, to satisfy some given constraint on the input and output inductors current ripple. Note that $C_{s_{min}} = 0.3\mu F$ and $L_r = 2.67$, while the maximum voltage conversion ratio (M_{max}) value is 1.25. Hence, $L_r > M_{max}$, so that $F_{m_{crit}}$ is a lower boundary for F_m. The stability boundary curve relating F_m and C_s is shown in Fig. 3.2. Regions A (blue shade) and B (green shade) correspond to F_m values that ensure the current loop stability. In particular, if $C_s > C_{s_{crit2}} = 2.36\mu F$ (region B) then the CL is stable for any F_m. Region C corresponds to CL instability: for $C_s < C_{s_{crit1}} = 0.3\mu F$ the CL is unstable for any F_m. The gray shaded area refers to negative F_m values, which have no physical meaning. Fig. 3.3, Fig. 3.4 and Fig. 3.5 show results of PSIM® simulations for three couples of values (F_m, C_s) identified by red circles in Fig. 3.2 and labelled as $\#1, \#2, \#3$ respectively. Low frequency oscillations in Fig. 3.3 confirm CL instability in region C.

Next, let us consider a PCC-SEPIC designed to met the same specifications of the previous example, with $L_i = 56\mu H$ and $L_o = 47\mu H$. As $L_r = 0.83$, $F_{m_{crit}}$ is an upper boundary for F_m when $V_{in} = V_{in_{min}}$. The stability boundary @ $V_{in_{min}}$ as a function of F_m and C_s is shown in Fig. 3.6. $F_{m_{crit}}$ is negative if $C_s < C_{s_{crit2}} =$

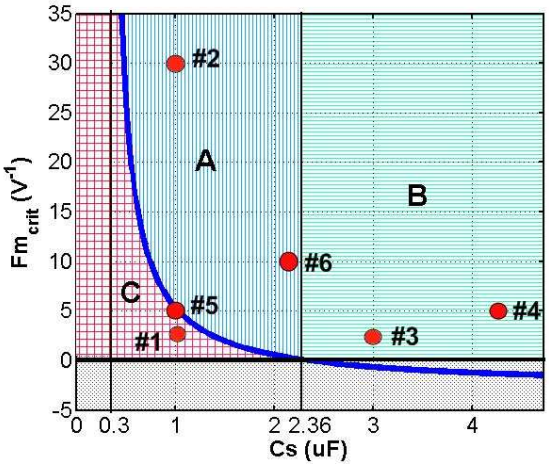

Figure 3.2 Current modulator gain boundary curve. $L_r > M$.

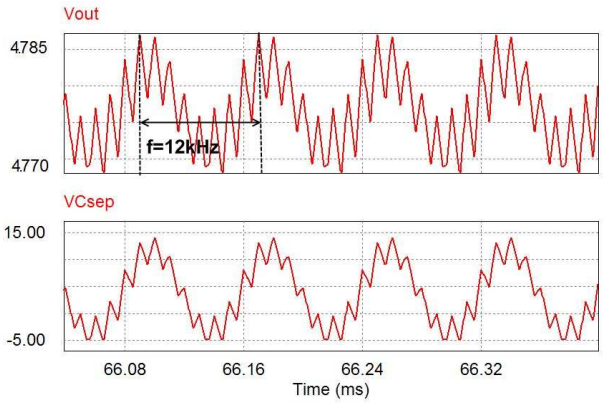

Figure 3.3 $V_o, V_{cs}, C_s = 1\mu F, F_m = 3V^{-1}(\#1, regionC)$

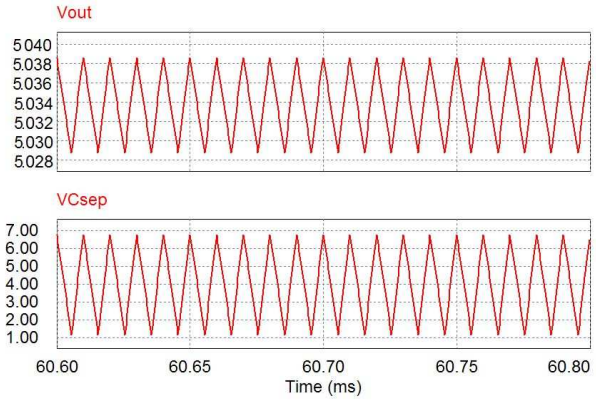

Figure 3.4 $V_o, V_{cs}, C_s = 1\mu F, F_m = 30V^{-1}(\#2, regionA)$

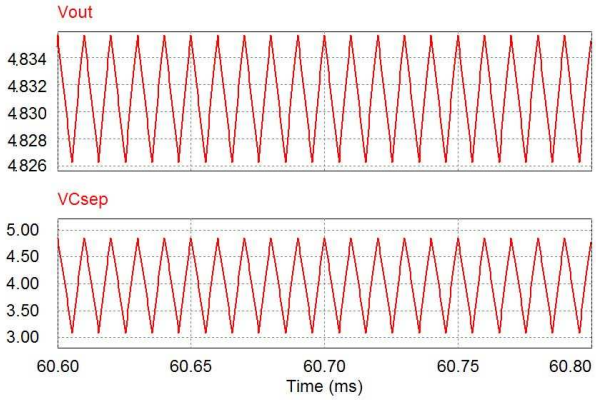

Figure 3.5 $V_o, V_{cs}, C_s = 3\mu F, F_m = 3V^{-1}(\#3, regionB)$

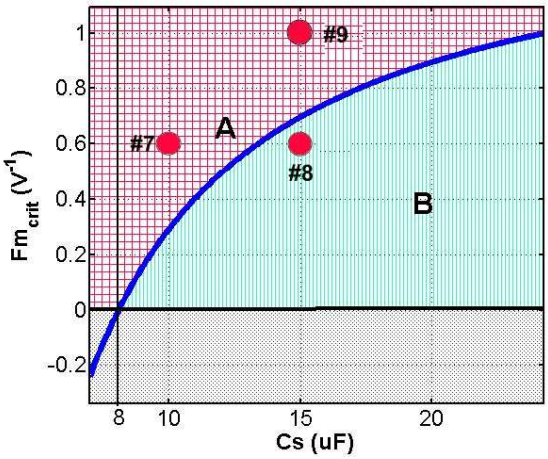

Figure 3.6 Current modulator gain boundary curve. $L_r < M$.

$8\mu F$. Results of PSIM® simulations are shown in Fig. 3.7, Fig. 3.8 and Fig. 3.9. Low frequency oscillations in Fig. 3.7 and Fig. 3.8 confirm that F_m values within region A (i.e. $F_m > F_{m_{crit}}$) lead to CL instability.

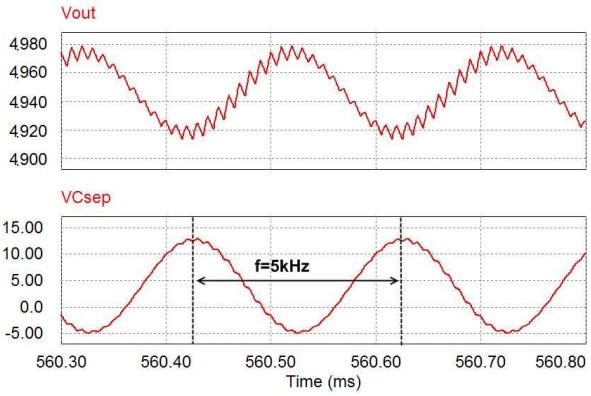

Figure 3.7 $V_o, V_{cs}, C_s = 10\mu F, F_m = 0.6V^{-1}(\#7, regionA)$

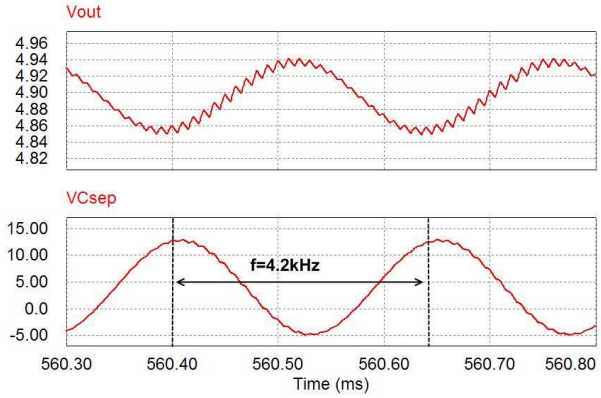

Figure 3.8 $V_o, V_{cs}, C_s = 15\mu F, F_m = 1V^{-1}(\#9, regionA)$

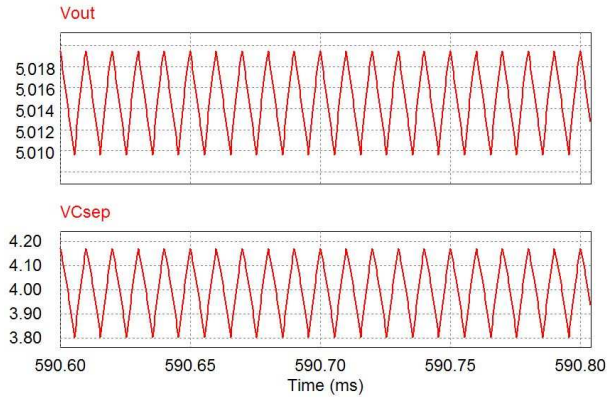

Figure 3.9 $V_o, V_{cs}, C_s = 15\mu F, F_m = 0.6V^{-1}(\#8, regionB)$

3.1.1 The impact of losses on stability predictions

For the SEPIC converter considered in the previous example, prediction based on the lossless reduced-order model lead to conclude that very low values of F_m are mandatory in order to ensure CL stability when $L_r < M$. To investigate the impact of power losses on stability, a complete model of PCC-SEPIC has been developed using the steady state averaging technique and including resistive losses of the power components. This model also include the small signal variations of the output voltage $\hat{v}_o$, which were neglected to derive the analytical stability boundary summarized in Table 3.1. The plots of the stability region as a function of F_m and C_s values have been generated through a numerical procedure and are shown in Fig. 3.10 and Fig. 3.11. In Fig. 3.10,

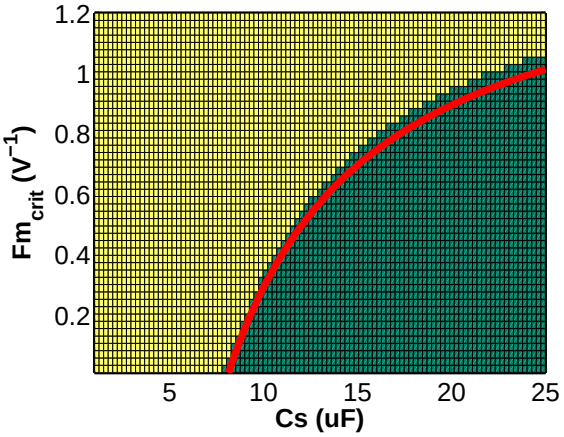

Figure 3.10 PCC-SEPIC stability region (dark green area). $V_{in} = V_{in,min}, L_i = 56\mu H, L_o = 47\mu H$. All parasitics are neglected.

the stability region for the PCC-SEPIC described in section 3.1 is highlighted in dark green. $L_i = 56\mu H$ and $L_o = 47\mu H$. This plot was obtained by neglecting all parasitics. The red line represents the boundary obtained through the use of the reduced-order model proposed in section 3.1. The SSA model confirms that there exist a minimum capacitance C_s below which stabil-

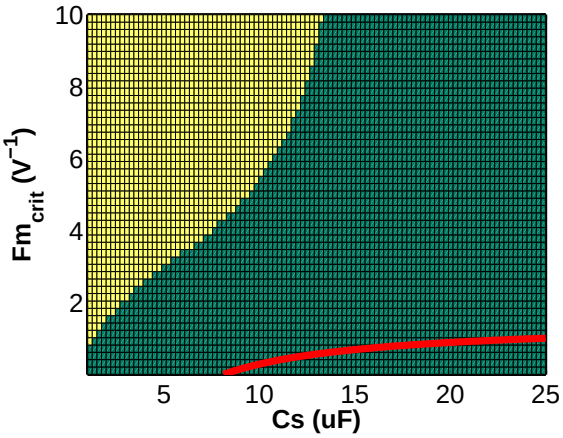

Figure 3.11 PCC-SEPIC stability region (dark green area). $V_{in} = V_{in,min}, L_i = 56\mu H, L_o = 47\mu H. R_{Li} = R_{Lo} = 100m\Omega$.

ity cannot be achieved. Also, to obtain stable behavior F_m cannot be increased above a maximum value, which is around $1V^{-1}$. Fig. 3.11 shows how the stability region is modified when the DC resistances of the inductors are included in the SSA model. A value of $100m\Omega$ has been used for both inductors. The stability boundary changes dramatically with respect to the ideal case. The minimum value for the coupling capacitance decreases, and there exist a critical value for such capacitance above which the current modulator gain can be increased without affecting the current loop stability. In Fig. 3.12, PSIM® simulations with $C_s = 15\mu F, L_i = 56\mu H, L_o = 47\mu H, R_{Li} = R_{Lo} = 100m\Omega$ and $F_m = 5V^{-1}$ are shown. Simulations show that the converter is stable, as predicted by the SSA model. Comparisons between the reduced-order model and the SSA model stability predictions for the converter stability for the example under study when $L_r > M$ are shown in Fig. 3.13 and Fig. 3.14. It is evident that the stability boundary obtained using the reduced-order lossless model is much more reliable when $L_r > M$.

It is worth noticing that the beneficial impact of resistive losses on PCC-SEPIC is reported in [47]. Unfortunately, losses of power converters are not constant, as they depend on electrical and ther-

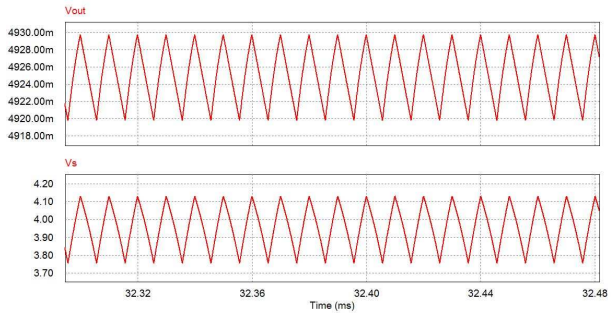

Figure 3.12 $V_o, V_{cs}, C_s = 15\mu F, V_{in} = V_{in,min}, Li = 56\mu H, Lo = 47\mu H. R_{Li} = R_{Lo} = 100m\Omega, F_m = 5V^{-1}$

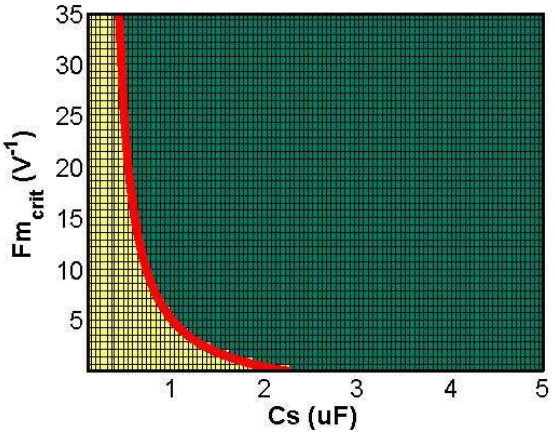

Figure 3.13 PCC-SEPIC stability region (dark green area). $V_{in} = V_{in,min}, L_i = 56\mu H, L_o = 150\mu H$. All parasitics are neglected.

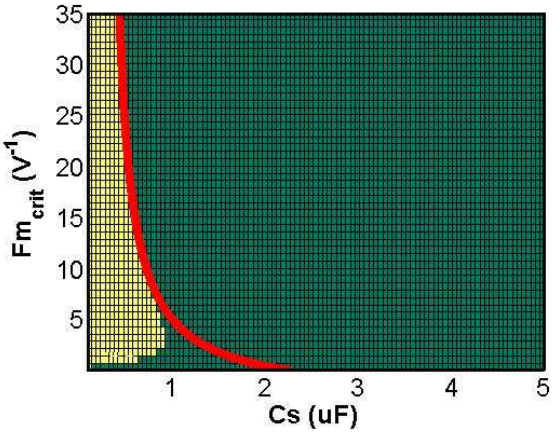

Figure 3.14 PCC-SEPIC stability region (dark green area). $V_{in} = V_{in,min}, L_i = 56\mu H, L_o = 150\mu H. R_{Li} = R_{Lo} = 100m\Omega$.

mal operating conditions:

$$\eta = f(V_{in}, V_{out}, I_{out}, T_{amb}), \tag{3.4}$$

where T_{amb} is the ambient temperature. This imply that the stabilizing effect of losses is uncertain and unreliable. For the example under study, the efficiency is quite low and the analytical prediction of lossless model when $L_r < M$ is too much conservative. However, Fig. 3.10 suggests that for high efficiency applications the predictions of the analytical model are more realistic.
The analytical model proposed in section 3.1 discloses the correlations that exist among parameters of passive components, current modulator gain and losses. To obtain reliable and not too conservative stability conditions for PCC-SEPIC, numerical calculations on the complete model of the converter (including losses) are needed.
In the next section, a numerical approach is proposed. A complete SSA model of PCC-SEPIC is applied to highlight the impact of the coupling capacitance and of the input and output inductances on stability. F_m is fixed to a given value, to avoid sub-harmonic oscillations typical of current mode control.

3.2 Inductive damping

The CTO gain (2.45) can be rewritten as the ratio between two fourth-order polynomials in the variable s:

$$G_{vc} = \frac{a_0 + a_1 s + a_2 s^2 + a_3 s^3 + a_4 s^4}{b_0 + b_1 s + b_2 s^2 + b_3 s^3 + b_4 s^4}. \tag{3.5}$$

The sign of real part of poles of (3.5) can be analyzed by means of the Routh-Hurwitz criterion to investigate the stability of the PCC-SEPIC. As the poles depend on L_i and L_o, numerical application of the Routh-Hurwitz criterion allows determining a region in the plane L_i-L_o where stability is guaranteed for any couples of inductors whose inductance falls in this region. Let us consider, for example, a converter designed to meet the following specifications: $V_{in_{min}} = 3V$, $V_{in_{max}} = 6V$, $V_{out} = 3.6V$, $R_{LOAD} = 2.4\Omega$, $f_s = 150kHz$, and let be $C_o = 270\mu F$, $ESR_{Co} = 16m\Omega$, $C_s = 2.2\mu F$, $F_m = 10.4V^{-1}$. The stability region at minimum and maximum input voltage obtained by means of Routh-Hurwitz criterion are shown in Fig. 3.15 and Fig. 3.16 respectively. It is evident that the critical operating point is at minimum input voltage. The

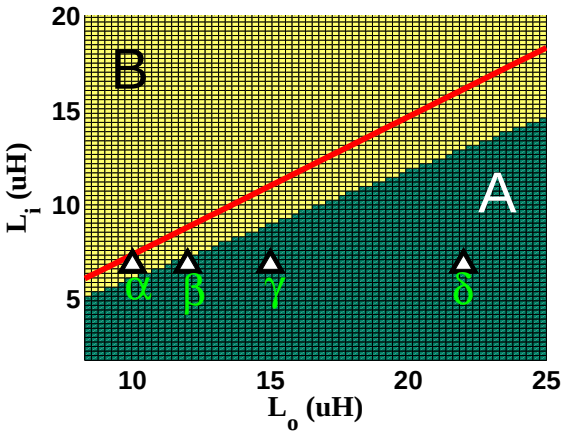

Figure 3.15 $L_i - L_o$ stability map for the converter under study @ $V_{in_{min}}$

couples of input and output inductors that ensure stability are located in the portion of the plane marked by the letter A. The

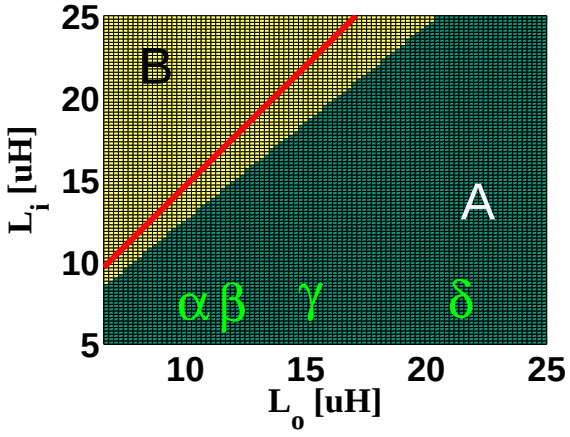

Figure 3.16 $L_i - L_o$ stability map for the converter under study @ $V_{in_{max}}$

couples of inductors lying in the portion of the plane marked with the letter B lead to instability. The red line represents the linear stability boundary $L_o = ML_i$ derived from the simplified model (2.32). As previously discussed in chapter 2, section 2.2, stability prediction based on such model are not reliable. The values

Table 3.2 couples of input and output inductors

	$L_i[\mu H]$	$L_o[\mu H]$
α	6.8	10
β	6.8	12
γ	6.8	15
δ	6.8	22
ϵ	6.8	47

of inductances listed in 3.2, together with the fixed value of F_m, provide a value comprised between 1 and 1.6 for the ratio between the slope of the compensation ramp and the falling slope of the current in L_{eq}, so that instability of the current loop due to subharmonic oscillations is prevented (refer to chapter 1 section 1.1 for more details). According to Fig. 3.15, combination α leads to instability, although the approximated condition (2.35) would predict otherwise. To confirm this result, the response of the system to a step line transient from $V_{in_{min}}$ to $V_{in_{max}}$ and viceversa has

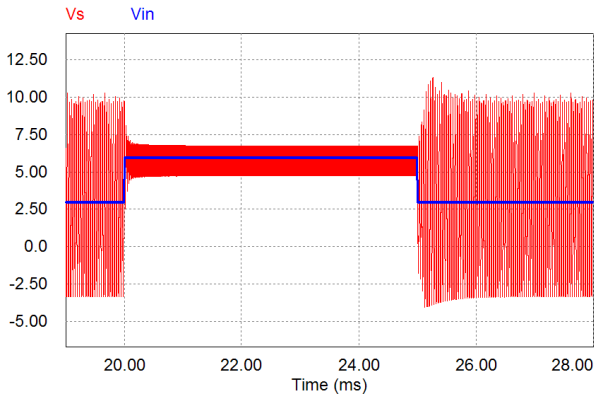

Figure 3.17 PSIM simulation of the coupling capacitor voltage response to a stepwise line transient. Inductors combination α

been simulated using PSIM®. The result is shown in Fig. 3.17. The wide oscillations affecting the voltage across the coupling capacitor clearly indicate that the system is unstable. Inductors combinations β and γ, instead, fall inside the stability region. Indeed, both design solutions guarantee that the CTO gain has no RHPPs. Bode plots of the CTO gain and PSIM simulation of step line transient with closed current loop and open voltage loop, with inductance combinations β and γ, are shown in Fig. 3.18 - Fig. 3.20. Fig. 3.18 confirms that there are no RHPPs in the CTO gain using inductor combination β. However, a severe resonant peak can be observed. Fig. 3.19 shows that oscillations at minimum line voltage with combination of inductors β are not well damped. Combination of inductors γ provides a higher damping factor, as shown in Fig. 3.20. To highlight the correlation between the oscillations of the coupling capacitor voltage due to line transients and the ratio between L_i and L_o, it is useful to refer to the closed current loop input-to-coupling capacitor voltage gain, G_{icc}. The plot of the damping factor ζ of the complex pole pair of G_{icc} as a function of the output inductance calculated at minimum input voltage is shown in Fig. 3.21. Inductances combination γ provides a damping factor of 0.05. To get a damping factor of 0.15, a higher output inductance is needed (combination δ). The stabil-

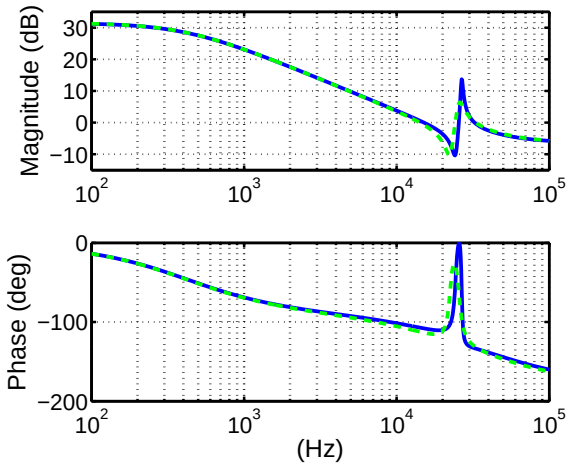

Figure 3.18 MATLAB generated CTO gain @ $V_{in_{min}}$, inductors combination β (solid blue line) and γ (dashed green line)

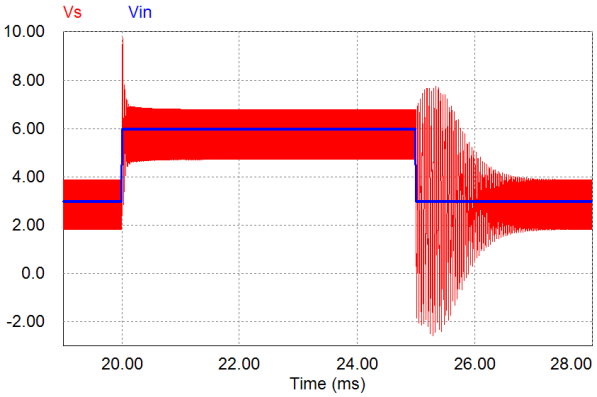

Figure 3.19 PSIM simulation of the coupling capacitor voltage response to a stepwise line transient. Inductors combination β

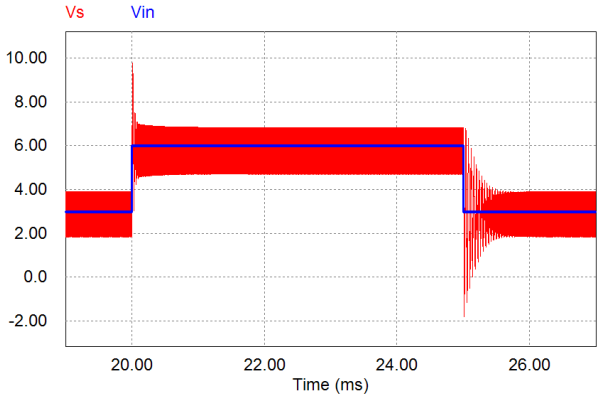

Figure 3.20 PSIM simulation of the coupling capacitor voltage response to a stepwise line transient. Inductors combination γ

ity boundary limit is conditioned by the value of the capacitance C_s. In Fig. 3.21, the dashed line is referred to $C_s = 47\mu F$. It is clear that a smaller value of L_o is sufficient to ensure stability in this case. However, the maximum damping factor is reduced with respect to the case $C_s = 2.2\mu F$. Fig. 3.22 shows the damping

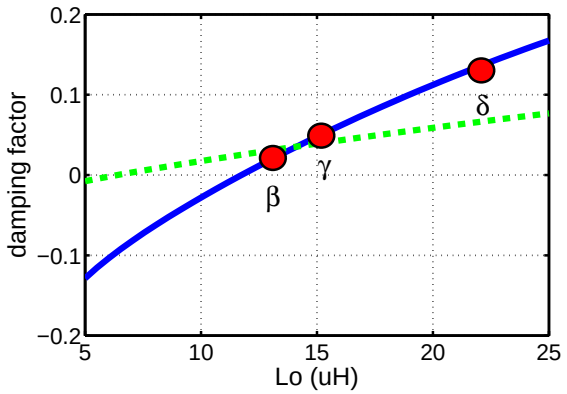

Figure 3.21 Damping factor of G_{icc} complex pole pair @ $V_{in_{min}}$. $L_i = 6.8\mu H$, $C_s = 2.2\mu F$ (solid line) , $C_s = 47\mu F$ (dashed line)

factor of the complex pole pair of G_{icc} plotted as a function of C_s, calculated numerically and parameterized for three values of L_o. The damping factor of the complex pole pair of G_{icc} exhibits a

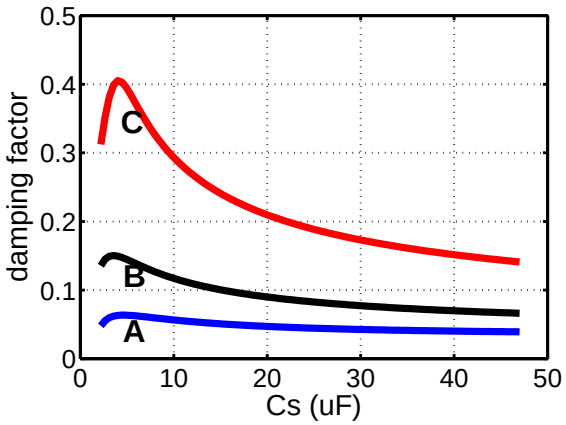

Figure 3.22 Damping factor of G_{icc} complex pole pair @ $V_{in_{min}}$. $L_i = 6.8\mu H . L_o = 15\mu H$ (curve A) , $22\mu H$ (curve B) , $47\mu H$ (curve C).

maximum for a certain value of the capacitance C_s. This result is confirmed by the simulated time response of the coupling capacitor voltage to a step-wise variation of the input voltage, shown in Fig. 3.23 for two values of C_s using inductances combination ϵ. It is worth to notice that the maximum obtainable damping factor is a function of the ratio L_r, while the value of the coupling capacitor corresponding to this maximum value changes with the absolute value of L_i and L_o. This is shown in table 3.3, where the results of simulation for different L_i, L_o and C_s values are summarized. This results suggest that to obtain both stability and a desired

Table 3.3 Maximum damping factor of G_{icc} complex pole pair @ $V_{in_{min}}$

$L_i[\mu H]$	$L_o[\mu H]$	L_r	$C_s[\mu F]$	ζ_{max}
6.8	15	2.2	3.9	0.06
10	22	2.2	3.9	0.06
18	39	2.2	3.9	0.06
6.8	22	3.23	3.9	0.15
10	33	3.3	3.9	0.15
18	68	3.23	6.8	0.15
6.8	47	6.9	3.9	0.4
10	68	6.8	5.6	0.4
18	120	6.66	10	0.39

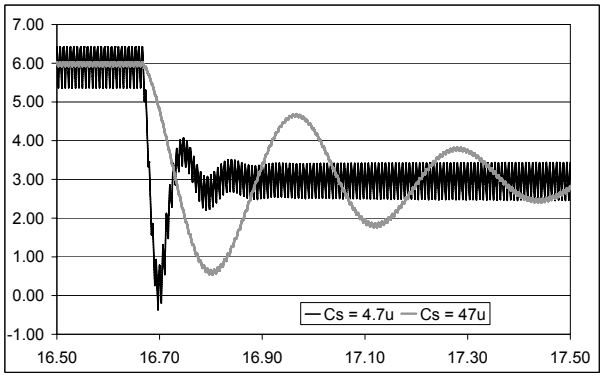

Figure 3.23 PSIM simulation of the coupling capacitor voltage response to a stepwise line transient. Inductance combinations ϵ. $C_s = 4.7\mu F$ (black line),$C_s = 47\mu F$ (gray line). $V_{in_{max}} = 6V, V_{in_{min}} = 3V$.

line transient behavior in PCC-SEPIC a compromise between the value of the coupling capacitor C_s and a minimum value for the ratio L_r is needed. As a general rule, it seems reasonable to identify a set of parameters for the power stage components that ensure the desired performances without imposing too tight constraints on the single components value. As an example, this would be the preferred design strategy in applications with a wide input voltage range. However, this is not always possible. Indeed, the SEPIC coupling capacitor is usually a ceramic one, since it has to sustain a discontinuous current with a possible high RMS content at the switching frequency. As a result, it is preferable to limit its capacitance, to avoid an increase in cost. This is especially true when high values of input voltage are reached. Similary, as highlighted in table 3.3, a bulky output inductor might be needed to get a desired damping factor. In many applications it is desirable to keep the input current peak-to-peak ripple below a certain threshold. Indeed, one of the advantages of the SEPIC is the presence of an input inductance. Considering the aforementioned converter with inductors combination δ, the peak-to-peak current ripple is 110% for the input inductor and 50% for the output inductor. If the target input current ripple was around 40% @ $V_{in_{min}}$, an $18\mu H$ input inductance would be needed. Then, from table 3.3, an out-

put inductance of $68\mu H$ should be selected if a damping factor of 0.15 is desired. Bigger output inductances are needed if a higher damping factor is required, or if the 40% input current ripple constraint has to be maintained for all the input voltage range. Next section shows how capacitive damping of PCC-SEPIC can help in these cases.

3.3 Capacitive damping

Fig. 3.24 shows the PCC-SEPIC with the additional R-C damping branch. R_d and C_d identify the elements of the damping branch. In order to be effective, the series R_d - C_d must be designed to offer a lower impedance path to the low frequency current harmonics, if compared with the impedance of C_s. In this way, the use of a sufficiently high capacitance C_d helps in limiting the low frequency oscillations of the coupling capacitor voltage, relaxing the constraint on the ratio L_r. As the RMS current value is due mainly to the harmonic components at the switching frequency, still flowing in C_s, the damping branch can be realized with an electrolytic capacitor. So, a high value C_d can be used without a significant increase in cost. To achieve the desired value for R_d, a commercial resistor can be put in series to C_d. To determine an appropriate combination of R_d and C_d values that allow to obtain a desired damping factor, it is useful to refer to G_{icc}. As already mentioned in section 3.2, G_{icc} is obtained by analyzing the SEPIC with closed current loop and open voltage loop. Moreover, as done in section 3.1, it is reasonable to assume that the output capacitor has sufficiently high capacitance, so that its influence on the ac voltage on the coupling capacitor can be neglected. Hence a reduced-order model for PCC-SEPIC with additional R-C branch can be obtained. The gain G_{icc} can be written as:

$$G_{icc} = G_{icc0} \frac{(\frac{s^2}{\omega_{z1}^2} + \frac{2\zeta_{z1}}{\omega_{z1}} s + 1)(1 + \frac{s}{\omega_{z2}})}{(\frac{s^2}{\omega_{p1}^2} + \frac{2\zeta_{p1}}{\omega_{p1}} s + 1)(\frac{s^2}{\omega_{p2}^2} + \frac{2\zeta_{p2}}{\omega_{p2}} s + 1)}. \tag{3.6}$$

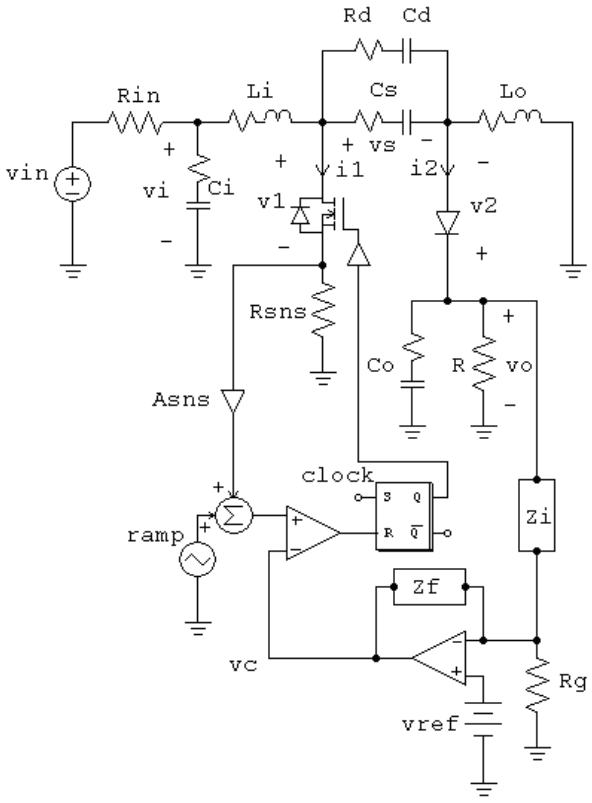

Figure 3.24 PCC SEPIC with parallel damping branch

One of the two trinomial terms of the denominator of (3.6) corresponds to a couple of dominant complex conjugated poles. The resonant frequency and damping factor of such dominant poles are referred to as ω_{p1} and ζ_{p1} respectively. The input voltage-to-input inductor current gain (G_{iLi}) and the input voltage-to-output inductor current gain (G_{iLo}) of PCC-SEPIC will also be used to select R_d and C_d values given a desired damping factor ζ:

$$G_{iLi} = G_{iLi0}\frac{(\frac{s^2}{\omega_{zi1}^2} + \frac{2\zeta_{zi1}}{\omega_{zi1}}s + 1)(1 + \frac{s}{\omega_{zi2}})}{(\frac{s^2}{\omega_{p1}^2} + \frac{2\zeta_{p1}}{\omega_{p1}}s + 1)(\frac{s^2}{\omega_{p2}^2} + \frac{2\zeta_{p2}}{\omega_{p2}}s + 1)}, \tag{3.7}$$

$$G_{iLo} = G_{iLo0}\frac{(\frac{s^2}{\omega_{zi1}^2} + \frac{2\zeta_{zo1}}{\omega_{zo1}}s + 1)(1 + \frac{s}{\omega_{zo2}})}{(\frac{s^2}{\omega_{p1}^2} + \frac{2\zeta_{p1}}{\omega_{p1}}s + 1)(\frac{s^2}{\omega_{p2}^2} + \frac{2\zeta_{p2}}{\omega_{p2}}s + 1)}. \tag{3.8}$$

The explicit expression of ζ_{p1} (ζ in the following) as a function of circuit parameters is quite involved. However, its graphical representation is much expressive in unveiling the role of the damping branch in SEPIC dynamics. G_{icc} has been evaluated at minimum input voltage and maximum load, for the same converter of section 3.2 and assuming $L_i = L_o = 6.8\mu H$. Fig. 3.25 shows the map of ζ for different values of R_d-C_d. Fig. 3.25 highlights that for each desired ζ there are infinite couples R_d-C_d that could be used. As an example, given a desired ζ of 0.3, three possible couples of R_d and C_d have been selected using the map in Fig. 3.25. The values of these couples are listed in table 3.4. A good solution for the

Table 3.4 R_d, C_d values. Desired ζ: 0.3

	$R_d(m\Omega)$	$C_d(\mu F)$
a	2500	4.7
b	550	18
c	3300	18

damping branch values should be characterized by its robustness with respect to parameters changes and by low power dissipation. An additional property to be considered is the settling time of

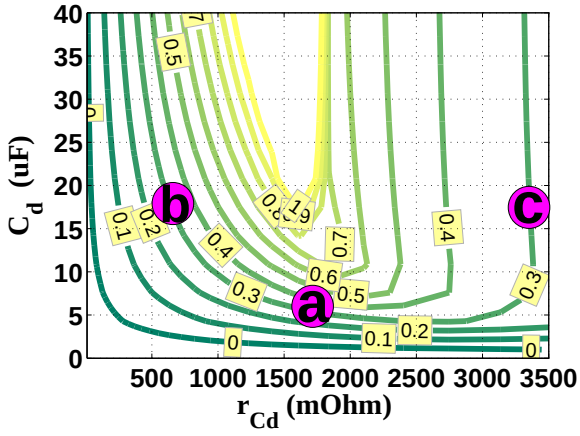

Figure 3.25 Damping map for the converter under study

the voltage across the coupling capacitor in response to changes in the input voltage. The importance of this last point will be clarified in the following. Considering solution **a** in table 3.4 and Fig. 3.25, it can be observed that ζ is much sensitive to the variations of capacitance C_d. This could be a major issue given the wide tolerance of capacitance usually found in commercial capacitors. Based on this consideration, good solutions would seem to be **b** and **c**. To further investigate the role of the R-C branch on the converter dynamics, table 3.5 shows the peak magnitude of the input-to-input inductor current gain and its frequency location for six couples of R_d and C_d values chosen to guarantee $\zeta = 0.3$, according to Fig. 3.25. The peak magnitude increases as R_d

Table 3.5 G_{iLi} peak magnitude and frequency location. The couples R_d, C_d are selected to get $\zeta = 0.3$

$R_d[m\Omega]$	$C_d[\mu F]$	$peak[dB]$	$f_{peak}[kHz]$
550	18	18.8	10.2
1000	8.2	13.4	14.7
1500	6.8	7.9	16
2000	5	7.7	19
3000	4.7	6	24
3300	18	1.31	29

value is reduced, while its frequency location increases as R_d value is increased. Consequently, if a step change in the input voltage is applied, the settling time of the input inductor current around its steady-state value increases, together with its peak value, if small values of R_d are selected. In Fig. 3.26 and Fig. 3.27, PSIM® time domain simulations of the response of the coupling capacitor voltage and of the input and output inductors current to a step down line transient are shown. Simulation are run with

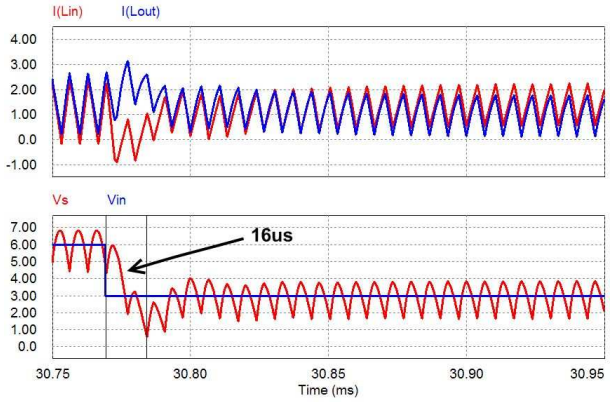

Figure 3.26 Simulated input and output inductor current response to a line step transient. $R_d = 3300m\Omega, C_d = 18\mu F$ (solution c)

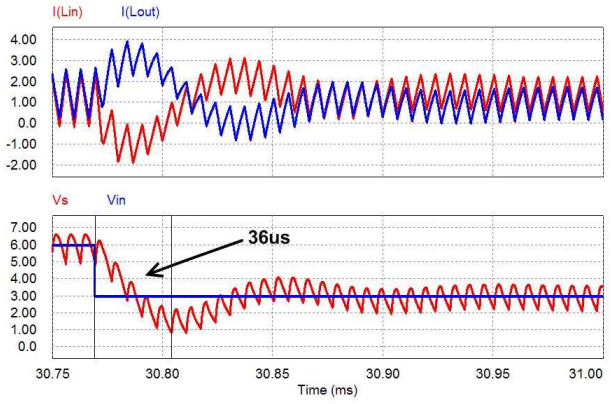

Figure 3.27 Simulated input and output inductor current response to a line step transient. $R_d = 550m\Omega, C_d = 18\mu F$ (solution b)

closed current loop and open voltage loop. It takes around $16\mu s$ for the coupling capacitor voltage V_s to reach its lower peak if solution **c** is considered, and almost $36\mu s$ if solution **b** is considered. Note that for both solutions **b** and **c** the lower peak of V_s is $1V$. Hence, if the system was a second-order one, it would be possible to conclude that **b** and **c** lead to the same ζ just by inspecting the time domain responses in Fig. 3.26 and Fig. 3.27. As a result of the lower resonant frequency of solution **b**, the voltage unbalance around the inductors persists for a longer period of time, and the peak inductors current increase. Unexpected high peaks can lead to saturation of inductors. Fig. 3.28 shows the plot of power dissipated in the damping resistor as a function of resistance R_d at the switching frequency. Given a desired ζ, a high value of R_d is to be preferred, as a smaller fraction of the current harmonics at the switching frequency is diverted from the ceramic capacitor to the parallel damping branch.

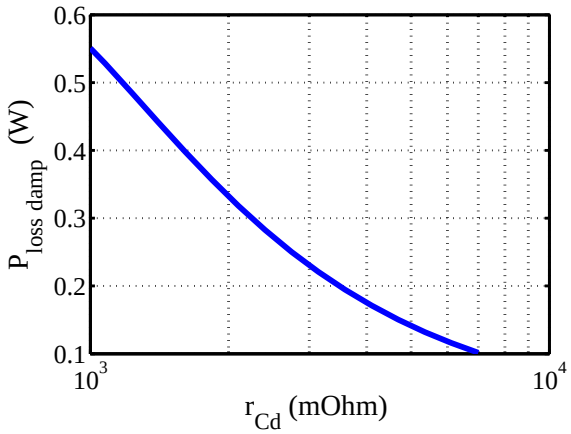

Figure 3.28 Predicted power dissipation in the damping branch for different values of R_d. The couples R_d, C_d are selected to get $\zeta = 0.3$

Chapter 4

Stability boundaries of PCC-Cuk converter

4.1 Cuk converter averaged models and open loop small signal transfer functions

The schematic of the peak-current mode controlled Cuk converter is shown in Fig. 4.1. Note that the output voltage is taken as positive. The switching cell port variables are highlighted. The large signal averaged model of the switching cell can be obtained using the same circuit averaging approach shown in chapter 2. Inspection of Fig. 4.1 allows to derive equations (4.1)-(4.4) for the averaged port voltages and currents:

$$\langle i_1 \rangle = d i_L, \tag{4.1}$$
$$\langle i_2 \rangle = d' i_L, \tag{4.2}$$
$$\langle v_1 \rangle = R_{ds} \langle i_1 \rangle + d'(v_s + V_d) + R_d \langle i_2 \rangle, \tag{4.3}$$
$$\langle v_2 \rangle = d v_s - d' V_d - R_{ds} \langle i_1 \rangle - R_d \langle i_2 \rangle. \tag{4.4}$$

As highlighted in chapter 2, the voltage v_s across the coupling capacitor is considered constant in T_s. From Fig. 4.1 it is easy to

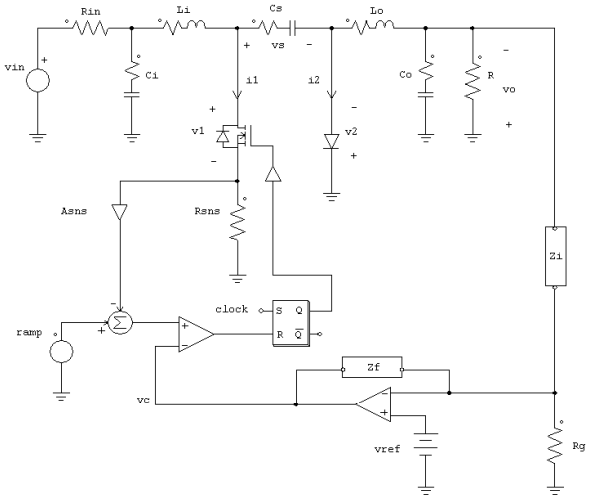

Figure 4.1 PCC-Cuk converter schematic

verify that:

$$v_s = v_1 + v_2 \tag{4.5}$$

The switching cell averaged terminal currents are related by the following equation:

$$\langle i_1 \rangle = \frac{d}{d'} \langle i_2 \rangle \tag{4.6}$$

Solving v_s from (4.4) and making use of (4.6), the terminal voltages of the switching cell can be related:

$$\langle v_1 \rangle = \frac{d'}{d} \langle v_2 \rangle + R_{eq}(d) \langle i_1 \rangle + \frac{d'}{d} V_d, \tag{4.7}$$

where:

$$R_{eq}(d) = \frac{R_{ds}}{d} + \frac{d'}{d^2} R_d. \tag{4.8}$$

Equations (4.6) and (4.7) represent the large signal averaged model of the Cuk converter switching cell. It is important to notice that the large signal averaged model of the switching cell is the same for

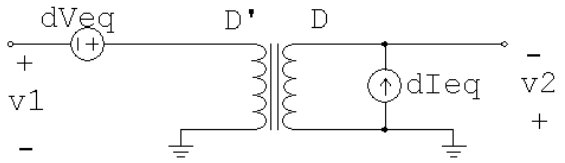

Figure 4.2 Cuk converter switching cell small signal lossless model

both SEPIC and Cuk converters, as R_{eq} is the same. Perturbing and linearizing (4.6) and (4.7), the DC model and the small signal model of the switching cell can be obtained. In chapter 1 it was shown that the DC value of the voltage v_s is equal to the sum of the input and output voltages:

$$V_s = V_{in} + V_{out} \tag{4.9}$$

From (4.1), (4.2), (4.5) and (4.9) it follows that:

$$\begin{aligned} V_1 + V_2 &= V_{in} + V_{out} = V_{off}, \\ I_1 + I_2 &= I_{in} + I_{out} = I_{on}. \end{aligned} \tag{4.10}$$

In Fig. 4.2 the lossless small signal linear circuit of the switching cell is shown, where:

$$V_{eq} = \frac{V_{off}}{D}$$
$$I_{eq} = \frac{I_{on}}{D}$$

The small signal model of Cuk converter is shown in Fig. 4.3. In the frequency domain, relationships among the input variables $\hat{d}(s)$, $\hat{v}_{in}(s)$, $\hat{i}_o(s)$ and the output variables $\hat{i}_L(s)$, $\hat{v}_s(s)$, $\hat{v}_o(s)$ can be expressed in compact form by means of the small-signal transfer functions:

$$\hat{i}_L(s) = G_{id}(s)\hat{d}(s) + G_{ig}(s)\hat{v}_{in}(s) + G_{io}(s)\hat{i}_o(s), \tag{4.11}$$
$$\hat{v}_s(s) = G_{sd}(s)\hat{d}(s) + G_{sg}(s)\hat{v}_{in}(s) + G_{so}(s)\hat{i}_o(s), \tag{4.12}$$
$$\hat{v}_o(s) = G_{vd}(s)\hat{d}(s) + G_{vg}(s)\hat{v}_{in}(s) + G_{vo}(s)\hat{i}_o(s). \tag{4.13}$$

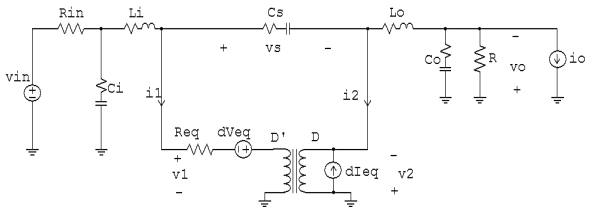

Figure 4.3 PCC-Cuk averaged model

In chapter 2 it was shown that the open loop SEPIC duty-to-output voltage gain G_{vd} is characterized by a real RHP zero and by a complex conjugate zeros pair which can be located either in the RHP or in the LHP depending on the ratio L_r between output and input inductances. It was also shown that stability properties of the PCC-SEPIC are influenced by the location of this zero pair in the complex plane. The zeros of the Cuk converter G_{vd} exhibits quite a different behavior. Indeed, in [46] it is shown that G_{vd} of a lossless Cuk converter has a complex zeros pair which is always located in the RHP. Also, as the output inductor is continuously supplying current to the load, the real RHP zero typical of converters with a boost-derived output stage is non present. In [46] it is also shown that the complex zeros can be located in the LHP if resistive losses of the components are considered. For the sake of simplicity, let's consider only the ESR of the input inductor r_{Li}. G_{vd} can be rewritten as:

$$G_{vd} = \frac{N_{vd}(s)}{Den(s)},$$

where: $N_{vd}(s) = n_2 s^2 + n_1 s + n_0$.
Coefficients of the polynomial $N_{vd}(s)$ are:

$$\begin{aligned} n_2 &= -RL_iC_sV_{off}, \\ n_1 &= -R(C_s r_{Li} V_{off} - L_i D I_{on}), \\ n_0 &= -R(V_{off}(1-D) - r_{Li} D I_{on}). \end{aligned} \tag{4.14}$$

The application of the Routh Hurwitz criterion to the coefficients (4.14) allows to determine that the zeros of G_{vd} are indeed located

in the LHP if the following condition holds:

$$\frac{L_i}{R} < \frac{(1-D)r_{Li}C_s}{D^2} \tag{4.15}$$

Equation (4.15) shows that for a given Cuk converter, there will exist a threshold for the output current I_o *below* which the G_{vd} complex zeros pair location will move from RHP to LHP. It is important to underline that the converter must be running in CCM for the condition (4.15) to be valid.

4.2 PCC-Cuk converter model

As shown in chapter 1, the small signal model of the current modulator is given by:

$$\hat{d} = F_m \left[\hat{v}_c - A_s \hat{i}_L - \frac{\hat{m}_1 D^2 T_s}{2} - \frac{\hat{m}_2 D'^2 T_s}{2} \right]. \tag{4.16}$$

Relevant transfer functions for PCC-Cuk, such as the CTO gain G_{vc} and the closed-current loop input-to-coupling capacitor voltage gain G_{icc} can be obtained by substituting (4.16) in (4.11) - (4.13). A first simplified approach to investigate PCC-Cuk stability is to neglect the low frequency variations between the coupling capacitor voltage and the input and output voltages when substituting the explicit expressions of $\hat{m}_1$ and $\hat{m}_2$ in (4.16), i.e. assuming that $v_s = v_{in} + v_o$. Under this hypothesis, and applying to the small signal model of the Cuk converter the same manipulations used in chapter 2, section 2.2 for the SEPIC, the CTO gain is given by the following equation:

$$G_{vc} = \frac{F_m N_{vd}(s)}{Den(s)(1 + \frac{F_m A_s I_{out}}{1-D}) + F_m N_{vd}(s)(\frac{A_s(1+sRC_o)}{R} + F_v')}. \tag{4.17}$$

Equation (4.17) is formally identical to the CTO gain (2.40) given for the PCC-SEPIC converter in chapter 2. Coefficients F_m and

F_v' are also identical to the ones found for the SEPIC converter. An important difference in the study of the stability between the PCC-SEPIC and PCC-Cuk converters is that it is not possible to give a simplified sufficient stability condition for the Cuk similar to (2.35). The only way to give such an approximate condition would be to ensure that (4.15) holds for all load conditions. However, condition (4.15) depends on the parasitic resistance of the input inductor, and hence may be a too unreliable stability boundary. This is due to the fact that other losses of the converter were not considered, and that the DCR of the input inductor may be unknown or uncertain.
A more useful approximated analytical boundary for PCC-Cuk stability can be obtained by removing the hypothesis $v_s = v_{in} + v_{out}$. The current controller model then becomes:

$$\hat{d} = \frac{1}{M_a T_s}\left[\hat{v}_c - A_s\hat{i}_L - F_i\hat{v}_{in} - F_s\hat{v}_s - F_v\hat{v}_{out}\right] \tag{4.18}$$

where:

$$\begin{aligned} F_i &= \frac{A_s}{2f_s}\left(\frac{D^2}{L_i} - \frac{D'^2}{L_i}\right), \\ F_s &= \frac{A_s}{2f_s}\left(\frac{D'^2}{L_i} + \frac{D^2}{L_o}\right), \\ F_v &= \frac{A_s}{2f_s}\left(\frac{D'^2}{L_o} - \frac{D^2}{L_o}\right). \end{aligned} \tag{4.19}$$

Notice that coefficients F_i and F_s are identical to the ones found for the PCC-SEPIC in chapter 2, subsection 2.2.1.
Although any of the closed current loop transfer function could be used to investigate the converter stability, it is useful to refer to the closed current loop input-to-coupling capacitor gain G_{icc}. Under the hypothesis that the output voltage variations do not influence the coupling capacitor voltage during a line transient, and neglecting all parasitics, the simplified lossless small signal linear circuit shown in Fig. 4.4 can be used to derive a reduced-order expression for G_{icc}. Neglecting the output voltage variations v_o

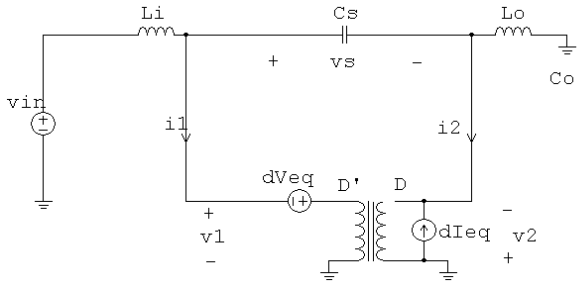

Figure 4.4 Reduced order small signal linear circuit of PCC-Cuk converter

imply that coefficient F_v has no impact on the current controller model given in (4.18). Hence, as the lossless small signal linear model of the switching cell is identical between PCC-SEPIC and PCC-Cuk, the reduced-order $G_{icc}(s)$ gain is also identical for both converters. Approximated analytical conditions for PCC-Cuk converter in terms of the current modulator gain F_m, of the coupling capacitor C_s and of the output to input inductances ratio L_r can be derived for a lossless PCC-Cuk converter. Such conditions are identical to the ones derived for the PCC-SEPIC in chapter 3, and are summarized in Table 4.1.

Table 4.1 Stability conditions for PCC-Cuk converter current loop

$L_r > M$		
$C_{s_{min}} < C_s < C_{s_{min}}/\alpha$	$F_{m_{crit}} > 0$	stable if $F_m > F_{m_{crit}}$
$C_s > C_{s_{min}}/\alpha$	$F_{m_{crit}} < 0$	stable ($F_m > 0$)
$L_r < M$		
$C_{s_{min}} < C_s < C_{s_{min}}/\alpha$	$F_{m_{crit}} < 0$	unstable ($F_m > 0$)
$C_s > C_{s_{min}}/\alpha$	$F_{m_{crit}} > 0$	stable if $0 < F_m < F_{m_{crit}}$

Where:

$$C_{s_{min}} = \frac{F_s L_{eq} I_{out}}{A_s V_{in}}, \tag{4.20}$$

$$F_{m_{crit}} = \frac{(\frac{V_{off}}{V_{in}})^2 \frac{1}{1+L_r} \frac{1}{1-\frac{Cs_{min}}{C_s}} - 1 - \frac{M^2}{L_r}}{\frac{V_{off}^2}{V_{in}}(\frac{A_s I_{out}}{V_{in}} + F_s)(1 - \frac{M}{L_r})}, \tag{4.21}$$

$$\alpha = 1 - \frac{(\frac{V_{off}}{V_{in}})^2}{(1+L_r)(1+\frac{M^2}{L_r})}.$$

As an example, consider a PCC-Cuk with the following specifications: $V_{in_{min}} = 4V$, $V_{in_{max}} = 24V$, $V_{out} = 5V$, $I_{out} = 1A$, $f_s = 100kHz$. Let be $L_i = 56\mu H$ and $L_o = 150\mu H$ to satisfy some given constraint on input and output inductors current ripple. Note that $C_{s_{min}} = 0.3\mu F$ and $L_r = 2.67$, while the maximum M value is 1.25. Hence, $F_{m_{crit}}$ is a lower boundary for F_m. In Fig. 4.5 the stability boundary according to table 4.1 is plotted in red. As a comparison, the stability region numerically calculated using a full order small signal model that includes losses is highlighted in dark green. Fig. 4.6 - 4.8 show PSIM®simulations corresponding

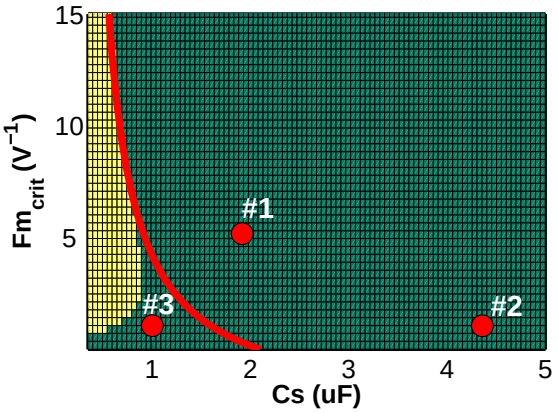

Figure 4.5 PCC-Cuk numerically evaluated stability region (dark green area) and approximated stability boundary (red curve) as a function of F_m and C_s. $L_r > M$.

to couples of F_m and C_s values marked with a red circle in Fig. 4.5 and labelled as #1, #2 and #3. All parasitics are neglected. The results of simulations confirm that the system is unstable if

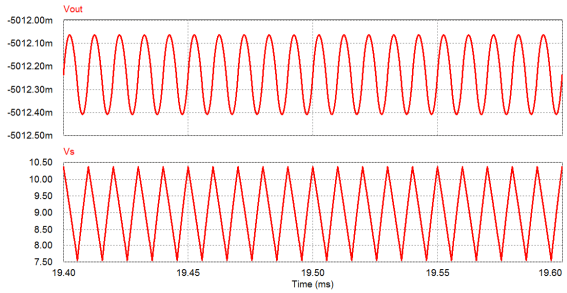

Figure 4.6 V_o, V_s. $C_s = 2\mu F, F_m = 5V^{-1}$ (#1).
$V_{in} = 4V, L_i = 56\mu H, L_o = 150\mu H$. Parasitics elements are neglected.

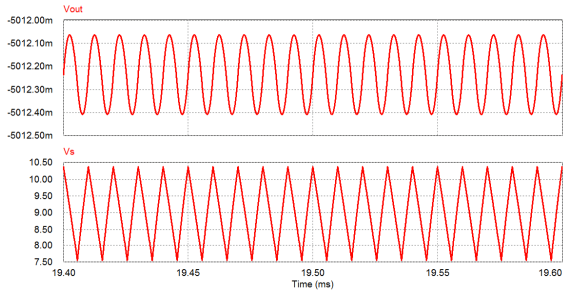

Figure 4.7 V_o, V_s. $C_s = 4.4\mu F, F_m = 1V^{-1}$ (#2).
$V_{in} = 4V, L_i = 56\mu H, L_o = 150\mu H$. Parasitics elements are neglected.

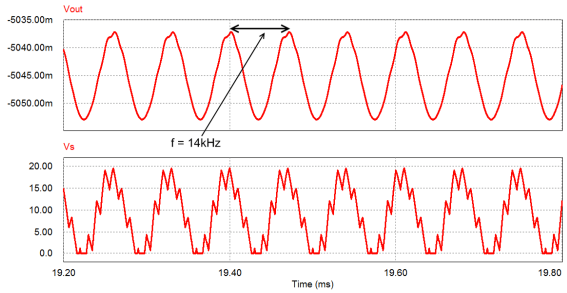

Figure 4.8 V_o, V_s. $C_s = 1\mu F, F_m = 1V^{-1}$ (#3).
$V_{in} = 4V, L_i = 56\mu H, L_o = 150\mu H$. Parasitics elements are neglected.

the couple of values #3 is used for F_m and C_s. The impact of losses on the stability predictions obtained using the proposed approximated model is similar to the one discussed for PCC-SEPIC. In Fig. 4.9, a PSIM®simulation that include parasitics elements using the couple of values #3 for F_m and C_s is shown. As predicted by the complete small signal model, the system is stable. Fig. 4.10 shows the approximated stability boundary for a Cuk

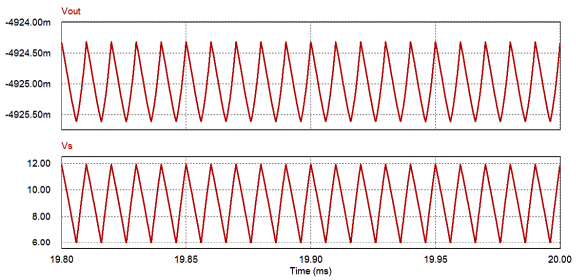

Figure 4.9 V_o, V_s. $C_s = 1\mu F, F_m = 1V^{-1}$ (#3). $V_{in} = 4V, L_i = 56\mu H, L_o = 150\mu H$

converter designed to meet the same specifications of the previous example and operated at $V_{in} = V_{in_{min}}$, with $L_i = 56\mu H$ and $L_o = 47\mu H$. The dark green area is the stability region obtained using a complete small signal model that includes losses. Note that $L_r = 0.83$, hence according to table 4.1 $F_{m_{crit}}$ is an upper boundary for F_m if $V_{in} = V_{in_{min}}$. Fig. 4.11 shows the results of PSIM®simulations of the proposed converter including resistive losses for the couple $F_m = 5V^{-1}, C_s = 15\mu F$ marked by the red circle in Fig. 4.10. Results of simulations when parasitics elements are neglected are shown in Fig. 4.12. The stability predictions obtained using the reduced-order model may result in a too conservative estimation of the real stability boundary of the Cuk converter, especially when $L_r < M$. However, they provide a valuable alert when designing high efficiency systems. Indeed, as highlighted when discussing SEPIC stability, to depend too heavily on the stabilizing effect of the power components losses may result in unreliable design solutions.

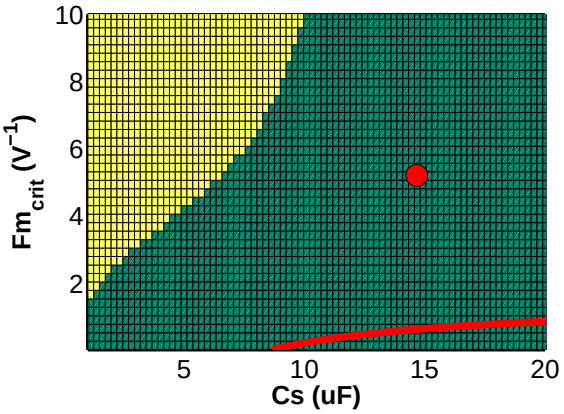

Figure 4.10 PCC-Cuk numerically evaluated stability region (dark green area) and approximated stability boundary (red curve) as a function of F_m and C_s. $L_r < M$.

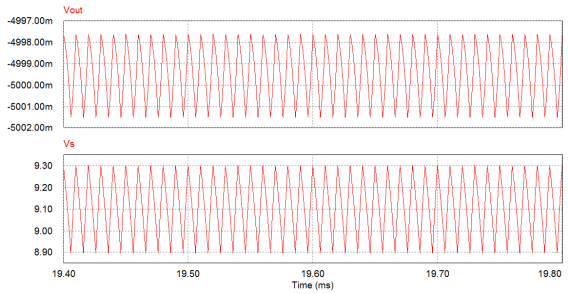

Figure 4.11 V_o, V_s.
$C_s = 15\mu F, F_m = 5V^{-1}, V_{in} = 4V, L_i = 56\mu H, L_o = 47\mu H$

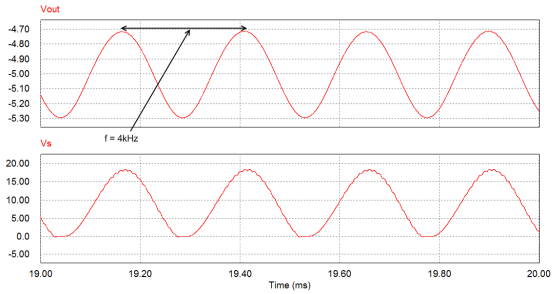

Figure 4.12 V_o, V_s.
$C_s = 15\mu F, F_m = 5V^{-1}, V_{in} = 4V, L_i = 56\mu H, L_o = 47\mu H$. Parasitics elements are neglected.

Chapter 5

Experimental Validations

Three PCC-SEPIC and two PCC-Cuk have been realized and tested, using a National Semiconductor Corporation LM3478 peak current mode controller IC. The first SEPIC prototype, #1 in the following, was realized selecting C_s and F_m according to the stability predictions obtained using the reduced order small signal model discussed in chapter 3, section 3.1. In order to validate the results obtained through the use of the full order small signal model shown in chapter 3, the second SEPIC prototype - #2 in the following - was realized selecting the input and output inductors according to the results shown in section 3.2. Combinations of inductances δ and ϵ were used (see table 3.2). The third SEPIC prototype - #3 in the following - shows the additional damping branch technique described in chapter 3, section 3.3. The two PCC-Cuk prototypes were realized selecting C_s and F_m according to the stability predictions obtained from the reduced order small signal model shown in chapter 4. Details of the power stage components are given in tables 5.2, 5.4, 5.5, 5.6, 5.9 and 5.11. The external voltage feedback was closed, since the LM3478 IC does not provide an easy way to operate the converter with the current loop closed and the voltage loop open. Hence, a compensation network has been designed to guarantee the stability of the voltage loop. Fig. 5.1 shows the simplified schematic of the IC voltage control stage. The values of the compensation network

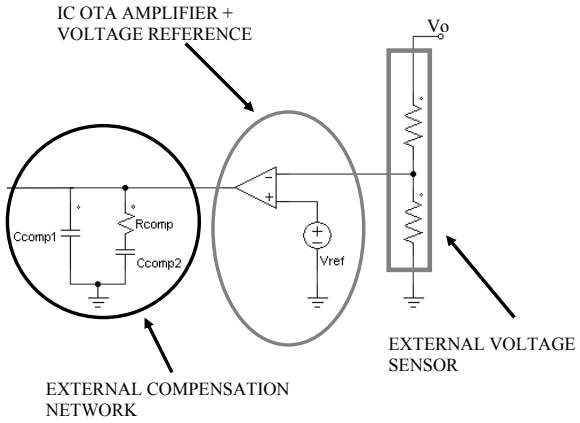

Figure 5.1 external voltage feedback loop

components are listed in table 5.3 for PCC-SEPIC converter #1 and in table 5.7 for #2 and #3. The values of the compensation network components for the two PCC-Cuk converters are listed in table 5.10 and 5.12

5.1 PCC SEPIC #1

The couples of C_s and F_m values used in the experimental validations are listed in table 5.1. They correspond to the solutions labelled as #4, #5 and #6 in Fig. 3.2, chapter 3, section 3.1. The steady state output voltage ripple of the converter is shown in Fig. 5.2, Fig. 5.3 and Fig. 5.4. Stable behavior can be observed in Fig. 5.2 and Fig. 5.3, while a low frequency oscillation (13.7 kHz) is evident in Fig. 5.4. These results closely match the results of PSIM simulations shown in chapter 3. High frequency oscillations in Fig. 5.2 and Fig. 5.3 do not represent an instability phenomenon as they are due to the interaction between the ceramic capacitor placed on the output and the capacitors and PCB stray inductances.

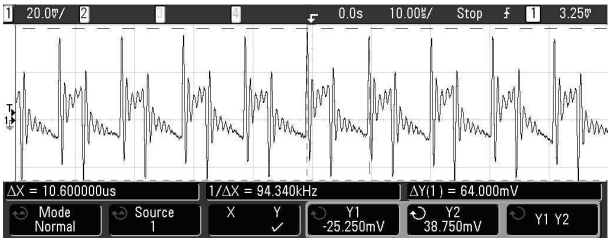

Figure 5.2 Solution #4, output voltage ripple.

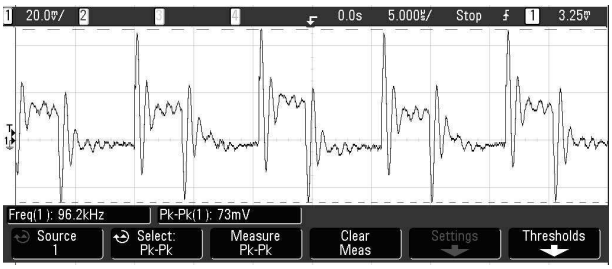

Figure 5.3 Solution #6, output voltage ripple.

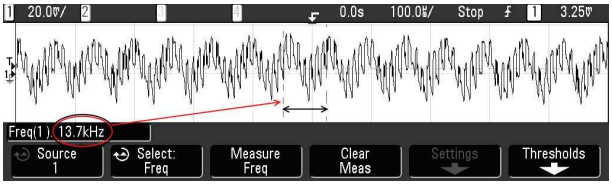

Figure 5.4 Solution #5, output voltage ripple.

Table 5.1 couples of F_m and C_s values used for validations

$F_m = 5V^{-1}, C_s = 4.4\mu F$	#4, inside region B
$F_m = 5V^{-1}, C_s = 1\mu F$	#5, boundary between region A and region C
$F_m = 10V^{-1}, C_s = 2.2\mu F$	#6, inside region A

Table 5.2 PCC-SEPIC #1, power stage components.

MOSFET	Vishay Si4840DY
DIODE	OnSemiconductor MBRS260T3G
Output Capacitor	2X Sanyo 16SVPC270M in parallel, 270μF equivalent capacitance 540μF
Ceramic Output Capacitor	TDK C5750X5R1H106M 10μF
Input capacitor	TDK C4532X7R1E106K, 10μF
Coupling Capacitor	2X TDK C4532X7R1H225K, 2.2μF equivalent capacitance 4.4μF TDK C4532X7R1H225K, 2.2μF C4532X7R2A105M , 1μF
Input Inductor	Coilcraft MSS1260-563, 56μH
Output Inductor	Coilcraft DO5022P-154, 150μH
Sensing Resistor	WSL-2512 0.025, 25$m\Omega$

Table 5.3 PCC-SEPIC #1, compensation network components values

R_{comp}	$1.4k\Omega$
C_{comp1}	$470nF$
C_{comp2}	$3.3nF$

5.2 PCC SEPIC #2

The Bode plot of the CTO gain obtained at minimum input voltage and maximum load for a PCC-SEPIC realized using inductance combination δ (see table 3.2, chapter 3, section 3.2) is shown in Fig. 5.5. The slight difference in the resonance peak between measurements and the developed model is most likely due to the presence of uncertain parasitics elements, which tend to increase the damping factor [47]. The discrepancies located at high frequency are due to the sampling effect of current mode control. Sampling was neglected in the proposed model, as it acts outside the frequency range of interest. To better highlight the impact of the passive components values on the dynamic behavior of the converter, Fig. 5.6 shows the closed loop response of the coupling capacitor voltage to a line transient for two different values of the coupling capacitance. Results are referred to a PCC-SEPIC using inductance combination ϵ. Substantial agreement with PSIM simulated response shown in Fig. 3.23 can be observed.

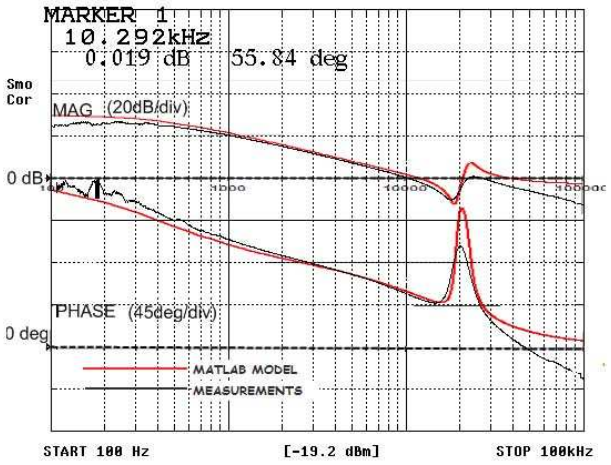

Figure 5.5 PCC-SEPIC #2, CTO gain. Inductance combination δ. $V_{in} = 3V$, $I_{out} = 1.2A$.

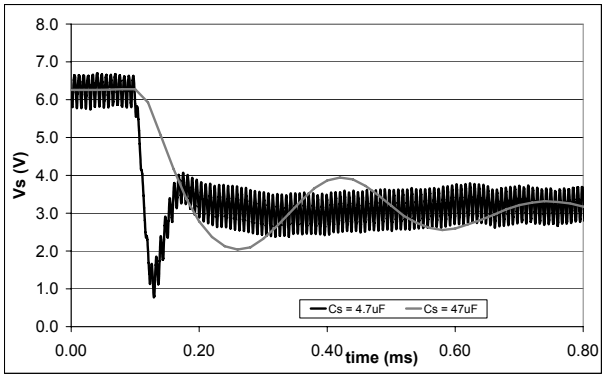

Figure 5.6 PCC-SEPIC #2, closed loop coupling capacitor voltage response to a line transient. Inductance combination ϵ. $C_s = 4.7\mu F$ (black line),$C_s = 47\mu F$ (gray line). $V_{in_{max}} = 6V, V_{in_{min}} = 3V, I_{out} = 1.2A$.

Table 5.4 PCC-SEPIC #2, power stage components.

MOSFET	Vishay Si4686DY
DIODE	OnSemiconductor MBRS260T3G
Output Capacitor	Sanyo 16SVPC270M, $270\mu F$
Input Capacitor	TDK C4532X7R1E106K, $10\mu F$
Coupling Capacitor	TDK C4532X7R1H225K, $2.2\mu F$
Input Inductor	Coilcraft DO3316T, $6.8\mu H$
Output Inductor	Coilcraft DO5022P, $22\mu H$
Sensing Resistor	WSL1206R015, $15m\Omega$

Table 5.5 PCC-SEPIC #2, alternate power stage components.

Coupling Capacitor	TDK C4532X7R1H475K, $4.7\mu F$
Coupling Capacitor	TDK C4532X7R1H476K, $47\mu F$
Output Inductor	Coilcraft DO5022P, $47\mu H$

5.3 PCC SEPIC #3

Fig. 5.7 shows the measured CTO of the converter, obtained at minimum input voltage and maximum load Values of the damping branch components are $R_d = 3.3\Omega$ and $C_d = 15\mu F$. From Fig. 3.25 shown in chapter 3, section 3.3, the corresponding damping factor of the dominant complex pole pair of G_{icc} is around 0.3. To underline the impact of the R_d - C_d values on the inductor

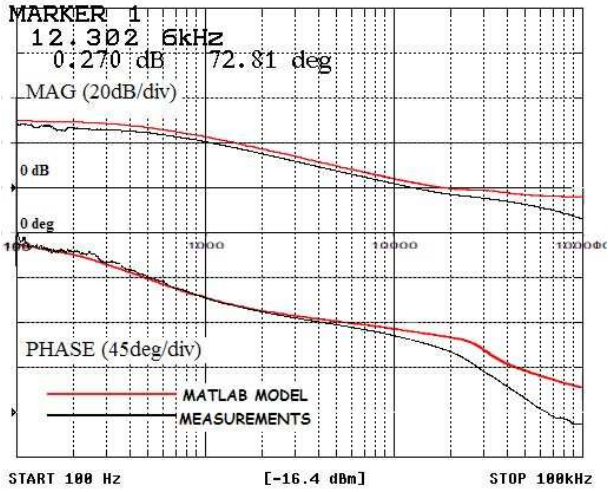

Figure 5.7 PCC-SEPIC #3, CTO gain. $V_{in} = 3V$, $I_{out} = 1.2A$.

current during transients, the closed loop transient response of the output inductor current due to an input voltage change from $V_{in} = 6.5V$ to $V_{in} = 3V$ are shown in Fig. 5.8 and in Fig. 5.9. Fig. 5.8 refers to the damping solution obtained using $R_d = 3.3\Omega$ and $C_d = 15\mu F$, while Fig. 5.9 refers to the damping solution obtained using $R_d = 0.650\Omega$ and $C_d = 15\mu F$. Fig. 5.10 shows a comparison between the G_{iLo} obtained only with the current loop closed and the G_{iLo} obtained with current and voltage loops closed. It is clear that the two gains are similar near the resonant frequency of the converter. Indeed, although measurements were taken with both inner current loop and output voltage loop closed, the results are coherent with Table 3.5 and with the time domain simulations of Fig. 3.26 and Fig. 3.27, referred to solutions **b** and **c** in table 3.4.

The damping branch using $R_d = 3.3\Omega$ allows for a faster response and a lower peak of the inductor current.

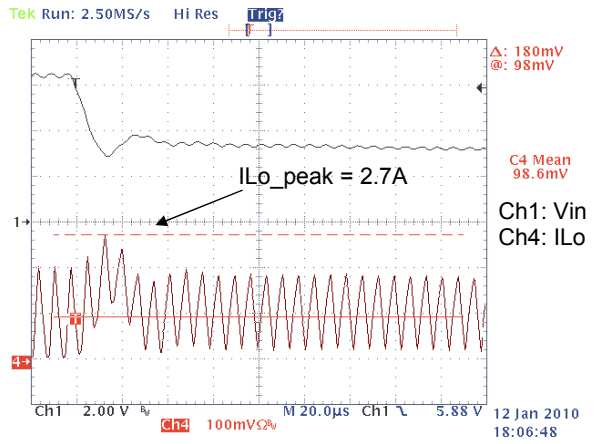

Figure 5.8 PCC-SEPIC #3, closed loop response of the output inductor current to a line transient. $R_d = 3300m\Omega$, $C_d = 15\mu F$, $V_{in_{max}} = 6.5V$, $V_{in_{min}} = 3V$, $I_{out} = 1A$.

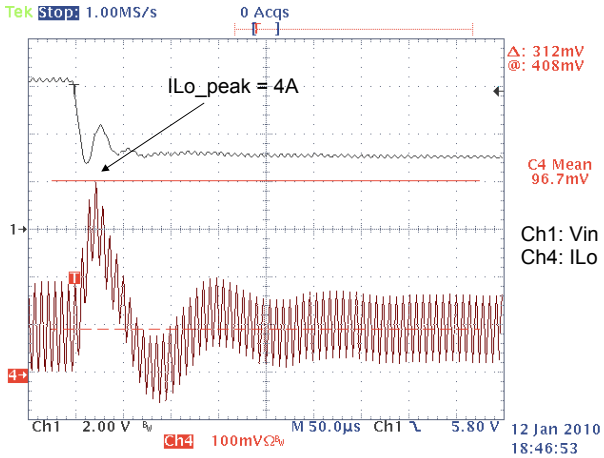

Figure 5.9 PCC-SEPIC #3, closed loop response of the output inductor current to a line transient. $R_d = 650m\Omega$, $C_d = 15\mu F$, $V_{in_{max}} = 6.5V$, $V_{in_{min}} = 3V$, $I_{out} = 1A$.

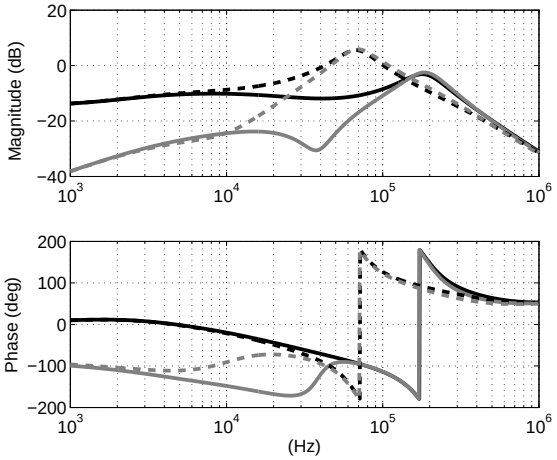

Figure 5.10 PCC-SEPIC #3, Comparisons between MATLAB generated G_{iLo} with closed current loop (black curve) and with current and voltage loops closed (gray curve). $R_d = 3300m\Omega$, $C_d = 15\mu F$(solid curves).$R_d = 600m\Omega$, $C_d = 15\mu F$(dashed curves). $V_{in} = 3V$, $I_{out} = 1.2A$.

Table 5.6 PCC-SEPIC #3, power stage components.

MOSFET	Vishay Si4686DY
DIODE	OnSemiconductor MBRS260T3G
Output Capacitor	Sanyo 16SVPC270M, $270\mu F$
Input Capacitor	TDK C4532X7R1E106K, $10\mu F$
Coupling Capacitor	TDK C4532X7R1H225K, $2.2\mu F$
Input Inductor	Coilcraft DO3316T, $6.8\mu H$
Output Inductor	Coilcraft DO3316T, $6.8\mu H$
Damping Capacitor	$15\mu F, ESR = 0.6\Omega$ @ 100kHz
External Damping Resistance	2.7Ω
Sensing Resistor	WSL1206R015, $15m\Omega$

Table 5.7 PCC SEPIC #2 and #3, compensation network components values

R_{comp}	$1.1k\Omega$
C_{comp1}	$2.2nF$
C_{comp2}	$220nF$

5.4 PCC Cuk #1

The couples of C_s and F_m values used in the experimental validations of the PCC-Cuk example discussed in chapter 4, section 4.2 are listed in table 5.8. The steady state output voltage ripple of the converter is shown in Fig. 5.11 and Fig. 5.12. As the voltage ripple is only $10mV$, the switching node voltage is also shown to make accurate measurements of the switching frequency. Stable behavior can be observed. This result is in agreement with the predictions based on the lossless reduced-order model discussed in chapter 4. Note that the output voltage ripple is much smaller than the one measured for the PCC-SEPIC #1, although the switching frequency and the power stage passive components are the same. This happens because the output inductor is directly connected to the load, and hence the current ripple in the output capacitors is much smaller with respect to the SEPIC prototype. This may allow for a reduction of the output capacitors number and size [63].

Table 5.8 couples of F_m and C_s values used for validations

$F_m = 10V^{-1}$	$C_s = 4.4\mu F$
$F_m = 10V^{-1}$	$C_s = 2.2\mu F$

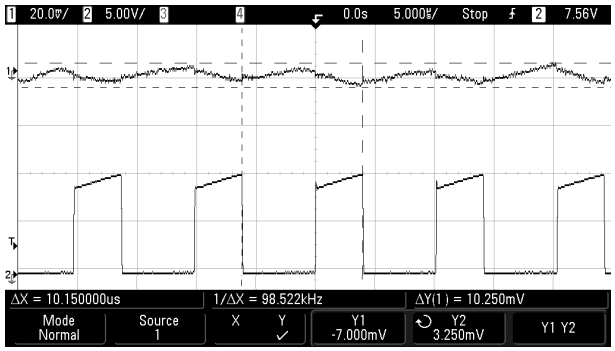

Figure 5.11 PCC-Cuk #1, $C_s = 4.4\mu F, F_m = 10V^{-1}$. Channel 1: output voltage ripple, Channel 2: switching node voltage.

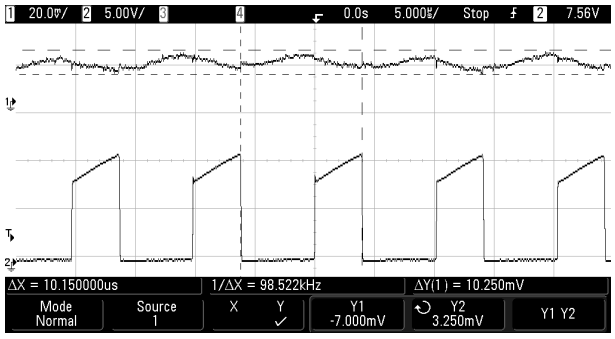

Figure 5.12 PCC-Cuk #1, $C_s = 2.2\mu F, F_m = 10V^{-1}$. Channel 1: output voltage ripple, Channel 2: switching node voltage.

Table 5.9 PCC Cuk #1, Power stage components

MOSFET	Vishay Si4840DY
DIODE	OnSemiconductor MBRS260T3G
Output Capacitor	2X Sanyo 16SVPC270M in parallel, 270μF equivalent capacitance 540μF
Input capacitor	TDK C4532X7R1E106K, 10μF
Coupling Capacitor	2X TDK C4532X7R1H225K, 2.2μF equivalent capacitance 4.4μF
	TDK C4532X7R1H225K, 2.2μF
Input Inductor	Coilcraft MSS1260-563, 56μH
Output Inductor	Coilcraft DO5022P-154, 150μH
Sensing Resistor	WSL-2512 0.025, 25$m\Omega$

Table 5.10 PCC Cuk #1, compensation network components values

R_{comp}	1.4$k\Omega$
C_{comp1}	470nF
C_{comp2}	3.3nF

5.5 PCC Cuk #2

Input and output specifications of the second Cuk prototype are as follows: $V_{in} = 4V, V_{out} = 5V, I_{out} = 1.5A$. The switching frequency is 100kHz, the input inductance L_i is $56\mu H$, the output inductance L_o is $150\mu H$ and the output capacitance C_o is $540\mu F$. Note that $L_r = 2.67 > M$. In Fig. 5.13, the approximated stability boundary and the numerical evaluated stability region (including losses) are shown: The red dots mark the couples of C_s and F_m values

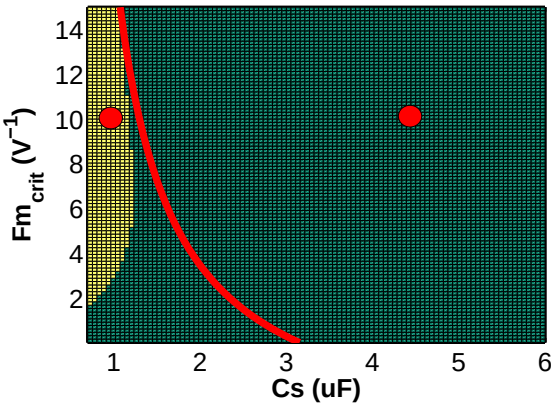

Figure 5.13 PCC-Cuk #2 numerically evaluated stability region (dark green area) and approximated stability boundary (red curve) as a function of F_m and C_s. $L_r > M$.

used in the validations. In Fig. 5.14, the measured output voltage ripple and the switching node voltage are shown for the converter realized using $C_s = 4.4\mu F$ and $F_m = 10V^{-1}$. Stable behavior can be observed. In Fig. 5.15 and Fig. 5.16, the measured output voltage ripple and the coupling capacitor voltage of the converter realized using $C_s = 1\mu F$ and $F_m = 10V^{-1}$ are shown respectively. The switching node voltage is also shown. The low frequency oscillation (12.3 kHz) clearly indicates that the converter is unstable. These results are in agreement with the prediction based on the approximated stability boundary discussed in chapter 4.

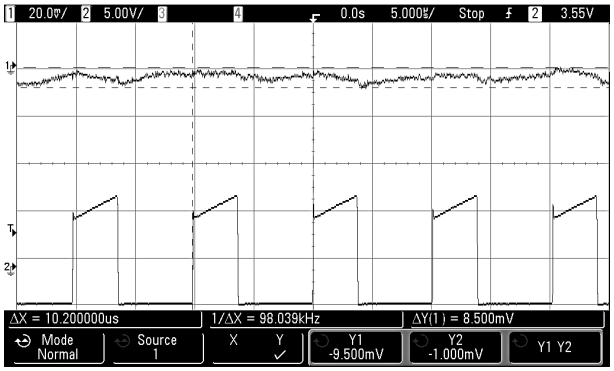

Figure 5.14 PCC-Cuk #2, $C_s = 4.4\mu F, F_m = 10V^{-1}$. Channel 1: output voltage ripple, Channel 2: switching node voltage.

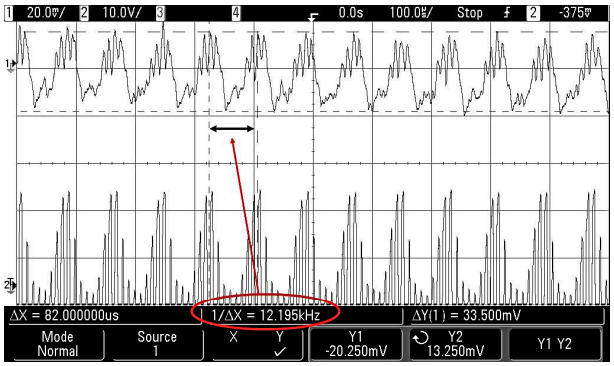

Figure 5.15 PCC-Cuk #2, $C_s = 1\mu F, F_m = 10V^{-1}$. Channel 1: output voltage ripple, Channel 2: switching node voltage.

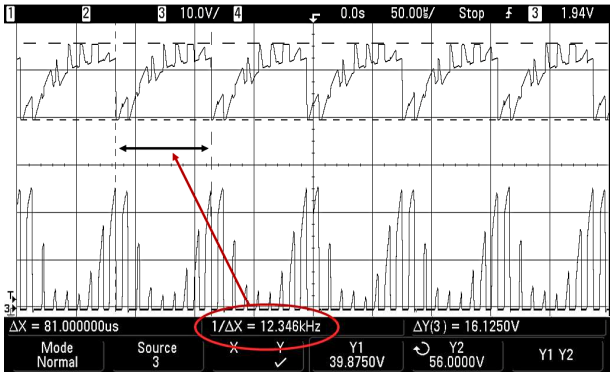

Figure 5.16 PCC-Cuk #2, $C_s = 1\mu F, F_m = 10V^{-1}$. Channel 1: coupling capacitor voltage, Channel 2: switching node voltage.

Table 5.11 PCC Cuk #2, Power stage components

MOSFET	Vishay Si4840DY
DIODE	OnSemiconductor MBRS260T3G
Output Capacitor	2X Sanyo 16SVPC270M in parallel, $270\mu F$ equivalent capacitance $540\mu F$
Input capacitor	TDK C4532X7R1E106K, $10\mu F$
Coupling Capacitor	2X TDK C4532X7R1H225K, $2.2\mu F$ equivalent capacitance $4.4\mu F$ TDK C4532X7R1H105K, $1\mu F$
Input Inductor	Coilcraft MSS1260-563, $56\mu H$
Output Inductor	Coilcraft DO5022P-154, $150\mu H$
Sensing Resistor	WSL-2512 0.01, $10m\Omega$

Table 5.12 PCC Cuk #2, compensation network components values

R_{comp}	470Ω
C_{comp1}	$1.4\mu F$
C_{comp2}	$3.3nF$

Conclusions

In this dissertation, the stability properties of fourth order peak-current-controlled (PCC) step up/down SEPIC and Cuk DC/DC converters are investigated. The simplifying assumptions usually found in literature when deriving the current controller model are discussed, and a refined small signal model is proposed. Its use allows to highlight the unreliability of stability predictions when traditional small signal models of the current controller are applied to PCC-SEPIC and PCC-Cuk.

Taking the proposed model as a starting point, stability conditions are derived for both converters. Through an appropriate reduced-order lossless model, closed-form analytical stability boundaries are derived, which unveil the joint impact of power stage passive components and of the current modulator gain on stability. In particular, a minimum value for the coupling capacitance is identified, and a boundary curve that relates the value of the current modulator gain to the coupling capacitance is derived. Such boundary curve may represent either a lower or an upper boundary for the current modulator gain, depending on the ratio between the output and input inductances values. To validate and critically evaluate the results obtained with the use of the proposed reduced-order model, a full-order model of both converters is derived using the SSA technique and including resistive losses of the power stage components. The use of a numerical procedure based on the Routh-Hurwitz criterion highlights that the stability boundaries based on the reduced-order model may be too conservative, as the beneficial influence of the losses in damping the system oscillations are neglected. However, such boundaries pro-

vide a valuable alert when designing high efficiency systems. These results lead to conclude that only numerical calculations of poles of the control-to-output gain can provide solution to the search of the proper compromise among parameters of passive components required to guarantee the current loop stability.
With particular reference to PCC-SEPIC, the use of the complete small signal model, including losses, leads to the determination of reliable stability predictions as a function of input and output inductances, coupling capacitance and current modulator gain values. The importance of the coupling capacitor value in ensuring both stability and adequate dynamic response in presence of line transients events is investigated. It is highlighted that good dynamic performances can be obtained either by proper selection of input and output inductances in relation to the coupling capacitor value or through the use of a damping technique based on an additional resistive-capacitive (R-C) branch placed in parallel to the coupling capacitance. This additional damping branch allows to mitigate the constraints on input and output inductances values imposed by stability considerations. The numerical results obtained allow to give some design guidelines for proper sizing of passive components and for the use of the additional damping branch technique. If pure *inductive damping* is adopted, i.e., if no additional damping branch is included in the circuit, the ratio between output and input inductances must be sufficiently higher than voltage conversion ratio. This guarantees both stability and adequate damping of the voltage oscillations across the coupling capacitor due to line transients events. Increasing the coupling capacitance value may help preventing the oversize of the output inductor to guarantee stability in high voltage ratio applications. However, there exist a maximum for the coupling capacitance value above which the damping of the oscillations of the voltage across the coupling capacitor decreases. The use of the additional R-C damping branch can help in those applications where the inductance ratio needed to achieve the required damping is too big. When using the damping branch, solutions to prefer for its components are the ones that ensure lowest sensitivity to

parametric changes, lowest current peaks in the inductors during line transients and lowest dissipation in the damping resistance. Simulations and experimental verifications confirm the validity of the results.

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