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ABSTRACT
TESI DI DOTTORATO

Analysis and Design of 4H-SiC Bipolar Mode Field Effect Power Transistor (BMFET)

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Analysis and design of a new Silicon Carbide polytype 4H (4H-SiC) bipolar power transistor are the main topics of this Ph.D. thesis. The device is the Bipolar Mode Field Effect Transistor (BMFET) and exploits the electric field due to the channel punching-through in order to have a *normally-off* behavior and the minority carrier injection from the gate regions into the channel in order to obtain the channel conductivity modulation. The structure of the transistor is oxide-free and its advantages are due to the lower conduction resistance, to the higher output current density and blocking voltage and to the elevated switching frequency, which make it competitive with commercial 4H-SiC Junction Field Effect Transistors or Bipolar Junction Transistors.

These activities, which have been completed with the definition of the main process steps and of the mask layouts, are supported by a technology activity and by an intense modeling activity of BMFET electrical characteristics, which has been validated by comparisons with the results of numerical simulator (ATLAS Silvaco) and the measures of commercial devices having a similar structure, like Vertical-JFETs.

In the former activity, in order to obtain an integrated free-wheeling diode in anti-parallel configuration to BMFET, an original 4H-SiC Schottky rectifier has been fabricated; precisely, for the first time in the literature, DiVanadium PentOxide (V_2O_5), a Transition Metal Oxide, has been used as anode contact of the rectifier. The device is a heterojunction between a thin V_2O_5 layer, which is thermally evaporated and has a thickness of around $5nm$, and a 4H-SiC *n*-type low doped epilayer. By analyzing the J_D-V_D and C_D-V_D curves, the structure has a rectifier behavior with a high/low current ratio higher than seven order of magnitude and its transport mechanism is described by the thermionic emission theory characterized by a Schottky barrier height and an ideality factor between $0.78eV$ and $0.85eV$ and between 1.025 and 1.06 , respectively, at $T=298K$.

Because the gate doping concentration greatly influences the BMFET performances, as input resistance, DC current gain and blocking voltage, Aluminum ion implantation process, used to realize the Gate regions, is strongly analyzed in terms of the dose concentrations and of the annealing temperature. It will show as the necessity of a low BMFET on-resistance, which is possible with highly conductive gate regions in order to permit high injection levels of the minority carriers, is counteracted by the Aluminum incomplete ionization in 4H-SiC. This phenomenon together with the band-gap narrowing effect limits the hole carrier density from gate to channel. The analysis, in collaboration with the Institute for the Microelectronics and Microsystems (IMM) of CNR in Bologna, Italy, consists to reveal the effects of various different doses at different temperature annealing ($1920K$ and $2170K$) on the gate injection efficiency and on the input current density.

Since the introduction of the first normally-off Si JFET in '80 years, the description of the potential barrier height into the channel has been unresolved due to the complex relations with the channel geometry and bias conditions. In the second activity an analytical model of the potential barrier height in the channel is proposed and compared with the numerical simulation results by changing the channel length and width, respectively in the range $0.1\div 6\mu m$ e $0.5\div 3\mu m$, the channel doping concentration, between $10^{14}\div 10^{17}cm^{-3}$, and the output and input bias voltages. Moreover, it has been also validated by using Silicon as semiconductor material, permitting to extend it to other devices with similar structures, like BSITs, VJFETs and SITs. From a further improvement of this model, another has been developed, which is able to describe the trans-characteristics of the transistor both in sub-threshold condition and in unipolar conduction, and the comparisons with numerical simulations and experimental data validated the results.

Finally, the analysis of the input diode during the switching-off has been performed because the switching capability of the BMFET depends on the storage charge into the channel during the "on" state. The result is the development of an analytical model that describes the spatial distributions of the electric field, of the minority carrier concentration and of the carrier current densities into the epilayer at each instant during the switching, in addition obviously to the current and voltage transients. It is shown as the combination of this model with another static model just developed in a previous Ph.D. thesis is an useful instrument to understand how physical parameters, which are

dependent on the manufacturing processes, as carrier life-time and doping concentrations, can affect the dynamic behavior.