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Models and methods for the design of isolated power converters in high-frequency high-efficiency applications

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Isolated power supplies design requires the achievement of overall stress, losses, cost, size and reliability trade-off. This problem is of considerable importance in modern applications of power converters, as for energy saving issues as for the achievement of high power density capabilities needed to integrate the power supply into the same boards where the system they feed is hosted.

The aim of this PhD dissertation is to discuss the fundamental issues regarding the design of high-efficiency high-power-density isolated power converters, related to the transformers design and to the system-level analysis of functional and parametric correlations existing among transformers and silicon devices in the achievement of high efficiency.

Transformer design is the central issue in isolated switching power supplies design. Affording a preliminary reliable investigation of possible feasible power supply designs using off-the-shelf transformers can be of great help in reducing the time to prototyping and the time-to-market. Even though many off-the-shelf transformers are available today for standard applications, many special situations occur such that the design of a custom transformer is required. New design method are needed in order to enable a wider detection and investigation of possible transformer design solutions by means of a straightforward matching between the available magnetic cores, the operating conditions of the transformer to be designed and the design constraints to be fulfilled.

A critical re-examination of transformers design methods discussed in technical literature has been afforded to highlighting some common misleading assumptions which can hinder the minimization of the transformer. Thus, a new design approach has been investigated and discussed, which helps in easily identifying possible transformer solutions in critical custom designs for a given application, complying with losses and size constraints. The new method is aimed at quickly identifying possible combinations of magnetic cores and windings turns number when many possible design might be feasible and a fast comparative evaluation is needed for preliminary cores selection. Novel geometric form factors of magnetic core (K_f and K_c) have been introduced and a consequent classification procedure for magnetic cores has been obtained, showing the correlation between the characteristics of the core and the specific applications in which each type of core offers major advantages in terms of minimizing losses and/or size.

A magneto-electro-thermal macro model of the transformer has been adopted in order to investigate the dependency of total transformer losses on the temperature and to analyze the temperature sensitivity of form factor constraints of magnetic cores for power loss compliance. In particular, temperature-dependent boundaries curves both for the core window area and cross-section and for the form factors Kf and Kc have been obtained, allowing quick identification of feasible design solutions, complying with all design constraints, included thermal issues.

Transformers and silicon devices do inextricably share the responsibility of major losses in isolated power supplies, and the optimization of the former normally impinges the one of the latter. As a consequence, the intimate correlation among these parts need to be jointly considered regarding the way the characteristics of one device influence the losses of the other one. In order to achieve reliable comparative evaluations among different design set-up, a new versatile numerical model for commutations analysis of power MOSFETs has been developed. The model takes into account the non-linear behavior of the inter-electrode capacitances and has been conceived to work as with parameters and information contained in the devices datasheets as with more detailed models. A Modified Forward Euler (MFE) numerical technique has been specifically developed and adopted in the realization of a numerical algorithm which solves the non linear system of differential equations describing the effect of parasitic capacitances in whatever operating conditions, in order to overcome the limitation exhibited by ODEs techniques for stiff problems in this particular application. The new MFE technique allows to compare the switching characteristics of MOSFETs with a good level of reliability and to obtain a detailed analysis of capacitive currents paths circulating between MOSFETs in half-bridge configuration during commutations. The numerical device-level model of the MOSFETs couples has been first tested in the analysis of basic non isolated synchronous rectification buck converter and then used into an integrated model allowing the analysis of Active Clamp Forward converters. It has been also demonstrated that the model adopted for the switching cell can be implemented in circuit simulators like Micro-Cap. The correlations existing between the parasitic parameters which characterize both transformer and MOSFETs and their impact on the switching behavior and the efficiency of such a conversion system can be effectively investigated by using such modeling approach, thus overcoming the limitations and unreliability of simplified analytical formulas for the prediction of the ZVS achievement. In particular, the integrated system model has been successfully used to determine the mutual constraint conditions between magnetic devices and solid state devices to achieve soft-switching, and their effects on the physical feasibility and design/selection of such power devices in order to achieve high efficiency.

Experimental activities have been done to validate the methods and models proposed, through the implementation of *on-line* losses measurements techniques for both magnetic and solid state devices. The high switching frequency, high slew rates, high current and low leakage devices make such measures extremely sensitive to the parasitic circuit layout parameters. In order to achieve reliable measurements, non-conventional measurement techniques have been investigated based on the use of current sensing MOSFETs, and applied in the development and implementation of new measuring circuits.