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TESI DI DOTTORATO

Characterization, Modeling and Simulation of 4H-SiC Power Diodes

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Thank you to everyone,
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Abstract

Exploring the attractive electrical properties of the Silicon Carbide (SiC) for power devices, the characterization and the analysis of 4H-SiC pin diodes is the main topic of this Ph.D. document. In particular, the thesis concerns the development of an auto consistent, analytical, physics based model, created for accurately replicating the power diodes behavior, including both on-state and transient conditions.

At the present, the fabrication of SiC devices with the given performances is not completely obvious because of the lack of knowledge still existing in the physical properties of the material, especially of those related to carrier transport and of their dependences on process parameters. Among these, one can cite the degree of doping activation, the carrier lifetime into epitaxial layers that will be employed and the sensitivity of some physical parameters to temperature changes. Therefore, a set of investigative tools, designed especially for SiC devices, cannot be regarded as secondary objective. It will be useful both for process monitoring, becoming essential to the tuning of technological processes used for the implementation of the final devices, and for a proper diagnostics of the realized devices. Following this need, in our research activity firstly a predictive, static analytical model, including temperature dependence, is developed. It is able to explain the carrier transport in diffused regions as function of the injection level and turns also useful for better understanding the influence of physical parameters, which depend in a significant way from the processed material, on device performances. The model solves the continuity equation in double carrier conditions, taking into account the effects due to varying doping profile of the junction, the spatial dependence of physical parameters on both doping and injection level and the modification of the electric field of the region with the injection regime. The model includes also the device characterization at high temperatures to analyze the influence of

thermal issues on the overall behavior up to temperature of 250°C. The accuracy of the static model has been extensively demonstrated by numerous comparisons with numerical results obtained by the SILVACO commercial simulator.

Secondly, with the aim to properly account for the dynamic electrical behavior of a diode with generic structure, the static model has been incorporated in a more general, self-consistent model, allowing the analysis of the device behavior when it is switched from an arbitrary forward-bias condition. In particular, the attention is focused on an abrupt variation of diode voltage due to an instantaneous interruption of the conduction current: although this situation is notably interesting for the study of the switching behavior of diodes, the voltage transitory is also traditionally used in different techniques of investigation to extract more information about the mean carrier lifetime. This occurs, for example, in the conventional *Open Circuit Voltage Decay* (*OCVD*) technique, where the voltage decay due to the current interruption is useful for an indirect measure of minority carrier lifetime in the epitaxial layer.

Because of its heavy dependence on processes, the carrier lifetime is an important parameter to be monitored, especially in the case of bipolar devices, and it cannot be neglected. Due to the existent uncertainty about this parameter in SiC epi-layers, the OCVD method reveals itself a practical way to overcoming this limit.

In detail, by using our self-consistent model, that exploits an improved method of the traditional OCVD technique, it is possible to characterize the carrier lifetime into 4H-SiC epitaxial layer of a generic diode under test, obtaining the spatial distributions of the minority carrier concentration and carrier lifetime at any injection regime. The overall model performances are compared to both device simulations and experimental results performed on Si and 4H-SiC rectifier structures with various physical and electrical characteristics. From the comparisons, the model results to have good predictive capabilities for describing the spatial–temporal variation of carriers and currents along the whole epi-layer, proving contextually the validity of the used approximations and allowing also to resolve some ambiguities reported in the literature, such as the stated inapplicability of the OCVD method on thick epitaxial layers, the reasons of the

observed non linear decay of the voltage with time, and the effects of junction properties on voltage transient.

Finally, with the imposition of right boundary conditions, it is possible to use the versatility of the developed model for extending the analysis and obtaining a physical insight of any arbitrary switching condition of 4H-SiC power diodes.

Thesis Outline

The thesis is arranged with a general introduction in chapter 1 to the potentiality of wide bandgap semiconductors, such as Gallium Nitride (GaN) and Silicon Carbide (SiC), as attractive materials in the electronic field. At this time, the state of the semiconductor industry is presented to give evidence of how these emerging technologies are expected to shift the theoretical limits for electronic devices even far beyond those of the most advanced Silicon devices.

The second chapter describes the set of electrical and physical characteristics which have relevance to the analysis of power diodes in Silicon Carbide. The attention is focused on the 4H-SiC polytype, because of its superior electrical properties with respect to the others. Along with a brief excursus on the physical models which are today available for this material, the analytical expressions to describe the transport and physical parameters, such as minority carrier lifetimes, mobility, bandgap narrowing and incomplete ionization effects, are also introduced. In order to obtain a suitable description of the main physical phenomenon associated to Silicon Carbide, some of these models were incorporated in our diode model and implemented in the numerical simulator.

Chapters 3 and 4 describe, respectively, the analytical development of our static and dynamic model. Here, with the aim to better highlight the versatility of the resultant auto-consistent model in the investigation of 4H-SiC power diodes with arbitrary structures, comparisons with the numerical and experimental data are presented. The usefulness of the model to predict the electrical behavior of a generic diode is proven at the end of Chapter 4, where the analysis has been extended to other switching conditions, such as reverse recovery transients.

In the last chapter a further research activity is finally presented. It is focused on the design of a new Context-Adaptive Variable Length Coding (CAVLC) encoder architecture, particularly aimed to be implemented with Field Programmable Logics (FPLs) like FPGAs.

Chapter 1

Emerging Wide Bandgap Semiconductors Based Devices

In the last six decades Silicon technology has always dominated the power electronic field, providing semiconductor devices able to operate in a broad spectrum of power levels and frequencies. In detail, as shown in Fig. 1, thyristors are favored for the low frequency and high power applications, IGBTs for the medium frequency and power applications, and MOSFETs are typically restricted to lower power and higher frequency applications [1]. Therefore, Silicon devices are

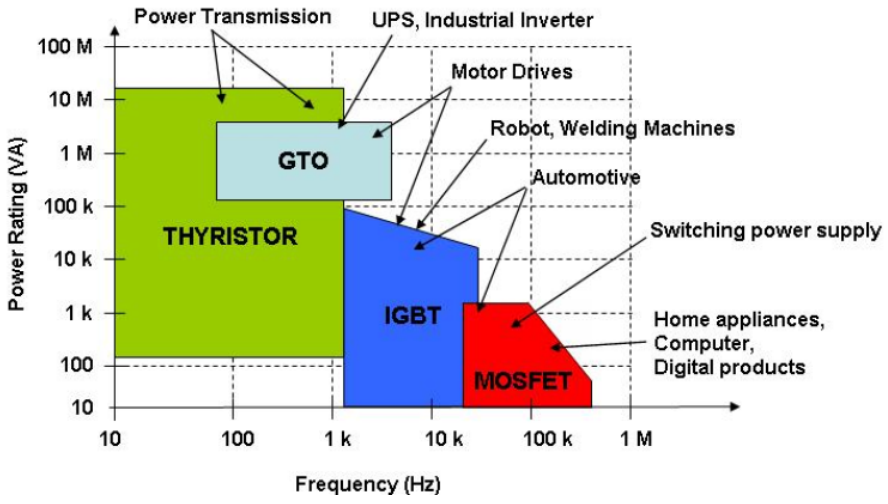


Fig. 1: Applications for power devices [2]

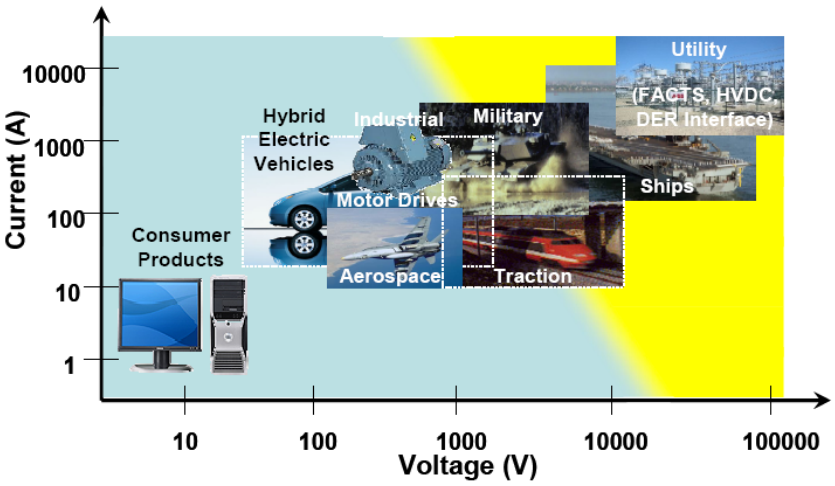


Fig. 2: System ratings for power devices [2]

presently able to serve every type of power application, each characterized by own current and voltage ratings as displayed in Fig. 2, including variable speed motion control, electric vehicle drives, uninterruptible power supplies (UPS), until to the higher power distribution, transmission and traction markets. However, with the aim to guarantee a continue improvement of power systems, the required performance by future devices is destined to increase continuously, so that the theoretical limits related to the devices based on traditional technologies are rapidly approaching. For overcoming the problem, which will make the conventional semiconductors incompetent for potential demands, especially in high power and high efficiency applications, manufacturers are exploring the possibilities of using valid counterparts. Among these, favourite candidates are the wide band gap semiconductors, like Gallium Nitride (GaN) and Silicon Carbide (SiC): compared to Silicon, they exhibit largely better figures for most of the key specifications, such as energy gap, electric field, electron mobility, and melting point, offering intrinsically better performance in terms of breakdown voltage, switching frequency and system efficiency. Thus, these innovative materials, due to their

unique electrical and chemical properties, are becoming very attractive into the electronics field.

At the present, for its direct band-to-band transition, GaN results superior to SiC for optical applications, favouring a well implanted and widely diffused semiconductor technology for ultra-bright blue light emitting diodes and lasers, ultraviolet emitters, and optical detectors [3]. Besides, the high critical field of both GaN and SiC gives a further advantage to these materials compared to Si and GaAs for RF power devices. In particular, SiC shows higher electron mobility than Si but GaN's electron mobility is higher than SiC, so that GaN is the best candidate material for very high frequencies. In this perspective, in the last decades, GaN based devices have been developed for RF wireless applications where they can efficiently replace Silicon transistors [4]. The spread in this field has also opened the doors to the power switching capability in the lower frequency range and thus also in the power electronic applications. Despite owing fundamentally superior electronic properties with respect to SiC, however, GaN must overcome the lack of a native substrate excluding any vertical devices, so that GaN based devices are usually characterized by lateral configurations on Si or SiC substrates. Regardless of the type of application, in the switching or RF field, the most extensively used lateral structure is becoming the High Electron Mobility Transistor (HEMT) [5]. The primary adopters of GaN on SiC HEMTs are defence systems, where performance is paramount and the cost is not the primary factor. Actually, GaN on SiC HEMTs are emerging for use at very high frequencies such as *C*, *X* and *Ku* bands, bringing to the integration of communications systems and multiple radars into a single amplifier [6-7]. Besides, RF GaN on SiC HEMTs are also manufactured [8] to replace the incumbent Si Laterally Diffused MOS (LDMOS) devices and the Pseudomorphic HEMTs (PHEMTs) of Gallium Arsenide, which are extensively used in telecommunication market. For example, since the base stations for Mobile Worldwide Interoperability for Microwave Access (WiMAX) require high power efficiency to drastically reduce the increase of power consumption, high-efficient transmission amplifiers are needed.

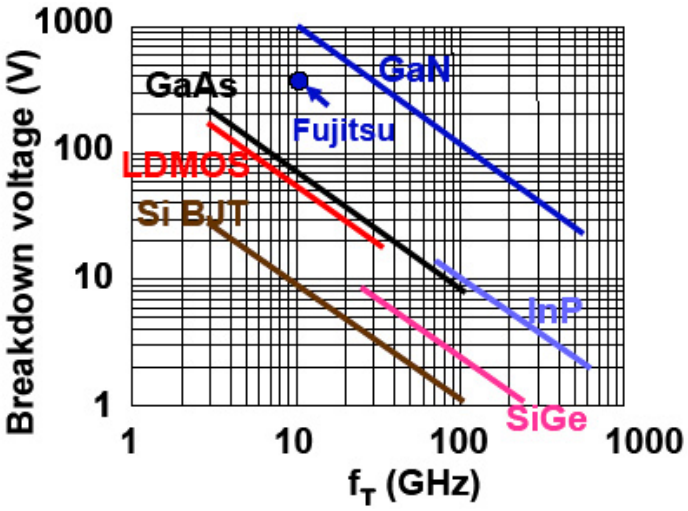


Fig. 3: Johnson's figure of merit [9]

In order to make possible the development of low compact base stations that offer both simple implementation and low operation cost, currently power amplifiers can be realized with GaN HEMTs. As displayed in Fig. 3, in fact, they are characterized by higher breakdown voltage with higher cut-off frequency than devices based on other materials (such as LDMOS and PHEMTs), providing in this way more system efficiency [9]. Finally, although GaN on Si HEMTs are not as performing as the equivalent SiC based device, they are beginning to dominate cost-driven sectors, thanks to their discrete results along with their lower cost.

On the other side, for applications characterized by high temperatures and harsh environments, SiC based devices are indeed favoured to operate at higher power densities than either GaN or Si. This is due to SiC's thermal conductivity, whose high value permits to the material of conducting heat more efficiently. So that, while actual Silicon transistors reach their normal operational temperatures approximately at 125°C, becoming highly susceptible to harsh environments, equivalent SiC devices promise to operate at temperature up to 600°C, and also at high power densities for both

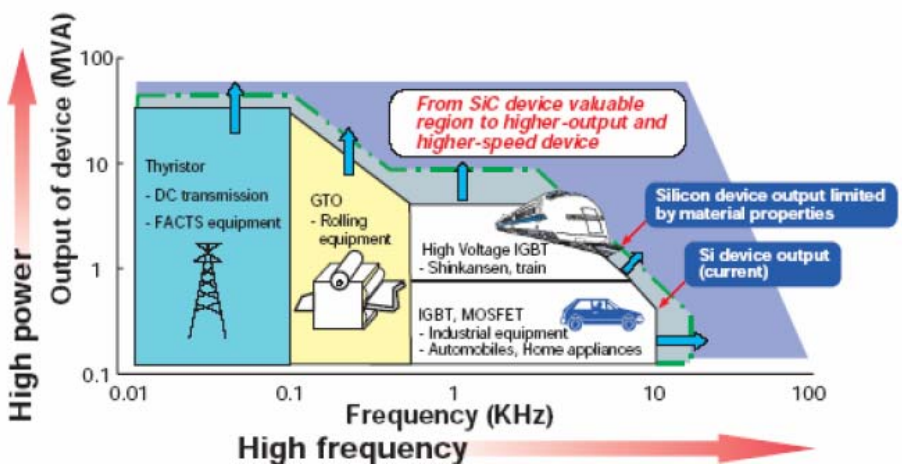


Fig. 4: Comparison of Si and SiC power devices for power applications [2]

medium and high frequency switching applications [10-11]. Therefore, higher thermal conductivity, combined with wide bandgap and high critical field, gives to SiC technology an advantage when high power is a desirable device feature [12-13]. Besides, compared to hetero-epitaxial GaN devices, SiC based structures are expected to dominate in power applications, also for a lower cost and easier fabrication of defect free wafers. This is due to important developments obtained in the last decades on sublimation process for the growth of Silicon Carbide crystals [14-15] and the commercial availability of single crystal 6H- and 4H-SiC wafers [16].

As shown in Fig. 4, the hope is that Silicon Carbide will enable a significant advance in the state of the power electronics in terms of ratings, losses, and speed of operation, shifting the theoretical limits for electronic devices even far beyond those of the most advanced Si devices.

Focusing on the determining factors in the operating frequency of a power circuit, such as the parasitic or non-idealities effects of the active devices, at the present the optimization effort on Silicon-based power devices has brought to just discrete improvements of performances. For majority carrier devices, for instance MOSFETs or JFETs, the limiting parasitic factors are the conduction resistance

(which determines conduction loss) and device capacitances (whose charging and discharging during turn-on and turn-off lead to switching loss). In a similar manner, for minority carrier devices, such as bipolar transistors and IGBTs, the conduction loss is due to both junction voltage drops and conduction resistance, while the switching behavior brings to further loss. Actually, regarding to Si MOSFET switching times, a decrease from 1.2μs down to 100ns is obtained; similarly, about the switching time of Si IGBTs, particularly the turn-off time, it has decreased from 3μs to 1.2μs. In terms of overall device ratings, the state of the power semiconductor industry at this time is power MOSFETs at 600V and 20A, and IGBTs up to 6kV and 1200A.

Regarding to Silicon Carbide market, Cree [16] is the leading manufacturer of SiC-based diodes for power control and management: its family of Zero Recovery rectifiers has essentially no reverse recovery at 600V, 650V and 1200V breakdown and is targeted for applications where low switching loss is required. More recent batches have achieved leakage currents of 18μA at 25°C and 50μA at 200°C with 1200V reverse bias. The offered current ratings range from 1A÷20A at 600V to 5A÷20A at 1200V. Rectifiers with currents of 10A and 25A at 1700V are also available in chip form. Other different companies sell Schottky diodes up to 20A [17], such as SiCED, Infineon and Rockwell Scientific.

For higher voltage applications it is necessary to use a pin device structure: actually, 20kV devices have been build in standard 200μm epi-layers. Respect to a SiC Schottky diode, it is observed that the conduction drop of a pin diode of equivalent area is lower at sufficiently high currents.

SiC MOSFETs developed by Cree were achieved by paralleling 3, 1.6mm x 1.6mm, dices. It is interesting to observe that the resulting SiC MOSFET achieves approximately 1/30th of the on-state resistance of an equivalent Si based MOSFET in the same die area. However, it is also important to note that the SiC MOSFET has a higher device capacitance or total drain charge than the corresponding Si device: given the thinner intrinsic region, the capacitance per unit area is approximately 10 times higher.

The reliability of the oxide remains the major concern to face for a commercial employment of SiC MOSFETs. The native oxide of

Silicon Carbide is SiO_2, which is typically grown on the SiC wafer using chemical vapour deposition (CVD) in a Silane (SiH_4) and oxygen environment. The problems occur at the SiO_2–SiC interface, where some of the Si is absorbed into the oxide layer, leaving behind carbon atoms that granulate and form carbon clusters at the interface. The resultant oxide layer is typically thicker than a corresponding Si device, requiring higher electric field to achieve channel inversion. Recent measurements show that the field strength in the gate oxide of these high voltage MOSFETs is too high for reliable operation at elevated temperatures. The simplest solution is to fabricate the devices with a thinner gate oxide: however, this requires an improvement of the quality of both oxide and interface.
From the above considerations, it is clear that SiC technology is not mature enough in order to benefit a high volume of production [18-19] in the field of power electronics. Much work must be done in this direction, especially for still unresolved material science issues. Many of the physical and electronic properties of SiC, in fact, are less well known than for Si and more commonly used III-V compounds. Among these, minority carrier lifetime, an important parameter specially for bipolar devices, is not still completely understood: although some measurements have been made on representative SiC material, its value on typical grown layers is not generally well evaluated and more attention is needed in this area. Due to the lake of a mature knowledge of their behavior, at the present, the majority of SiC devices are only experimental elements, with the exception of Schottky diodes, which are available for rectifier market.

Nowadays many companies and industry centers are devoting efforts to study and develop SiC devices, relying on the impact and benefits that this technology could have on the design of future power systems. With this aim, device optimizations are traditionally performed by hand, changing device parameters until sufficient performance is achieved. This is very time consuming work without any guarantee of achieving an optimal result.

Our developed analytical model, presented in the following, results a valid tool for evaluating the effect of geometrical and electrical changes on overall performance of 4H-SiC power diodes.

Chapter 2

Silicon Carbide (SiC)

Due to a rigorous formalism, the proposed model shows a good ability to support a large number of physical models, such as carrier mobility, incomplete ionization of doping atoms, and lifetime profiles. In this chapter, after a brief introduction to the principal structural characteristics of Silicon Carbide, the attention is focused on the physical and electrical parameters useful for analyzing the behavior of power diodes realized with this semiconductor, especially with the polytype of interest, the 4H-SiC.

2.1 Crystallographic Structure and Polytypes of SiC

The Silicon Carbide is the most stable compound of carbon (C) and silicon (Si) among those belonging to IV group of periodic table, with a partially ionic bond between C and Si atoms. The fundamental structural unit is a tetrahedron, with four atoms of Si (C) and one atom of C (Si) at the center, as shown in Fig. 5.

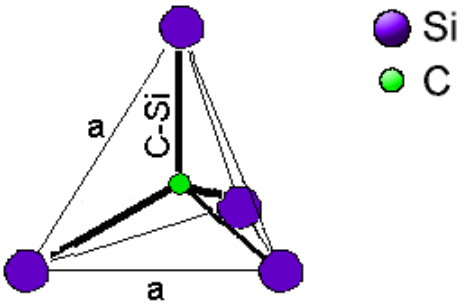


Fig. 5: Basic structural unit of Silicon Carbide

The distance named *a* between adjacent Si and C atoms is near to 3.08 Å; the C atom is located at mass centre of the tetraedric structure so that to keep an equidistance among neighbouring Si atoms of about $a\sqrt{\frac{3}{8}} = 1.89$ Å. The height of the cell, named *c*, changes among the polytypes: in particular, the *c/a* ratio is 1.641, 3.271 e 4.908, respectively for 2H-, 4H- and 6H-SiC [20].

Silicon Carbide exhibits a one-dimensional polymorphism called polytypism. There are a large number of different SiC polytypes which are characterized by the stacking sequence of the tetrahedrally bonded Si-C bilayers. While the individual bond lengths and local atomic environments are nearly identical, the overall symmetry of the crystal is determined by the stacking periodicity [21]. There are three possible positions available for each SiC bilayer with respect to its adjacent bilayers: all maintain the tetrahedral bonding scheme of the crystal and to each one it is arbitrarily assigned the notation A, B, or C. A schematic view of different stacking sequence for some common SiC polytypes is presented in Fig. 6, while a complete analysis to SiC polytypism can be found in [22].

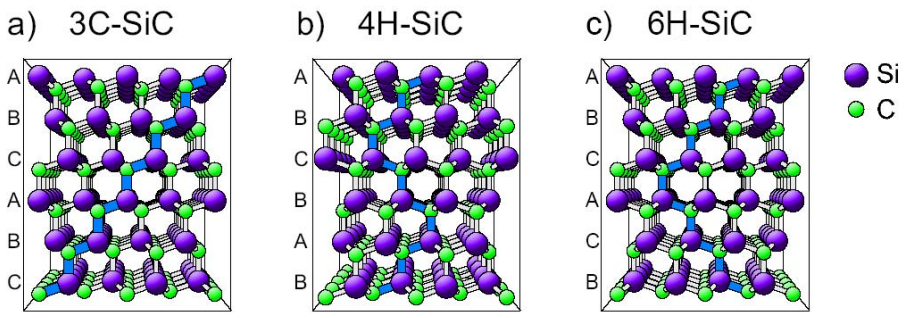


Fig. 6: Crystal structure of different SiC polytypes, displayed parallel to the $11\bar{2}0$ plane: a) zinkblende (cubic 3C-SiC), b) hexagonal 4H-SiC and c) hexagonal 6H-SiC [23]

Depending on the stacking order, the bonding between Si and C atoms in adjacent bilayer planes is either of zinkblende (cubic) or wurtzite (hexagonal) nature. So that each type of bond provides a slightly altered atomic environment, whose effect is relevant when the substitutional impurity incorporation and electronic transport properties of SiC are considered. In Fig. 7, the inequivalent layers are denoted by the letters *h* and *k* and the hexagonality of a polytype can be defined as the percentage of *h-type* layers, according to the Jagodzinski's notation [24].

There are other different ways to indicate the SiC polytypes. The traditional notation consists of using the stacking sequence, so that 4H- and 6H-SiC are respectively indicated by the sequence of *ABCB* and *ABCACB*. Besides this, another commonly used notation is due to

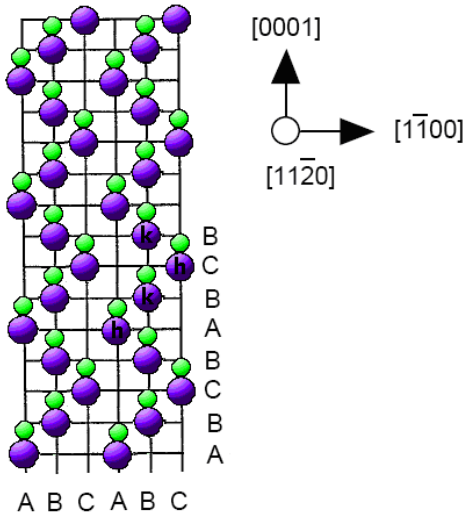


Fig. 7: Crystal structure of 4H-SiC polytype. Half of the atomic sites are hexagonally (h) while half are cubic (k)

Ramsdell [25], who categorizes every polytype with a number, followed by a letter: the first one represents the stacking periodicity, while the latter the bonding type, so that 4H- and 6H-SiC are hexagonal polytypes (which are also referred to as α-SiC in literature) with a stacking period of four and six, respectively. A review of the possible notations for indicating the principal SiC polytypes is reported in Table 1.

Ramsdell	***ABC***	***Jagodzinski***
2H (wurtzite)	*AB*	*h*
3C (zinkblende)	*ABC*	*k*
4H	*ABCB*	*hk*
6H	*ABCACB*	*hkk*
15R	*ABCACBCABACABCB*	*hkkhk*

Table 1: The most common notations of some of the SiC polytypes [26]

2.2 Transport Properties

The transport properties of 4H-SiC polytype are listed in Table 2, along with other wide bandgap semiconductors, like Gallium Nitride and Diamond, and the most commonly used semiconductor materials (Si and GaAs). By a direct comparison, the advantages of SiC over Si are the tenfold increase in breakdown fields, twofold increase in saturation velocity, and more than doubling of thermal conductivity. Although the carrier mobility in Silicon Carbide is somewhat lower than in Silicon, in general the transport parameters give Silicon Carbide devices better performances than comparable Silicon devices. Investigating the basic electrical and physical parameters for electronic devices, such as bandgap (E_g), mobility (μ), saturation velocity (v_{sat}), breakdown electric field (E_{crit}), and thermal conductivity (λ), it instantly evident that wide bandgap semiconductors are very promising materials for using in high performance electronic devices.

	Si	***GaAs***	***4H-SiC***	***GaN***	***Diamond***
$Eg_{@300K}$ *[eV]*	*1.1*	*1.4*	*3.2*	*3.4*	*5.45*
Ec [MV/cm]	*0.3*	*0.4*	*2.2*	*2.0*	*10*
v_{sat} *[x10^7 cm/s]*	*1.0*	*2.0*	*2.0*	*2.5*	*2.7*
$\mu_{n@N=10^{16}cm^{-3}}$ *[cm^2/V s]*	*1500*	*8500*	*720*	*1000*	*2200*
$\mu_{p@N=10^{16}cm^{-3}}$ *[cm^2/V s]*	*480*	*400*	*120*	*30*	*850*
ε_r	*11.9*	*13.1*	*9.7*	*8.9*	*5.5*
λ *[W/cm K]*	*1.5*	*0.5*	*5*	*1.3*	*22*

Table 2: Key characteristics of SiC vs. other semiconductor materials

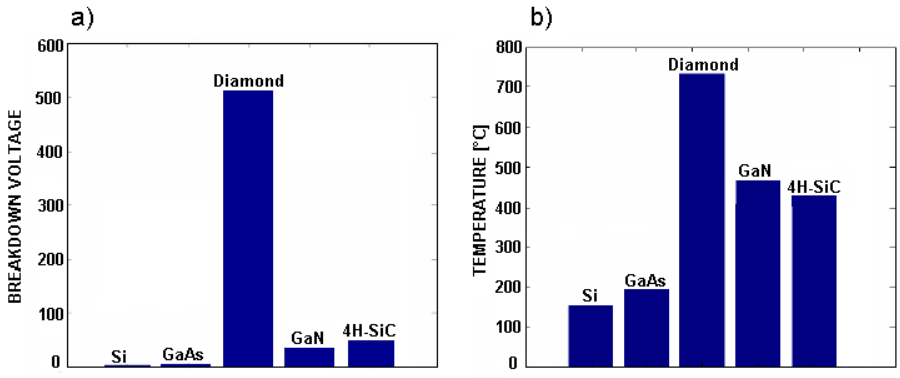


Fig. 8: Maximum a) normalized breakdown voltage and b) operational temperature of a power device realized with traditional and wide bandgap semiconductor

In fact:

- A higher electric breakdown field brings to power devices with higher breakdown voltages, as shown in Fig. 8.a, where the reported values are normalized to the breakdown voltage of Si diode, together with the assumption that the diodes are realized with the same doping density. As can be seen, the theoretical breakdown voltage of a Diamond diode results in 500 times bigger than of a Si diode, while the breakdown voltage numbers for 4H-SiC and GaN are 46 and 34 times that of Si diode, respectively. For the same breakdown voltage, instead, the consequence of higher E_{crit} is the reduction of the width of the drift region, which enables smaller unipolar device and smaller on-resistance as can be seen in Fig. 9. This turns in lower conduction loss and in a consequent increasing of the efficiency.

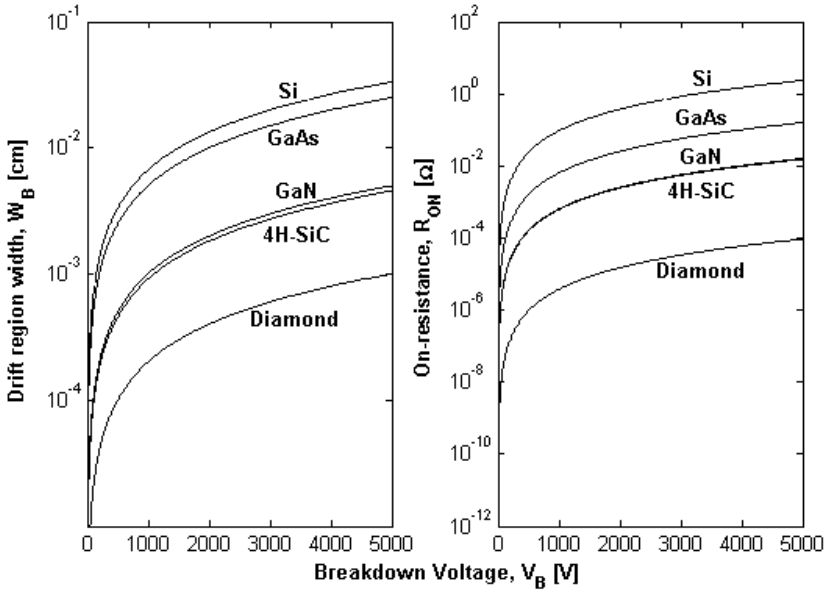


Fig. 9: Width (left) and resistance (right) of the drift region vs. breakdown voltage

- Semiconductors with wider bandgap can operate at higher temperatures (see Fig. 7.b).
- Due to the direct proportionality between the high frequency switching capability of a semiconductor material and its drift velocity, it is expected that wide bandgap materials, having more than twice the drift velocity of Si, could be switched at higher frequencies than their Si counterparts. Moreover, higher drift velocity allows charge in the depletion region of a diode to be removed faster, so it is likely that the reverse recovery current of diodes based on wide bandgap semiconductors is smaller and the reverse recovery time is shorter.
- The thermal conductivity does not directly affect the performance, but with a good thermal conductivity it is easier to conduct the heat away from the chip to a heat sink, so it obviates the need to have bulky and expensive cooling systems.

As discussed in Chapter 1, all these properties make wide bandgap semiconductors good candidates for high power, high temperature, and high frequency devices. However, it is important to remark that, respect to the other wide bandgap competitors, SiC is the best suitable transition material for future power electronics devices. In fact, although Diamond is the material with the best electrical characteristics, it must face significant processing hurdles that must be overcome before it can be commercially used for power applications. On the other side, GaN turns out less attractive than SiC for different aspects, such as the unavailability of pure wafers, the lake of a native oxide required for MOS device, and for having a thermal conductivity equals only one-fourth of that of SiC. However, it must be remarked that, although SiC process technology is continuously improving, it is not yet mature to introduce large volume of commercial devices into the market. In fact, compared to Silicon, this innovative material remains very expensive, the obtained wafers are just of discrete quality and the resultant devices show electrical behaviors not completely known.

2.2.1 Bandgap Energy

Many of the favourable transport parameters in SiC are related to its large bandgap: along with conduction and valence band structure, it defines the electric properties of the semiconductor. Band structure calculations for SiC have been made for the past forty years; early, the theorists have concentrated on the zinkblende 3C-SiC polytype and the wurtzite 2H-SiC structure given that the other polytypes are much more complicated due to their larger unit cell [27]. Then, since both 3C-SiC and 2H-SiC are indirect-gap semiconductors, they have reasonably assumed that all polytypes are indirect-gap semiconductors. In the following years, the accuracy of initial calculations has been considerably improved to work also on the band structures of 4H- and 6H-SiC polytypes [28-30]. The resultant first Brillouin zone and band-structure for 4H-SiC are shown in Fig. 10 (the hexagonal direction [0001] coincides with the k_Z axis). In a similar manner respect to the other polytypes, the top of valence band for 4H-SiC is localized at the Γ–point, while the bottom of conduction band is localized in the M–point.

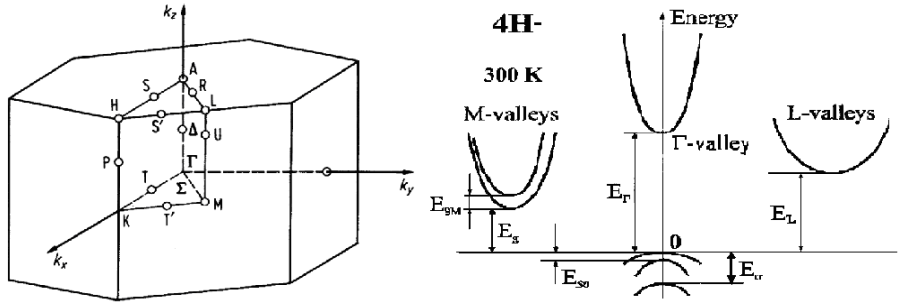


Fig. 10: First Brillouin zone for α-SiC polytypes (left) and band-structure of 4H-SiC polytype (right)

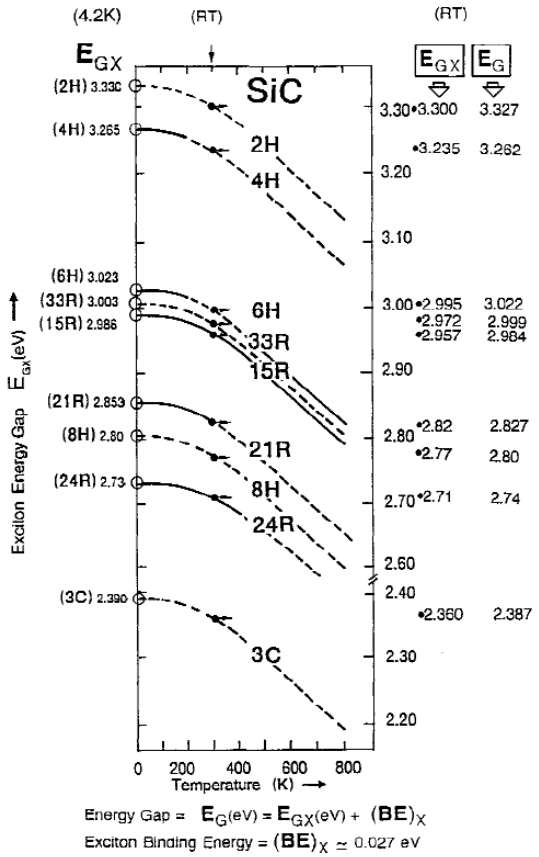


Fig. 11: Summary of the experimentally observed exciton bandgaps and their temperature variation for the different polytypes [27]

Fig. 11 summarizes the experimentally observed exciton bandgaps and their temperature variations. Experiments have also given an estimate of the bending energy of the exciton 3C-SiC of about 27meV: with the assumption that this value is not different for the other polytypes, the actual bandgap can be calculated by adding an amount of 27meV to the known value of the exciton bandgap. Ambient-temperature values of total (E_G) and exicton (E_{GX}) bandgap are also reported in Fig. 11 for the principal SiC polytypes.

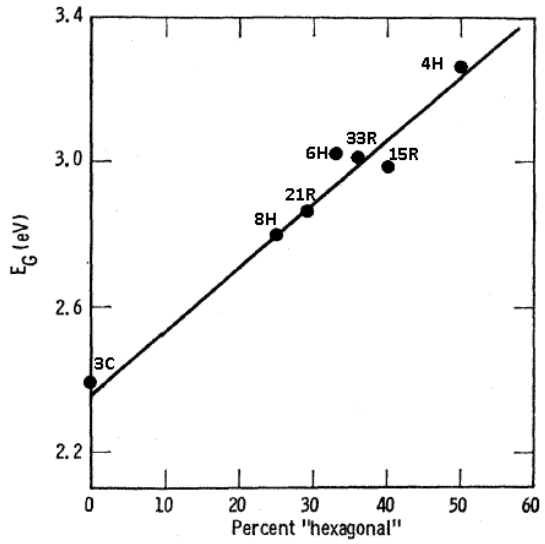


Fig. 12: Linear behavior of energy bandgap as a function of percentage of hexagonal planes

Choyke, Hamilton and Patrick in [31] have derived an empirical correlation of E_G with percentage of hexagonal planes, whose value can be easily obtained by Jagodzinski's notation (see Table 1): for the principal polytypes, a plot of energy gap against percent hexagonal is shown in Fig. 12, evidencing a quasi linear relationship.

Due to a wide bandgap for all SiC polytypes, ranging from 2.38eV to 3.33eV (see Fig. 11), it is evident that electronic devices in Silicon Carbide can operate at extremely high temperatures without suffering from intrinsic conduction effects, since they are negligible at temperatures up to 600°C. Moreover, being the bandgap the minimum energy required to create an electron-hole pair, SiC reveals suitable as a detector material for UV radiation with minimal noise from the visible background [32], since the value of about 3eV as bandgap energy corresponds to a photon with wavelength approximately of 400nm, making SiC an insensible material to the main part of the visible spectrum.

Because of the interest for the employment of SiC material also for high temperature applications, it is relevant to adequately describe

the dependence of bandgap energy by this parameter. Pioneering work in this area was performed by Choyke [33] who observed that, in the temperature range 0÷800 K, the bandgap value can be evaluated by an analogue expression used for Silicon. Although Choyke's measurements are dated, at the present it is been observed that they accurately predict, for all α-SiC polytypes, the temperature variation of the bandgap. This results equal to dEg/dT=-3.3x10^{-4} eV/K, so that the complete bandgap relation for a generic SiC polytype, with a total bandgap at ambient temperature (T_O) equals to E_G, is given by the following:

$$E_g(T) = E_{gO} + \alpha(T - T_O), \text{ with } \begin{cases} E_{gO} = \mathrm{E_G}\ [eV] \\ \alpha = -3.3\ 10^{-4}\ [eV/K] \\ T_O = 300\ [K] \end{cases} \quad (2\text{-}1)$$

2.2.2 Intrinsic Carrier Density

With the parabolic approximation for conduction and valence band [34], the intrinsic carrier concentration can be expressed as a function of the temperature:

$$n_i(T) = \sqrt{N_C(T)N_V(T)}\ e^{-\frac{E_g(T)}{2KT}} \quad (2\text{-}2)$$

where K is Boltzmann constant and $N_C(T)$ and $N_V(T)$ are the effective density of states in the conduction and valence band, respectively, which are given by:

$$N_C(T) = 2M_c\left(\frac{2\pi m_e^* KT}{h^2}\right)^{\frac{3}{2}} = N_C(T_O)\left(\frac{T}{T_O}\right)^{\frac{3}{2}} \quad (2\text{-}3a)$$

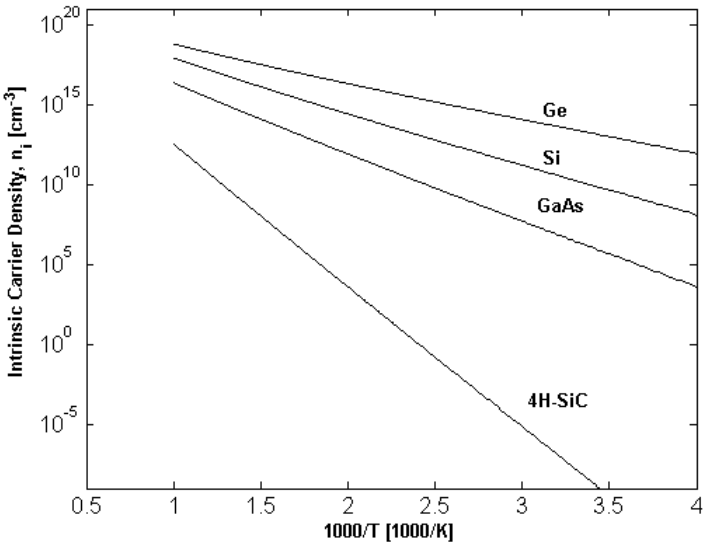


Fig. 13: Intrinsic carrier density as a function of reciprocal temperature

$$N_V(T) = 2\left(\frac{2\pi m_h^* KT}{h^2}\right)^{\frac{3}{2}} = N_V(T_O)\left(\frac{T}{T_O}\right)^{\frac{3}{2}} \qquad \text{(2-3b)}$$

with m_e^* and m_h^* the electron and hole effective masses, and *Mc* the equivalent valleys in conduction band. For the 4H-SiC polytype, the values of these parameters are: $m_e^*=0.77m_0$ [35], $m_h^*=1.2m_0$ [36] (where m_0 is the electron rest mass) and *Mc*=3.

Fig. 13 shows the intrinsic carrier concentration for traditional and wide bandgap semiconductors, where also the temperature dependence of energy gap is considered. As expected, the bigger bandgap brings to lower value of n_i: in particular for 4H-SiC, at ambient temperature the intrinsic carrier density results smaller by the order of 18 compared to Silicon.

The modification of the density of states by heavy doping leads to an additional influence on intrinsic carrier density, the so-called "bandgap narrowing". This phenomenon, in more detail analyzed in

section 2.4, is generally modelled by rigid shifts of the band edges [37] and brings, evaluating the consequent bandgap shrinking by the term ΔE_g, to express the effective intrinsic carrier concentration as:

$$n_{ie} = n_i \, e^{\frac{\Delta E_g}{2KT}} \tag{2-4}$$

2.2.3 Saturation Velocity

At high electric fields the velocity ceases to be proportional to the electric field, due to increased scattering and it saturates at v_{sat} value, which for SiC is approximately twice the value for silicon; in this way, it is allowed to realize faster devices with shorter switching times.

2.2.4 Mobility

As shown in Table 2, the mobility in SiC is somewhat lower than for Silicon and much lower than in high-mobility materials, such as GaAs: however, the low mobility in SiC devices is compensated by operation at larger electric fields taking advantage of the higher carrier velocity.

The mobility describes the mean velocity of electrons and holes when an electric field is applied. At low electric fields, the velocity increases proportional to the field, since the carrier mobility is fundamentally due to the Coulomb and phonon scattering; for higher fields, the proportionality is lost and the velocity saturates at v_{sat}. In general, there are various scattering mechanisms, schematized in Fig. 14, which determine the free carrier mobilities.

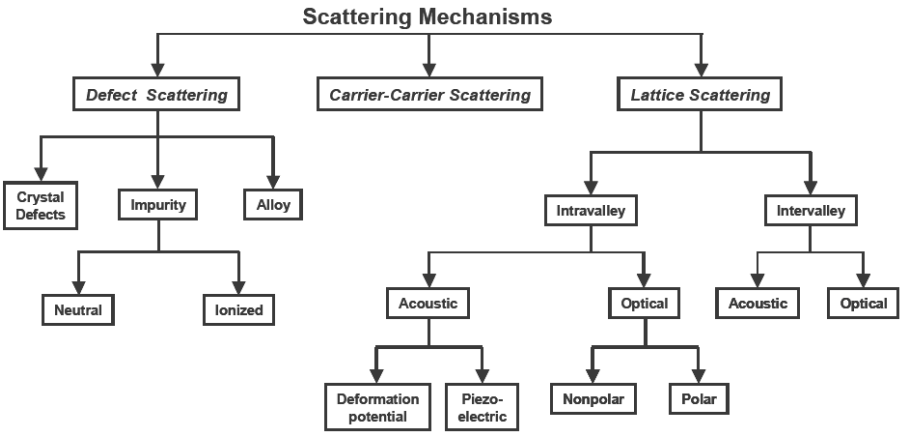


Fig. 14: Schematization of the principal scattering mechanisms

Due to the complex nature of these mechanisms, phenomenological models have been developed for the various experimentally observed mobility phenomena in Si devices [38]. The contributions from different scattering processes can be combined using the simple Matthiessen's rule:

$$\frac{1}{\mu_{eff}} = \sum_i \frac{1}{\mu_i}. \tag{2-5}$$

In literature, a lot of low field mobility models for Si are available: they represent, along with experimental data and Monte Carlo simulations published for SiC, a valid fundament to develop empirical expressions related to the mobility for this innovative material. Contributions focused on this aim are [39-30], while a comparative analysis of these models can be found in [41].

Because of their crystallographic structure, the α-SiC polytype are characterized by an anisotropy of the principal electro thermal parameters. Although, in general, anisotropic parameters result expressed by second rank tensors, for 4H- and 6H- polytypes they are reduced to a diagonal form [42], so that it is possible to use the following convenient representation for the electron mobility:

$$\mu = \begin{bmatrix} \mu_{\perp} & 0 & 0 \\ 0 & \mu_{\perp} & 0 \\ 0 & 0 & \mu_{\parallel} \end{bmatrix}.$$

Actually an exhaustive modelling of anisotropic properties does not exist; since the most of SiC devices are realized on wafers with surface orthogonal, or lightly rotated, to c-axis ([0001] direction), it is common rule to define an anisotropic ratio between base-plane and the [0001] direction. Following this observation, because the commonly measured mobility is orthogonal to c-axis ($\mu\perp$) while the parallel component is generally not equal, the ratio between these components is derived by experiments or by Monte Carlo simulations.

In relation to 4H-SiC, the obtained results define a unitary ratio and a ratio of $\mu\perp/\mu_{||}=0.8$ for holes and electrons, respectively. Anyway, due to a better isotropic behavior of 4H-SiC respect to the other polytypes, it is possible to consider just the mobility in the base-plane with a reasonable approximation.

From published experimental data obtained by Hall measurements on 4H-SiC bulk epitaxial layers, free carrier mobility tensor components are extracted, within a wide range of impurity concentration and temperature [39-43]. The data can be well described using the phenomenological model of Caughey-Thomas [44], including the temperature dependence for $T > 300$K:

$$\mu_i^{low}(T,N) = \mu_{0i}^{\min}\left(\frac{T}{300}\right)^{\alpha_i} + \frac{\mu_{0i}^{\max}\left(\frac{T}{300}\right)^{\beta_i} - \mu_{0i}^{\min}\left(\frac{T}{300}\right)^{\alpha_i}}{1+\left(\frac{N}{N_i^{crit}}\right)^{\delta_i}\left(\frac{T}{300}\right)^{\gamma_i}},\ i=n,\ p \quad (2\text{-}6)$$

where the various parameters N^{crit}, α, β, γ and δ, taken from the measurement results of Roschke et al. and Schaffer for SiC, are listed in Table 3. Although the mobility parameters depend on technology,

	μ_{0i}^{max} (To) [cm²/V s]	μ_{0i}^{min} (To) [cm²/V s]	N_i^{crit} [cm⁻³]	α_i	β_i	δ_i	γ_i
n	950	40.0	2.00E17	-0.5	-2.40	0.76	-0.76
p	125	15.9	1.76E17		-2.15	0.34	-0.34

Table 3: Values of low field mobility parameters for 4H-SiC, at To=300K

this table can serve as a base for evaluating measured device characteristics. In Fig. 15 it is interesting observe that, for the same doping, the less value of hole mobility compared with electron one is related to a smaller electron effective mass. The temperature dependence of electron and hole mobility is shown in Fig. 16.

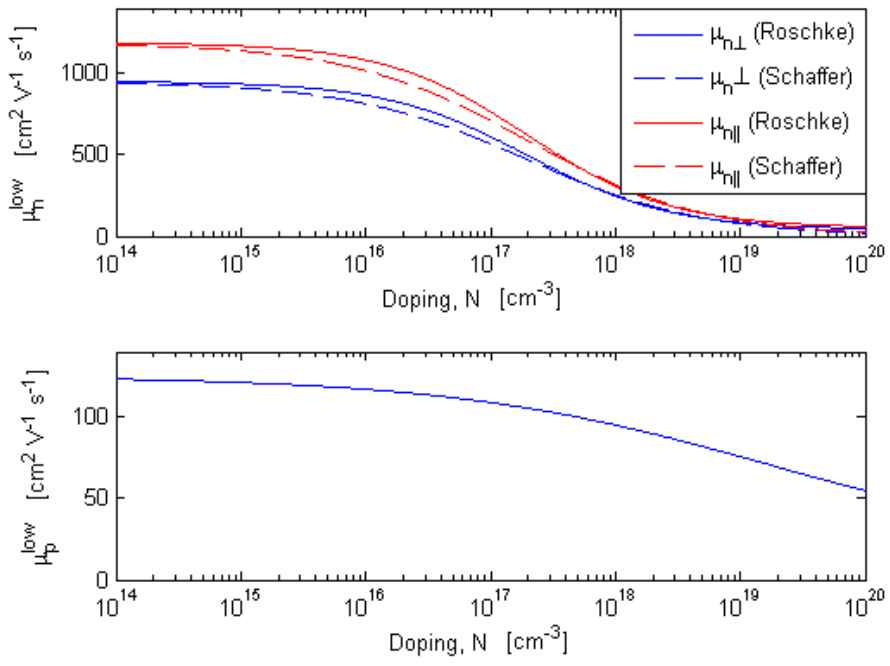


Fig. 15: Electron and hole low field mobility models for 4H-SiC at To=300K

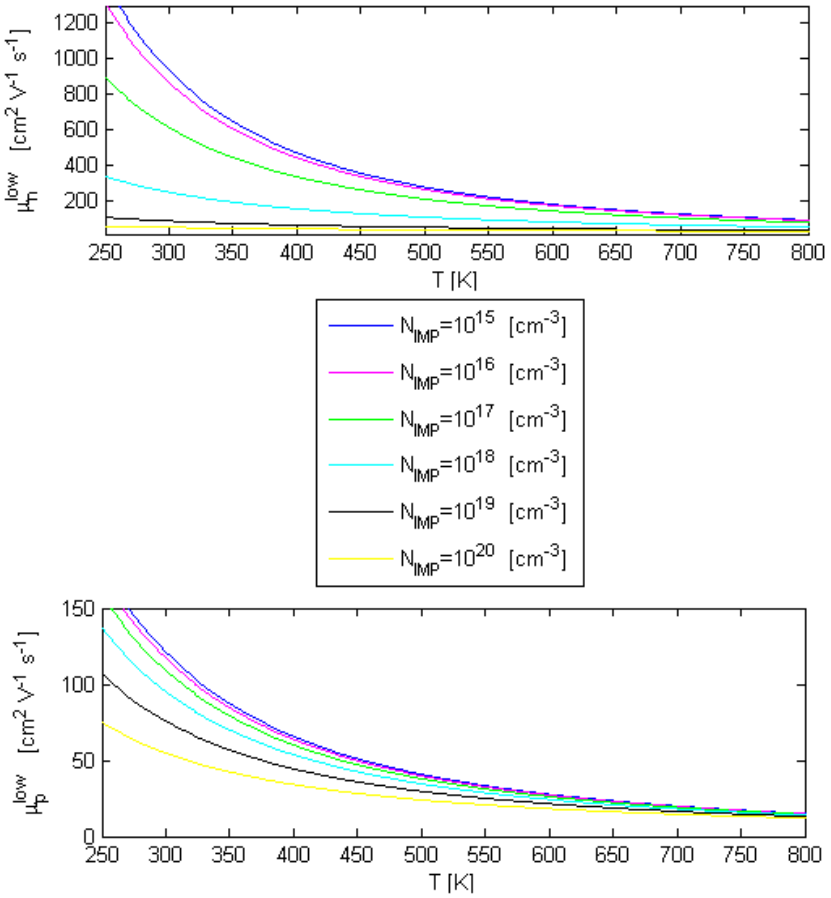


Fig. 16: Temperature dependence of electron and hole low field mobility for 4H-SiC at different doping values

At high electric field, the mobility models must keep in count their dependence from it; for SiC, the analytical expression used for this aim is analogue to that largely employed for Silicon [39]:

$$\mu_i = \frac{\mu_i^{low}}{\left[1+\left(\frac{\mu_i^{low} E}{v_{sat}}\right)^{\beta}\right]^{\frac{1}{\beta}}}, \quad i=n, p. \tag{2-7a}$$

with the temperature dependence of v_{sat} and β coefficient described by the following:

$$\begin{cases} v_{sat} = \dfrac{v_{\max}}{1+0.6\ e^{\frac{T}{600}}} \\ \beta = \beta_o + a\ e^{\frac{T-T_{ref}}{b}} \end{cases}. \tag{2-7b}$$

All available measured data refers to a current flow perpendicular to the c-axis, while no measured data of holes is presently available. For 4H-SiC the saturation velocity is $2x10^7$cm/s at ambient temperature and the different fitting parameters (v_{max}, β_o, a, T_{ref} e b) are summarized in Table 4.

In Fig. 17 is plotted the electron drift velocity as a function of electric field in 4H-SiC at three different temperature and with a doping of 10^{17}cm^{-3}.

	v_{max} [cm/s]	β_o	T_{ref} [K]	a	b
4H-SiC	*4.77E7*	*0.816*	*327*	*4.27E-2*	*98.4*

Table 4: Values of high field mobility parameters for 4H-SiC

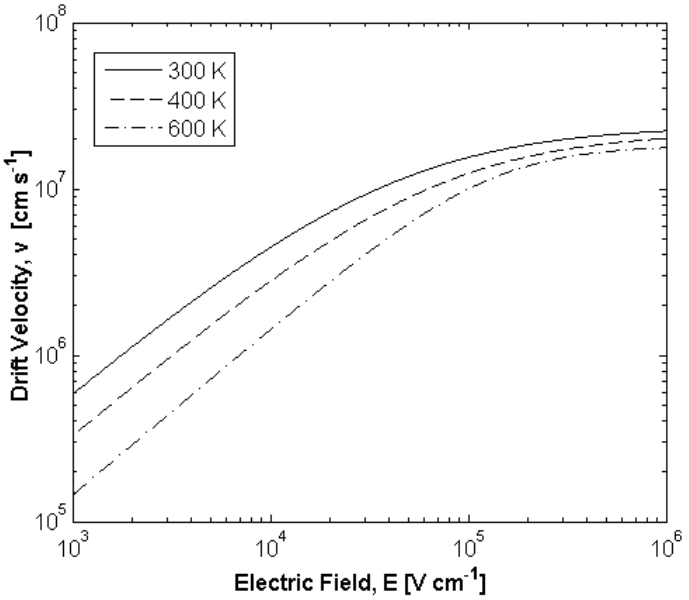


Fig. 17: Saturation of the electron drift velocity with increasing electric field in 4H-SiC

2.3 Carrier Freeze Out

Although the large bandgap of SiC is a favourable property in most cases, it also causes one of its largest disadvantage: the energy levels for the doping materials used in Silicon Carbide are located at a significant distance from the band-edge. This brings to a high thermal ionization energy also at ambient temperature, comparable value to the mean thermal energy for the carriers at this temperature (KT=25.9meV). The resultant effect is that a fraction of the carriers are not thermally activated: they are instead frozen in the band-gap without being ionized. This phenomenon is known as *freeze-out* and in the traditional semiconductors is significant at low temperatures.

With the aim to accurately describe the doping phenomenon, it must keep in count that the inequivalent α-SiC sites (one with cubic

surrounding and the other with hexagonal surrounding) are expected to cause also site dependent impurity levels [45].

Generally, the most common dopants for 4H- and 6H-SiC are nitrogen (N) and phosphor (P) for n-type layers, while aluminum (Al) and boron (B) are acceptor atoms. In detail, N preferentially incorporates into the lattice sites which are normally occupied by C atoms, while P and Al prefer the Silicon sites of SiC and B may substitute on both sites [46].

Relatively to the behavior of bipolar devices, the incomplete ionization of the most common dopants in SiC will affect it within a wide range of operation conditions; fundamentally, it will causes a substantial increase of the bulk resistance dependent on temperature and doping concentration. Therefore, an appropriate incomplete ionization model which accounts for variation of ionization rates and also the lattice site-dependent impurity level must be considered.

By referring to a generic n-type extrinsic region, because a corresponding equation it can be derived for the holes, the relative position of the Fermi level, E_{Fn}, required in the ionized (activated) donor density formula:

$$N_D^+ = N_D \left[1 + g_d \exp\left(\frac{E_{Fn} - E_d}{KT} \right) \right]^{-1} \tag{2-8}$$

can be evaluated by equating the above expression with the majority carrier density:

$$n = N_C(T_O) \left(\frac{T}{T_O} \right)^{1.5} \exp\left(-\frac{E_C - E_{Fn}}{KT} \right) \tag{2-9}$$

being g_d the degeneration factor of conduction band, thus obtaining the following expression for the ionization grade:

$$\xi_D = \frac{N_D^+}{N_D} = \frac{-1+\sqrt{1+4g_d \frac{N_D}{N_C(T)} e^{\frac{\Delta E_d}{KT}}}}{2g_d \frac{N_D}{N_C(T)} e^{\frac{\Delta E_d}{KT}}} \qquad (2\text{-}10)$$

where N_D is the doping level, ΔE_d represents the energy distance of donor level from conduction band, and $N_C(T)$ is the effective density of states presented in the subsection 2.2.2.

In the case of multiple, site-dependent energy levels, the ΔE_d expression becomes:

$$\begin{cases} \Delta E_{dh} = E_c - E_{dh} & \text{for hexagonal sites} \\ \Delta E_{dk} = E_c - E_{dk} & \text{for cubic sites} \end{cases} \qquad (2\text{-}11)$$

Therefore, the resultant ionized donor doping is given by:

$$N_D{}^+ = \sum_{i=1}^{X} N_{Dh_i}^+ + \sum_{j=1}^{Y} N_{Dk_j}^+ \qquad (2\text{-}12)$$

where X and Y represent the number of inequivalent hexagonal and cubic sites, respectively. For the 4H-SiC polytype, in particular, X=Y=1, and so the ionization rate is:

$$\xi_D = \frac{N_{Dh}^+ + N_{Dk}^+}{N_D} =$$

$$= \frac{-1+\sqrt{1+2g_d \frac{N_D}{N_C(T)} e^{\frac{\Delta E_{dh}}{KT}}}}{2g_d \frac{N_D}{N_C(T)} e^{\frac{\Delta E_{dh}}{KT}}} + \frac{-1+\sqrt{1+2g_d \frac{N_D}{N_C(T)} e^{\frac{\Delta E_{dk}}{KT}}}}{2g_d \frac{N_D}{N_C(T)} e^{\frac{\Delta E_{dk}}{KT}}} \qquad (2\text{-}13)$$

In Table 5 the experimental values of site-dependent ionization energy levels for the principal dopants for 4H-SiC and 6H-SiC are presented: for Al and B doping, independent ionization energy from polytype and occupied lattice site is noted, while the opposite behaviour is observed for donor atoms.

	Al	***B***	N_h	N_k	P_h	P_k
4H-SiC	*210 ± 20*	*330 ± 30*	*50 ± 5*	*90 ± 5*	*50 ± 5*	*90 ± 5*
6H-SiC	*210 ± 20*	*330 ± 30*	*80 ± 5*	*140 ± 5*	*80 ± 5*	*110 ± 10*

Table 5: Site-dependent, ionization energy levels [meV] for Al, B, N e P in α-SiC

In Fig. 18 the dependence of ionization rate by doping and temperature is reported for Aluminum and Nitrogen: at low doping levels most of the carriers are ionized at ambient temperature, but the fraction is reduced at higher levels.

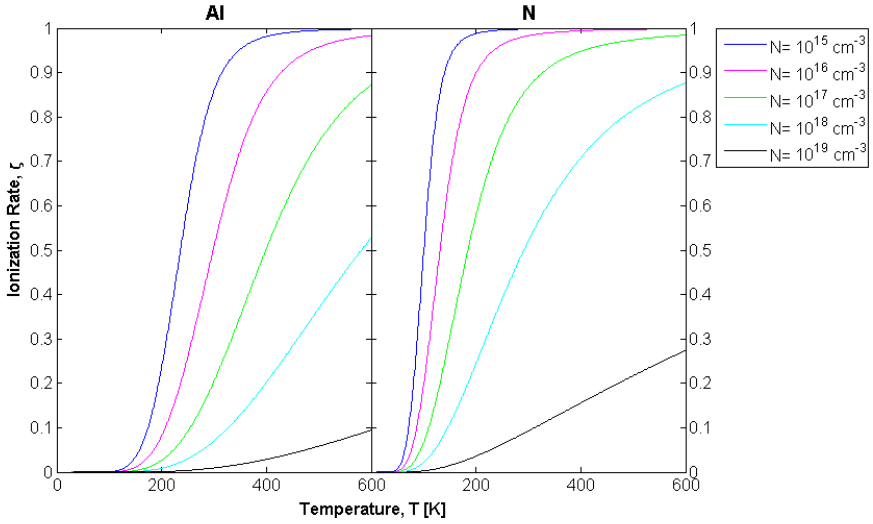


Fig. 18: Ionization degree of Al (left) and N (right) in electro thermal equilibrium

2.4 Bandgap Narrowing

In devices containing adjacent layers or regions with different doping concentrations, doping-induced band edge displacements may greatly influence device behaviour. This is due to the resultant potential barrier which influences carrier transport across the junctions.

Apparent bandgap narrowing models for calculating the shifts in band edges for 4H-, 6H- and 3C-SiC have been published in the 1998 by Lindefelt [47]. Relatively to 4H-SiC, he quantifies the band edge displacements as a function of the activated doping according to the following expressions:

$$\Delta E_{gd} = 1.7x10^{-2}\sqrt{\frac{N_D^+}{10^{18}}} + 1.9x10^{-2}\left(\frac{N_D^+}{10^{18}}\right)^{\frac{1}{4}} + 1.5x10^{-2}\left(\frac{N_D^+}{10^{18}}\right)^{\frac{1}{3}} \quad \text{(2-14a)}$$

$$\Delta E_{ga} = 1.54x10^{-2}\sqrt{\frac{N_A^-}{10^{18}}} + 1.3x10^{-2}\left(\frac{N_A^-}{10^{18}}\right)^{\frac{1}{3}} + 1.57x10^{-2}\left(\frac{N_A^-}{10^{18}}\right)^{\frac{1}{3}} \quad \text{(2-14b)}$$

As displayed in Fig. 19, where a direct comparison is done respect to the Si, a larger ΔE_g is expected in n-type material for 4H-SiC, whereas approximately the same displacements are obtained in p-type material for both materials. The resultant bandgap narrowing effect and its influence on the intrinsic carrier concentration are shown in Fig. 20.

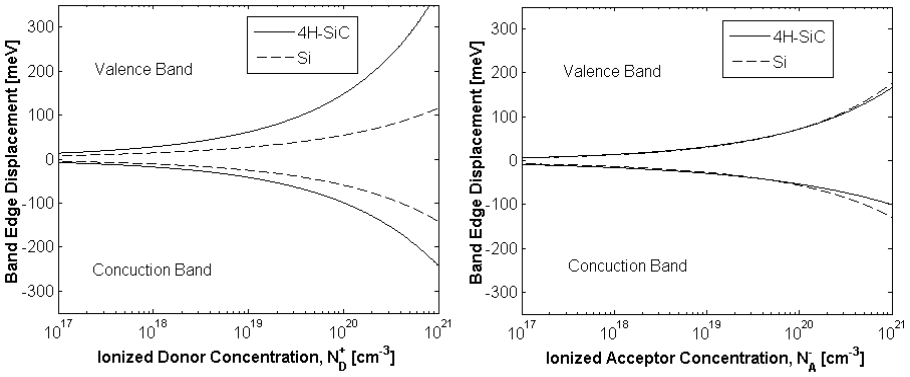


Fig. 19: Conduction and valence band displacements for 4H–SiC vs ionized doping concentration in purely *n*-type (left) and *p*-type (right) material. For comparison, the band edge displacements for Si are also shown

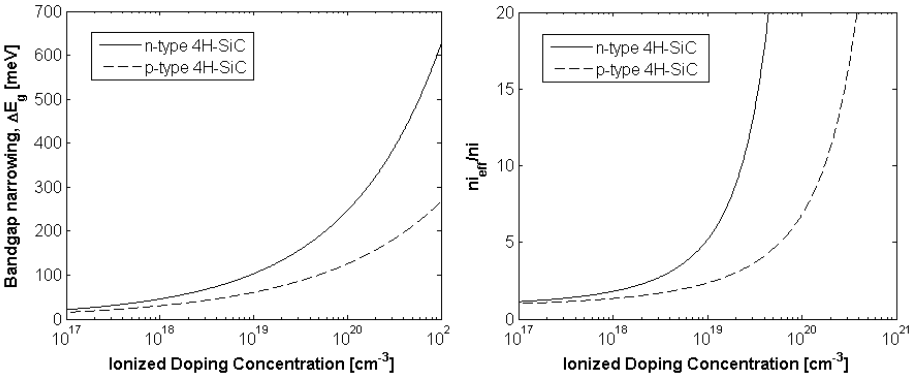


Fig. 20: Bandgap narrowing in 4H-SiC (left) and corresponding influence on the effective intrinsic carrier density (right)

2.5 Carrier Recombination Lifetime

In semiconductor materials the generation of electrons and holes in excess is due to thermal activity, electrical and/or light excitation; opposite to this phenomenon, there is the recombination of such carriers, whose rate can be defined by the following expression:

$$U = \frac{\Delta c}{\tau} \tag{2-15}$$

with Δc the excess carrier density, and τ the recombination lifetime of such carriers. This latter parameter is strongly related to the crystal quality and defects and, since its value quantifies the effect of different processes which conjointly participate to the recombination phenomenon, it is important to use a complete model that includes all the involved recombination mechanisms in order to get an accurate estimation of the effective lifetime.

As shown in the following sections, there are fundamentally three recombination mechanisms which occur in semiconductors, with different intensities: radiative recombination, Auger recombination and recombination through defects in the bandgap [48]. Respect to the latter, the first two are band to band, or direct, recombination processes and they depend only on the concentration of free carriers present in the bulk semiconductor.

The free carrier concentrations (electrons and holes) are defined as:

$$n = n_0 + \Delta n \approx N_D + \Delta n \quad \text{for n - type material} \tag{2-16a}$$

$$p = p_0 + \Delta p \approx N_A + \Delta p \quad \text{for p - type material} \tag{2-16b}$$

where n_0 , p_0 are the electron and hole concentrations at equilibrium, N_D, N_A the donor and acceptor doping density, and Δn , Δp the

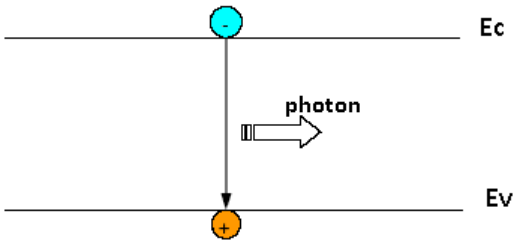


Fig. 21: Radiative recombination process

density of electrons and holes in excess per unit volume. At equilibrium, both excess carrier concentrations must be equal, because the generation process involves the creation of electron-hole pairs, i.e. $\Delta n = \Delta p$. Therefore, at given doping density and illumination level mechanisms, the direct recombination processes are exclusively inherent to the material properties: in this case, the only way to reduce the total recombination rate is through the minimization of the number of defect during the manufacture process.

2.5.1 Radiative Recombination

The radiative recombination consists of the annihilation of an electron-hole pair, which leads to the creation of a photon with energy close to that of the bandgap (see Fig. 21). If the carrier has energy higher than that of the bandgap, the excess energy is released as thermal energy to the lattice. The radiative recombination rate depends directly on the availability of electrons and holes and it is given by:

$$U_{rad} = \beta\left(np - n_i^{\,2}\right) \tag{2-17}$$

where β is the radiative recombination coefficient.

The radiative carrier lifetime results constant at low injection levels, while it is inversely proportional to the excess carrier density at

high injection levels, as can be observed combining Eq. (2-17) with Eq. (2-16), which bring to the followings:

$$\tau_{rad}^{low} = \frac{1}{\beta N_{D,A}} \tag{2-18a}$$

$$\tau_{rad}^{high} = \frac{1}{\beta \Delta n} \tag{2-18b}$$

Since the Silicon Carbide is an indirect semiconductor, like the Silicon, the radiative process must be assisted by a photon and a phonon in order to simultaneously preserve momentum and energy. This makes the radiative recombination for SiC much less probable respect to the others recombination mechanisms.

2.5.2 Auger Recombination

Auger recombination, that can be considered as the inverse of the impact ionization process, involves three particles (one electron and two holes, or vice versa). It occurs when the energy released by the recombination of an electron-hole pair is transferred to a third free carrier [49], as shown in Fig. 22. In this process, at low injection level, the expression of the recombination rate is related to the excess

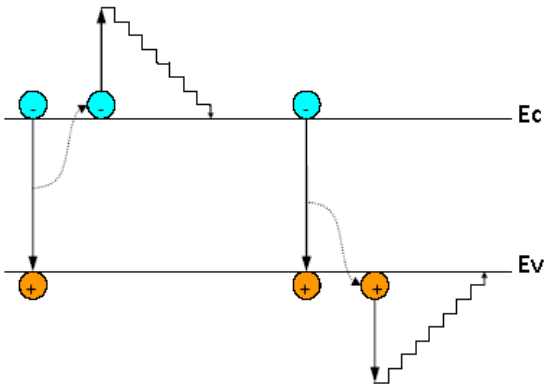


Fig. 22: Auger recombination process

carrier concentration and to doping density [50]:

$$U_{Auger}^{n} = C_n \Delta p N_D^{\ 2} \quad \text{for n - type material} \tag{2-19a}$$

$$U_{Auger}^{p} = C_p \Delta n N_A^{\ 2} \quad \text{for p - type material} \tag{2-19b}$$

with C_n and C_p the Auger coefficients for electrons and holes.

Therefore, the Auger carrier lifetime at low injection level is given by:

$$\tau_{Auger}^{low} = \frac{1}{C_{n,p} N_{D,A}^2} \tag{2-20a}$$

Keeping in count that at high injection levels both carriers participate to the recombination process, the carrier lifetime at these regimes can be expressed as:

$$\tau_{Auger}^{high} = \frac{1}{C_a \Delta n^2} \tag{2-20b}$$

where $C_a = C_n + C_p$ is the ambipolar Auger recombination coefficient.

Focused on the evaluation of radiative and Auger coefficients, abundant literature exists for the traditional semiconductors, but this is not the same for Silicon Carbide. By our knowledge, estimated and derived values for 4H-SiC can be found just in [51]: they are reported in Table 6, along with values of the traditional semiconductors.

	Radiative Recombination Coefficient β *[cm^3 s^{-1}]*	*Auger Recombination Coefficient* $C_{n,p}$ *[cm^6 s^{-1}]*
Si	*2.0E-15*	C_n*=2.8E-31;* C_p*=1.0E-31*
Ge	*5.2E-14*	C_n*=8.0E-32;* C_p*=2.8E-31*
GaAs	*1.7E-10*	C_n*=1.6E-29;* C_p*=4.6E-31*
4H-SiC	*1.5E-12*	C_n*=5.0E-31;* C_p*=2.0E-31*

Table 6: Radiative and Auger recombination coefficient for different semiconductor materials [51-52]

2.5.3 Shockley -Read-Hall (SRH) Recombination

The recombination through defects in the bandgap is a process which is the dominant recombination mechanism in semiconductors with indirect forbidden bandgap, such as Silicon and Silicon Carbide.

It results explicitly dependent on the number of imperfections in the crystal, caused by impurities or by crystallographic defects, such as vacancies and dislocations. These imperfections originate intermediate states (see Fig. 23) within the bandgap that act as recombination centers, or traps, for the free carriers. The theory for recombination through these localized traps was for the first time analyzed by Shockley and Read [53] and then by Hall. Their analytical model which describes the recombination rate (SRH-rate) is given by:

$$U_{SRH} = \frac{pn - n_i^2}{\tau_p (n + n_1) + \tau_n (p + p_1)} \tag{2-21}$$

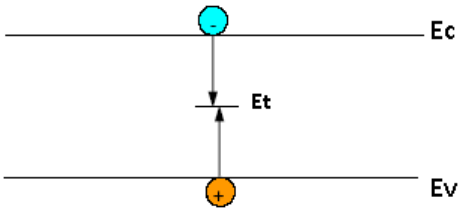


Fig. 23: SRH recombination process

with $n_1 = n_{ie}\, e^{\frac{E_T - E_i}{KT}}$; $p_1 = n_{ie}\, e^{\frac{E_i - E_T}{KT}}$ and $\tau_{n,p} = \left(\sigma_{n,p} v_{th} N_T\right)^{-1}$. Here, E_T and E_i are, respectively, the recombination center and the intrinsic Fermi energy levels; N_t is the recombination center density; v_{th} is the electron thermal velocity, and σ_n (σ_p) is the capture cross section, that is an estimation of how much the electron (hole) must be near to the trap to be captured. Since most of recombination centers are close to the intrinsic Fermi level, Eq. (2.21) can be simplified in:

$$U_{SRH} = \frac{pn - n_i^2}{\tau_p (n + n_i) + \tau_n (p + n_i)} \tag{2-22}$$

For conventional semiconductors, the SRH carrier lifetimes in the above equations are modelled as functions of doping and temperature by the following [54]:

$$\tau_{n,p}^{SRH} = \frac{\tau_{n0,p0}}{1 + \frac{N}{N_{n,p}^{SRH}}} \tag{2-23}$$

where N is the total doping density and the other parameters are fitting values, opportunely chosen for considering the process-dependent factors.

At the present, poor contributes are avoidable in literature focused on the estimations of these values for Silicon Carbide, particularly for

the 4H-SiC polytype. However, although for the intrinsic carrier lifetimes $\tau_{n0,p0}$ there is not a convergence of opinions, for the $N_{n,p}^{SRH}$ parameters it is typically used the extracted value for Silicon [55], i.e. $N_{n,p}^{SRH}$=5x10^{16} cm^{-3}.

2.5.4 Effective Lifetime

With different intensity, depending on the semiconductor topology and technology, all the above recombination mechanisms conjunctly contribute to the final effective carrier lifetime, whose value can be evaluated by the following:

$$\tau_{EFF} = \frac{1}{\tau_{SRH}^{-1} + \tau_{rad}^{-1} + \tau_{Auger}^{-1}} \tag{2-24}$$

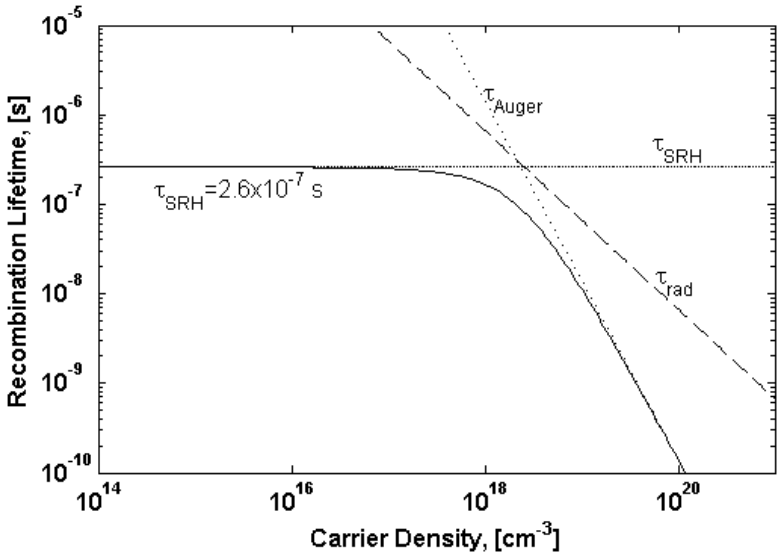


Fig. 24: Recombination lifetime in 4H-SiC as a function of the injection level (solid curve is calculated to fit experimental data extracted from [51])

The 4H-SiC recombination lifetime due to these three components is displayed in Fig. 24: as evident, the Auger recombination is significant only at high carrier densities, while the radiative recombination is completely negligible in Silicon Carbide.

There are several experiments over the past few years [56] conducted for investigating the carrier lifetimes for Silicon Carbide. Since it is an indirect semiconductor, for this material values comparable with those of Silicon are expected in pure crystals, with very low contaminations [57]. At the present, the highest estimated values are up to 2 μs at ambient temperature, which are achieved in thick (40-60 μm) CVD grown epitaxial layers [58].

Because of its high influence on semiconductor performances, the recombination carrier lifetime has been one of the most measured parameters for traditional materials during years. For example, in a pin rectifier, the recombination carrier lifetime is a crucial parameter to predict the performance of the device. In fact, the voltage drop in direct conduction is related to the degree of carrier modulation in the epi-layer, and so it is a function of carrier lifetime and thickness of this region. Therefore, at a given carrier lifetime, a larger epitaxial layer thickness brings to a bigger voltage drop, while a higher carrier lifetime results in better conductivity modulation, with on-state voltage drop approaching the built-in voltage of a $P^{+}N$ junction.

Due to the fragmentary knowledge that actually is available for the Silicon Carbide, the carrier lifetime is still a crucial parameter, especially for monitoring the semiconductor properties and the device operation conditions. So, it must not amaze the intensive effort made by a lots of scientific works to provide accurate measurement methods (one of which is discussed in Chapter 4) for evaluating the carrier lifetime, not only for conventional materials but also for innovative semiconductors, like SiC.

Chapter 3

Modeling of Static Electrical Behavior of 4H-SiC pin Diodes

Since the pin diode is one of the Silicon Carbide devices more promising for its application in power systems, the development of a model that allows to correctly describe its behavior is crucial. In this chapter, our d.c. analytical model was elaborated to predict in detail the forward *I-V* characteristics of Al implanted 4H-SiC pin diodes. The aim of this model is to correlate the material chemical-physical properties to the device electrical behavior. For its peculiarity to disaggregate the minority contributions of the total current, this model aids in better understanding the impact of technological parameters on the steady-state behavior of diodes, besides the role of the above presented physical parameters, such as the band gap narrowing effect, the incomplete doping activation and doping-dependent mobility. In order to analyze the influence of the material properties at different currents and temperatures, the diode total current has been expressed in terms of the minority current contributions in the various diode regions, namely, the highly doped regions, the neutral base and the space charge layer. The accuracy of the model is verified by comparisons with numerical simulations and experimental data in a wide range of currents and temperatures (from 298 K to 523 K).

3.1 Motivation

The development of a new class of high-power SiC-based devices [59-63] imposes the deployment of intensive efforts for a better evaluation of the impact of processing steps on their electrical performances.

Though numerical simulation tools have reached an impressive degree of complexity so that they are essential today to explore the electrical characteristics of devices under specific conditions and verify new structures [64-65], physics-based models remain particularly suited for obtaining meaningful interpretations of the experimental behavior of devices and developing compact models for circuit simulation programs.

Currently, the majority of analytical models used for SiC diodes [66-67] are constructed on the Herlet's model [68], which was originally proposed for the highest current operation of Silicon p-i-n diodes, so there is still a lack in the literature of models capable of describing the *I-V* characteristics of SiC diodes from the lowest to the highest injection regimes and verify the consistency of the various parameter models proposed for this semiconductor. Besides, the modeling of SiC diodes is more complex than other semiconductors because of the higher activation energies of dopants which inhibit their full ionization at room temperature and have a strong impact on the temperature coefficient of the device [69].

Although our d.c. model is derived by one originally used for the analysis of GaAs pin diodes [70], in this work it has been modified to account for the effect of incomplete ionization, doping dependency of carrier mobility and minority carrier lifetime. Moreover, for the first time it has been compared with numerical simulations for checking its ability to account for the role of the various physical parameters. The model is shown capable of describing previously published experimental results [71-73] in the whole range of the examined test conditions and estimating, in agreement with numerical simulations, the contribution of each device region to the total current in a wide range of temperature and injection levels. It is shown that the model formulation can be interpreted in terms of a circuital schematic, which

can turn useful for accurate simulations of diodes including their thermal behavior.

3.2 The *I-V* Analytical Model: Basic Theory

Concerned the analysis of the on-state of a diode, the main complexity for obtaining a closed form expression of the *I-V* curves of power diodes, valid at any bias, is related to the need of accounting for the injection dependence, within the base, of physical parameters such as the carrier mobility and lifetime, when the current varies from the lowest to the highest levels.

By referring to the one-dimensional schematic of diode of Fig. 25 and assuming the charge neutrality condition $n(x)=p(x)+N_B$ valid everywhere in the base outside the space charge region, it is well known that by expressing the electric field as function of the total current:

$$E(x) = \frac{(D_p - D_n)\frac{dp}{dx} + \frac{J_D}{q}}{(\mu_n + \mu_p)p + \mu_n N_B} \tag{3-1}$$

the use of (3-1) in the hole and electron current lead these latter to be written as:

$$J_{P(N)} = \mp qD_a \frac{dp}{dx} + \lambda_{P(N)} J_D \tag{3-2}$$

where $D_a = D_n \frac{2p(x) + N_B}{b[p(x) + N_B] + p(x)}$ represents the ambipolar diffusion coefficient, $b = \mu_n / \mu_p$, $\lambda_P = p/[b(p + N_B) + p]$ and $\lambda_N = \lambda_P(bn/p)$. Note that, when the minority carrier density varies from low ($p<<N_B$) to high injection regime ($p>>N_B$), D_a moves from D_p to $\frac{2D_pD_n}{D_p + D_n}$, whereas λ_P starts to be negligible at low injection level, coherently

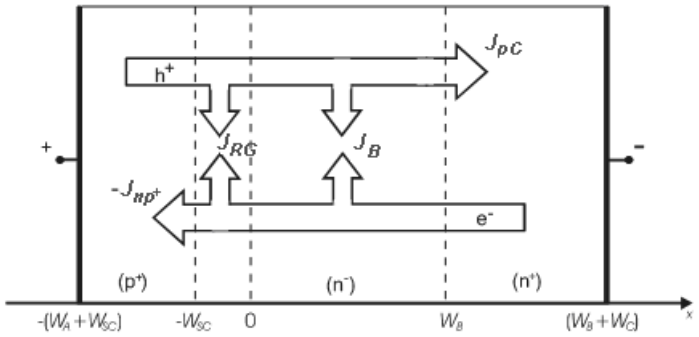


Fig. 25: Electron and hole current components considered in the model

with of the irrelevant role of the electric field, and tends to *1/b* at high injections.

Similarly, by writing the Shockley-Hall-Read recombination in the neutral base as $U = \frac{p}{\tau_a}$, where $\tau_a = \tau_{0p} + \tau_{0n} \frac{p(0^+)}{p(0^+) + N_B}$ [74] is the ambipolar carrier lifetime in the neutral epilayer which comes from assuming the trap level located at the middle of the energy gap, it follows that D_a, λ_P and τ_a are all injection dependent parameters. Therefore, the steady state diffusion equation:

$$-\frac{1}{q}\frac{dJ_P}{dx} = U \tag{3-3}$$

can be solved, along with (3-2), at any injection regime, provided that the spatial derivatives of the three parameters above are considered negligible along the base.

By assuming as independent variable the minority carrier concentration injected at low doped side of P^+N junction ($x=0^+$), namely $p(0^+)$, the quantities D_a, λ_P and τ_a can be treated as injection-dependent constants (through $p(0^+)$) and the solution of the diffusion equation valid at any bias results [75]:

$$p(x) = \frac{p(W_B)\sinh\left(\frac{x}{L_a}\right) - p(0^+)\sinh\left(\frac{x - W_B}{L_a}\right)}{\sinh\left(\frac{W_B}{L_a}\right)} \tag{3-4}$$

where $L_a = \sqrt{D_a \tau_a}$ represents the injection dependent-ambipolar diffusion length.

The hole concentration $p(W_B)$ in (3-4) can be calculated exploiting the electron and hole current balance at the two extremities of the base, namely at $x=0^+$ and $x=W_B$, according to the following expressions:

$$qD_a \left.\frac{dp}{dx}\right|_{x=0^+} + \lambda_{P(N)}\Big|_{x=0^+} J_D = J_{np^+}(0^-) + J_{RG} = J_{nA} \tag{3-5a}$$

$$-qD_a \left.\frac{dp}{dx}\right|_{x=W_B} + \lambda_{P(N)}\Big|_{x=W_B} J_D = J_{pC}(W_B) \tag{3-5b}$$

where:

$$J_{RG} = qW_{SC}\frac{n_i}{2\sqrt{\tau_{0n}\tau_{0p}}}\left[e^{\left(\frac{V_{pn}}{2V_T}\right)} - 1\right] \tag{3-5c}$$

is the recombination current [76] inside the space charge region of width $W_{SC} = \sqrt{\frac{2\varepsilon(V_{bi} - V_{pn} - 2V_T)}{qN_B}}$ [34], being V_{pn} the fraction of the applied voltage falling across P^+N junction and, finally, J_{np^+} and J_{pC} represent the minority currents injected into the anode and cathode respectively:

$$J_{np^+}(0^-) = qS_{P^+}p(0^+)\left[1 + \frac{p(0^+)}{N_B}\right] \tag{3-6}$$

$$J_{pC}(W_B) = qS_{N^+}\,p(W_B)\left[1+\frac{p(W_B)}{N_B}\right] \tag{3-7}$$

where:

$$S_{P^+} = \frac{D_{nA}}{L_{nA}}\frac{N_B}{N_{aA}^-}\exp\left(\frac{\Delta E_{gA}}{kT}\right)\coth\left(\frac{W_A}{L_{nA}}\right) \tag{3-8a}$$

$$S_{N^+} = \frac{D_{pC}}{L_{pC}}\frac{N_B}{N_{dC}^+}\exp\left(\frac{\Delta E_{gC}}{kT}\right)\coth\left(\frac{W_C}{L_{pC}}\right) \tag{3-8b}$$

represent the effective recombination velocities associated to the anode and cathode [77], and all the other symbols having their usual meaning.

It must be noted that, expressing the exponential term in (3-5c) at any bias in term of $p(0^+)$, according to the junction law $V_{pn} = V_T \ln\left(\frac{p(0^+)N_B}{n_i^2}\right)$, and using (3-4) in (3-5a) and (3-5b), the total current J_D can be eliminated from these latter to obtain an expression of the ratio $p(W_B)/p(0^+)=Y$ in the form $Y^3 + aY^2 + bY + c = 0$. It can be analytically solved to obtain the relation existing between the minority carrier concentrations at the base region edges ($p(W_B)$ as a function of $p(0^+)$), as shown in *Appendix B*.

3.2.1 *J-V* Characteristics

To better investigate the physical operation of SiC diodes, instead of calculating J_D through the gradient of (3-4), it is convenient to estimate J_D as sum of its contributions according to the schematic of Fig. 25:

$$J_D = J_{nA}(0^+) + J_{pC}(W_B) + J_B = J_{np^+}(0^-) + J_{RG} + J_{pC}(W_B) + J_B \tag{3-9}$$

where J_B represents the recombination current inside the base neutral region:

$$J_B = q\int_{0^+}^{W_B}\frac{p(x)}{\tau_a}dx = q\frac{L_a}{\tau_a}\left[p(0^+)+p(W_B)\right]\frac{\cosh\left(\frac{W_B}{L_a}\right)-1}{\sinh\left(\frac{W_B}{L_a}\right)} \qquad (3\text{-}10)$$

and the other current components have been described before.

In a similar manner, the applied diode voltage bias, V_D, can be expressed as the sum of the following four contributions:

$$V_D = V_{pn} + V_{nn+} + \int_{0^+}^{W_B} E(x)dx + (R_{p+} + R_{n+} + R_S)J_D \qquad (3\text{-}11)$$

where V_{pn} is the already mentioned junction voltage, $V_{nn+} = V_T \ln\left(1+\frac{p(W_B)}{N_B}\right)$ describes the voltage across the NN^+ junction [78], R_{n+} and R_{p+} represent the specific resistance of the terminal regions, namely $(q\mu_{n^+(p^+)}N_{dC(aA)})^{-1}W_{C(A)}$, R_S accounts for the contact and external parasitic resistances, and finally the voltage across the base can be written from (3-1) as:

$$\int_{0^+}^{W_B} E(x)dx = V_T \ln\left(\frac{p(0^+)+\frac{b}{b+1}N_B}{p(W_B)+\frac{b}{b+1}N_B}\right)^{\frac{b-1}{b+1}} + R_B J_D \qquad (3\text{-}12)$$

being R_B the injection-dependent resistance of the modulated base (see *Appendix C*).

The sequence of calculations to obtain the J_D-V_D curve at a given temperature is sketched in the flow chart of Fig. 26: for a given V_{pn}, once the effective recombination velocities S_{P^+} and S_{N^+} are evaluated

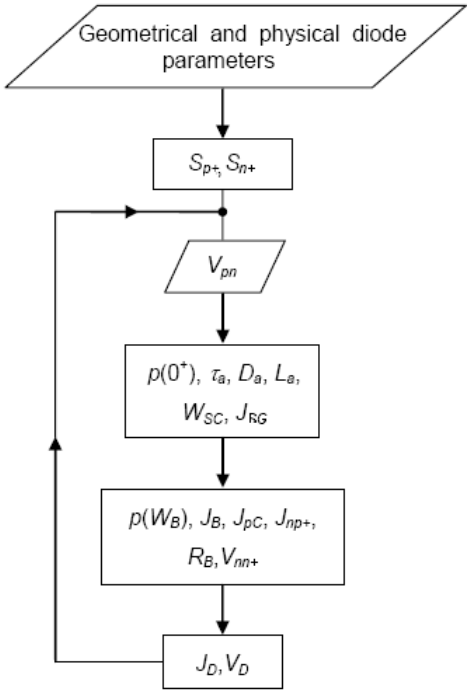


Fig. 26: Flow chart of the static analytical model

from (3-8), the $p(0^+)$-dependent parameters τ_a, D_a and L_a are evaluated, and subsequently used in the third-order polynomial to obtain $p(W_B)$ as function of $p(0^+)$. Hence, the values of the various components of (3-9) and (3-11) are calculated. So, our model reveals useful for intuitive and methodical circuit analysis: in fact, it must be noted that the J_D-V_D calculation can be also represented by means of the schematic Fig. 27, where J_{RG} coincides with (3-5c), while the current and voltage dependent sources, J_{DIF} and V_{DIF}, both controlled by the junction voltage V_{pn}, are given by:

$$J_{DIF} = J_B + J_{pC}(W_B) + J_{np^+}(0^-) \qquad (3\text{-}13a)$$

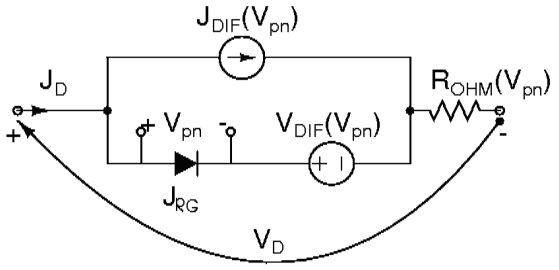


Fig. 27: Equivalent steady-state schematic of the diode model

$$V_{DIF} = V_T \ln\left[\left(\frac{p(0^+)+\frac{b}{b+1}N_B}{p(W_B)+\frac{b}{b+1}N_B}\right)^{\frac{b-1}{b+1}}\left(1+\frac{p(W_B)}{N_B}\right)\right] \qquad \text{(3-13b)}$$

and, finally, $R_{OHM}=R_{p+}+R_{n+}+R_S+R_B$ represents the cumulative effects of the resistances in (3-11).

It is interesting to observe that the resistive drops like R_{p+} and R_{n+} are not trivial in bipolar device like pin rectifiers because of significantly high current densities that typically flow through these devices, as compared to majority carrier devices like Schottky diodes.

3.2.2 Doping and Temperature Dependencies of Physical Parameters

The calculation of the J_D-V_D curves requires the knowledge of a number of doping dependent parameters, some of them are not predictable being strictly process-dependent, as carrier lifetime and the diffusion length, whereas others, as the apparent bandgap narrowing and carrier mobilities, are less uncertain being strictly related to the crystalline structure and the activated doping level.

In our analysis the diffusion constants D_a, D_{nA} and D_{pC}, along with respective diffusion lengths L_a, L_{nA} and L_{pC}, can be calculated through the Caughey and Thomas mobility model and the Einstein relation: $D = \mu V_T$. Besides, using the equations (2-6) and (2-7), the electron and hole mobilities have been modelled as in [39-43] for SiC.

By neglecting the Auger recombination rate, which is in particular not significant for 4H-SiC power devices operated at high temperatures [79], it has been assumed for the carrier lifetimes, in all the regions, the Shockley-Read-Hall phenomenon as the prevalent recombination mechanism, so that the doping dependence of these parameters follows the expression reported in Eq. (2-23), with $N_{n,p}^{REF} = 5\text{x}10^{16}\text{cm}^{-3}$.

Finally, as shown in the previous chapter, for the Silicon Carbide the doping concentration cannot be assumed in principle fully activated, due to the higher activation energy of the acceptors and donors in the material. This contributes to increase the diode series resistance and make more complex the calculation of the active-doping-dependent quantities, such as the apparent bandgap narrowing: referring to the models already presented, these phenomena are also keep in count in our static analysis.

3.3 Model Validation

The reliability of the static model is evaluated through a direct comparison with numerical and experimental results obtained by referring to the diode structures with characteristics summarized in Table 7.

	Theoretical (#1)			***Experimental (#2)***		
Region	***Anode***	***Base***	***Cathode***	***Anode***	***Base***	***Cathode***
Width (μm)	*5*	*10*	*30*	*1.2*	*5*	*300*
Doping (cm^{-3})	*1E20*	*1E14*	*5E20*	*6E19*	*3E15*	*5E19*
Active doping $N_{aA,dC}^{-,+}$ (cm^{-3})	*7.04E17*		*1.61E19*	*5.45E17*		*4.98E18*
Bandgap narrowing $\Delta E_{gA,C}$ (meV)	*27.2*	-	*122.9*	*25.2*	-	*79.7*
Effective doping N_{eff} (cm^{-3})	*2.44E17*	*1E14*	*1.35E17*	*2.04E17*	*3E15*	*2.21E17*
Effective recombination velocity S_{P^+,N^+} (cm s^{-1})	*28.87*	-	*245.95*	*1.61E4*	-	*4.34E3*
Carrier Lifetime (ns)	τ_n=*25E-2*	τ_{0n}=*500* τ_{0p}=*100*	τ_p=*1E-2*	τ_n=*8*	τ_{0n}=*15* τ_{0p}=*15*	τ_p=*15E-3*
Specific resistance $R_{n+,p+}$ (Ωcm^2)	*8E-5*	-	*2.72E-5*	*2.2E-6*	-	*7E-4*
Parasitic resistance R_{EXT} (Ωcm^2)	-			*2.5E-3*		

Table 7: Geometrical and physical parameters for the device #1 and the device #2, at ambient temperature

As it will be shown in the following subsections, the analytical model permits to assert that, because of the relatively thin epilayers of the under test devices, the total current (3-9) of pin diodes at highest levels is mainly determined by the currents injected in the terminal regions and therefore the quantities S_{P^+} and S_{N^+} become determinant for the validity of whole model. In our analysis an accurate derivation of such terms is assured through the use of equations (3-8a) and (3-8b), where also the complex dependence of the total doping and of its active value through the bandgap narrowing is considered. In Fig. 28 is displayed, at different temperatures, the effect related to a potential missed inclusion of this dependence in the above mentioned equations.

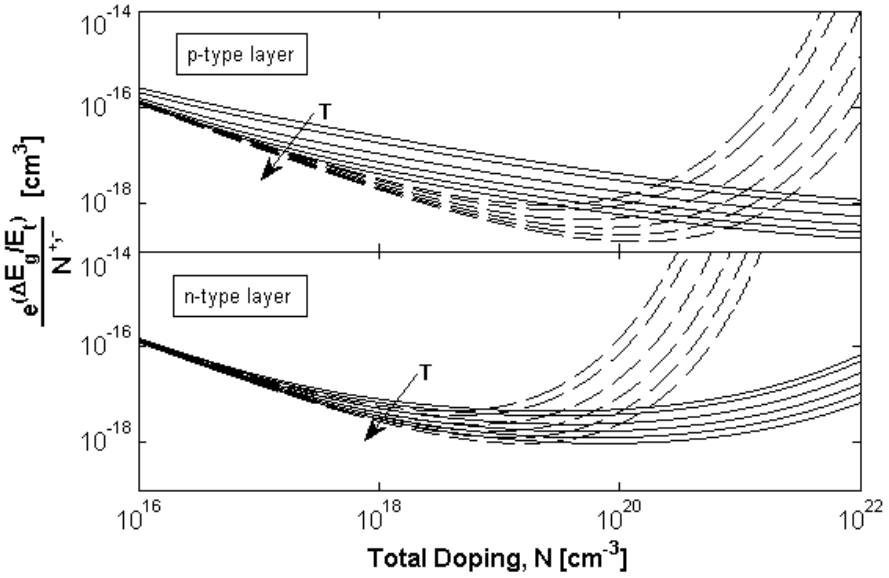


Fig. 28: Behaviour of the exponential term in Eqs. 3-8 vs total doping at different temperatures (from 298K to 523K), with the inclusion of the incomplete ionization effects (solid lines) or less (dashed lines)

3.3.1 Simulation Results

To highlight the accuracy of the model in describing the carrier transport at the two P^+N and NN^+ interfaces for a wide range of parameter values, the model has been compared to numerical simulations [80] carried out on the diode structure named #1 in Table 7. The impact of changing the electrical characteristics of the material was included in the analysis by using two different set of values for τ_{0n} and τ_{0p} in the relation (2-23), and by imposing, for each lifetime value, alternatively or in conjunction, $\Delta E_{gA,C} = 0$ (no bandgap narrowing) and $\xi = 1$ (complete ionization) in Eq. (2-14) and (2-10). For reader convenience, the resulting values of active N_{dC}^{+} (N_{aA}^{-}) and effective doping (N_{eff}) in the heavy doped regions are also reported in Table 7.

It is interesting to observe that, as expected from the considerations done in section 2.3, due to the higher activation energy of acceptors, less than 1% of them is activated (ξ_A=0.007) at ambient temperature, leading to a relatively low active doping level, precisely of the order 10^{17} cm^{-3}, and to a negligible bandgap narrowing effect inside the anode. Although this final value does not differ too much from the saturation level of N_{eff} which should result in the case of a fully activated anode doping, so that the effects of incomplete ionization and bandgap narrowing are, in principle, indistinguishable at ambient temperature, the temperature dependence of the *I-V* curve is expected to be significantly different in the two cases due to the exponential behavior of the apparent bandgap narrowing. Besides the significant agreement of curves, it is interesting noting in Fig. 29 both the premature down bending of the curves in the case $\xi \neq 1$, due to the higher series resistance determined by incomplete ionization, and the higher sensitivity of the *I-V* curves to the physical properties of the terminal regions at higher lifetime, as consequence of the reduced relevance of the recombination current in the base (3-10).

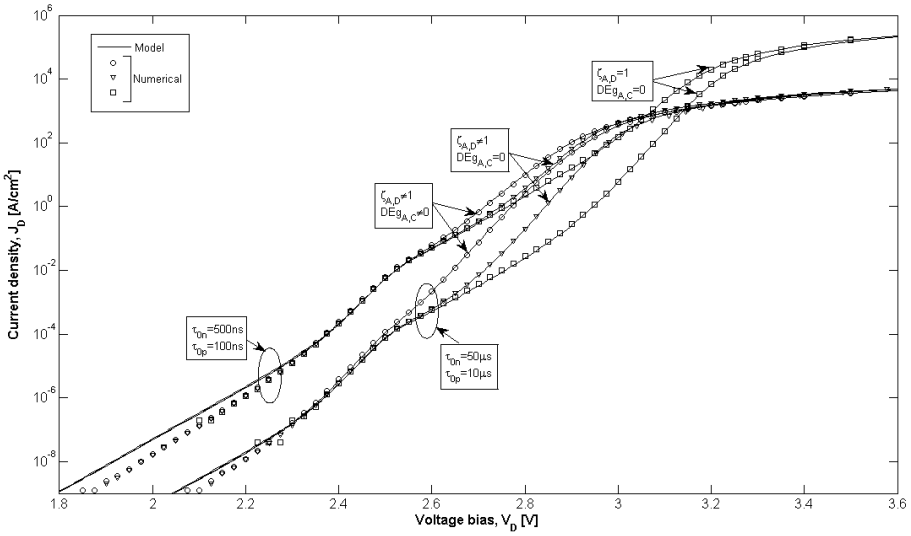


Fig. 29: J_D-V_D curves of devices #1 in Table 7, for two different τ_{0p} and τ_{0n} lifetime values, showing the effect of the bandgap narrowing and the partial activation in the terminal regions

This latter behavior can be better explained in Fig. 30 where, for the same structure #1, the total current J_D is plotted together with the minority current components J_{nA} and J_{pC}, at two different temperature values, assuming for the bandgap the temperature dependence proposed in Eq. (2-1). Here, the plot of the recombination component J_B has been omitted for clearness, although it can be obtained as difference from the other ones.

At lowest biases, namely below 2 Volt, the dominant component is the recombination current J_{RG} (3-5c) as shown by the $1/2V_T$ slope of the J_{nA} curve at this regime, whereas J_B (3-10) tends to dominate at increasing voltage and leads the total current to be strongly influenced by the carrier lifetime in the base.

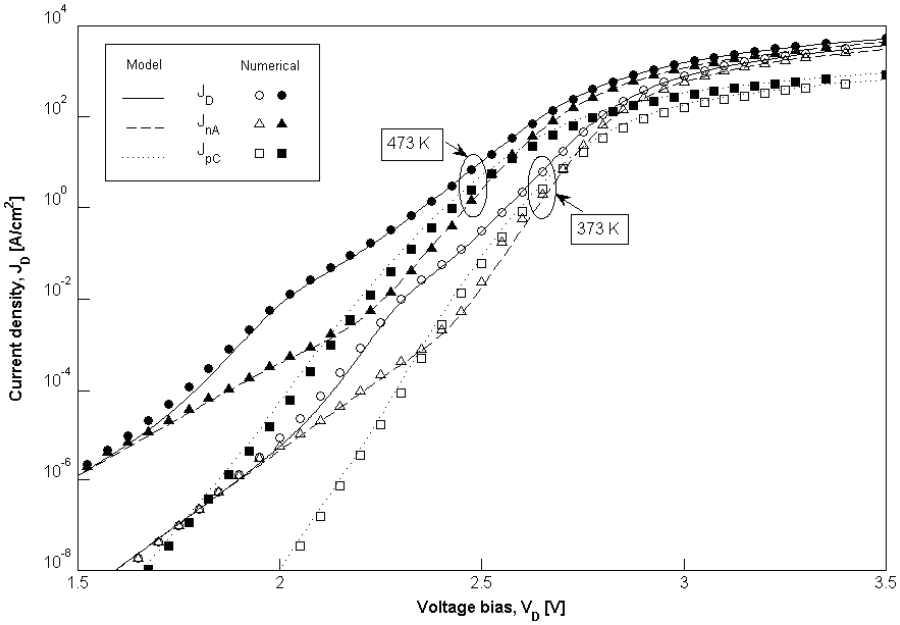


Fig. 30: Plots of J_D-V_D theoretical and simulated curves at T = 373K and 473K for the device #1 in Table 7

At voltage higher than 2.6 Volt, the minority carrier injection currents in the terminal regions become significant for conduction and, for diode biases above 2.9 Volt, the electron component J_{np+} of (3-6) dominates in the total current.

The relative weight of the current components does not change at higher temperatures and the current component J_{nA} continues to dominate at high current densities as consequence of the higher activated doping in the N^+ region which tends to suppress the hole injection in the substrate and to enhance the electron injection in the anode.

3.3.2 Experimental Results

For a complete analysis, the presented model has been also compared with the measured and simulated J_D-V_D curves of the experimental diode #2 reported in Table 7, in a wide range of temperature and current. The under test diode, fabricated by the IMM-CNR of Bologna-Italy, belong to a class of devices which are subject to a realization process schematized in Table 8. Briefly, the anode regions were realized by Aluminum implant to obtain a *SIMS* peak value of $6x10^{19}$ cm^{-3} onto 5µm-thick and $3x10^{15}$ cm^{-3}-doped epilayers, grown on 300µm-thick and $5x10^{19}$ cm^{-3} nitrogen-doped substrates, with an active area of 10^5 μm^2. A schematic cross-section of the diode structure and the net doping profile are displayed in Fig. 31.

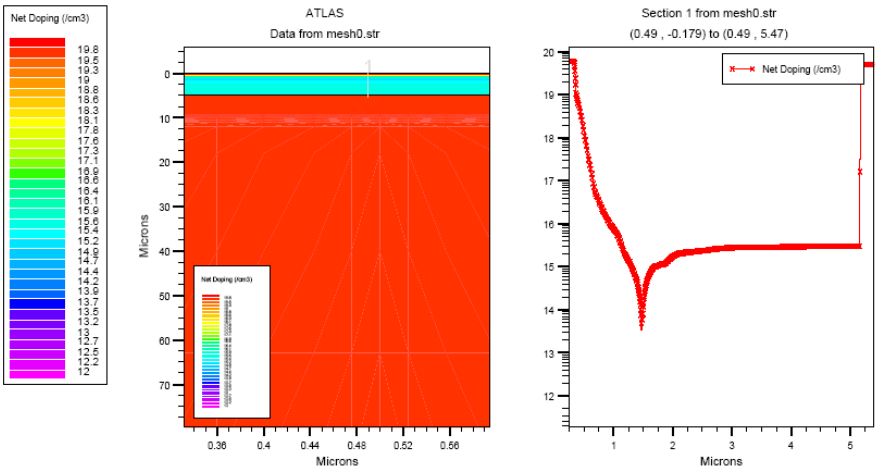


Fig. 31: Cross-section (left) and net doping profile (right) of the 4H-SiC samples

Process	*Description*
Washing	-Boiling trichloroethylene for 5 minutes -Boiling acetone for 5 minutes -Boiling isopropyl alcohol for 5 minutes -Piranha for 5 minutes -HF:H_20-1:10 for 30 seconds
Photolithograph	-Photoresist modeling on the top of wafer by exposition through a mask at UV light
Attacks	-Pattern transfer on the sample surface by Reactive Ion Etching (RIE) -Photoresist cleaning
Washing	RCA washing
Deposition	-Chemical Vapor Deposition (CVD) densification on the top of sample of an oxide layer of 0.4um thick -At the top of wafer, sputter deposition of 1.2um-Al layer (with 1% of Si)
Photolithograph	Photoresist modeling for the transfer of the implantation mask on the surface of the Al-layer and UV radiation
Attacks	-Attack of the Al layer by Alu Etch (composed of acetic acid, ortophosphor acid and nitric acid) for modeling the implantation mask on it -Photoresist cleaning
Implantation	At the top of wafer, implantation at 400°C, according to the following scheme: Energy [keV] — Dose [Ions/cm^2] 250 — 7.2E14 350 — 1.5E15 Corresponding to an approximate flat profile, with 0.2um depth and 6E19cm^{-3} as maximum density
Washing	-Elimination of mask layer of Aluminum by Alu Etch -Elimination of oxide layer by HF:H_20-1:5 for 15 minutes -Piranha for 5 minutes -HF:H_20-1:10 for 30 seconds -RCA washing for preparing the surface at heat treatment
Annealing	At 1600°C for 30 minutes, with 40°C/s ramp, in Ar environment (JIPELEC furnace)

Attacks	Removal of 40nm superficial layer from the top of samples by RIE
Washing	-Piranha for 5 minutes -HF:$H_2$0-1:10 for 30 seconds
Deposition	-Sputter deposition of Ti-layer with 0.08um thick on the top of samples -Deposition of Al-layer (with 5% of Si) with 0.350um thick on the top of layer
Photolithograph	-Photoresist modeling for the transfer of the metallization mask on the surface of previously deposited metallic layers -UV illumination
Attacks	-Attack of surface for modeling the previously deposited metallic layers by: - Alu Etch, for Aluminum - HF:$H_2$0-1:10 for 30 seconds, for Titanium -Photoresist removal
Deposition	Electron beam physical vapor deposition of a 0.3um-layer of Nickel, on the back of sample
Annealing	Samples annealing at 1000°C in vacuum, for 2 minutes

Table 8: Fabrication processes of the SiC samples

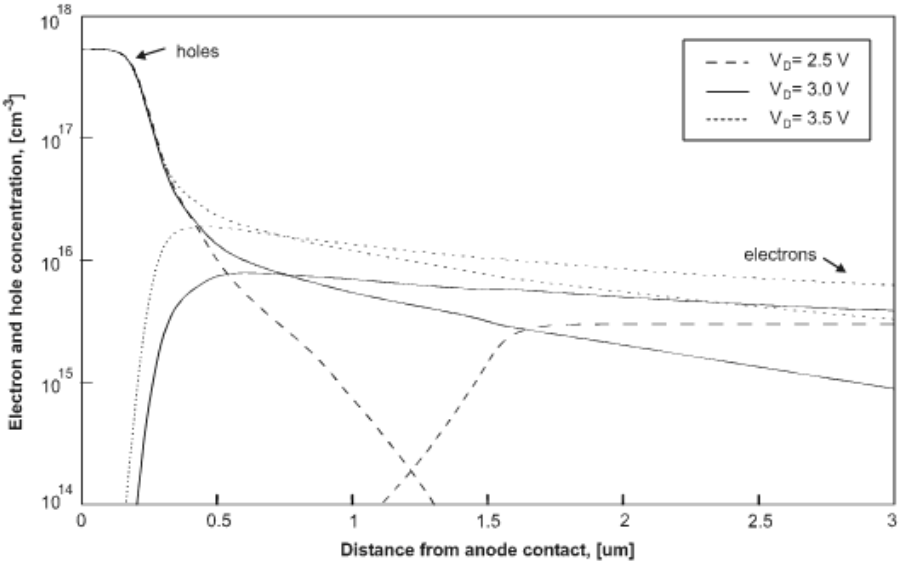


Fig. 32: Electron and hole concentration profiles at three distinct anode voltages for device #2 in Table 7

To avoid the use of any fitting parameter in the model, the τ_{0n}, τ_{0p} terms present in Eq. (2-23) have been set equal to the value of 15 ns measured on similar structures by reverse recovery in [72] and by OCVD measurements in [81]. The role of the carrier injection in device #2 is highlighted in Fig. 32 where the numerical simulations of the electron and hole distributions calculated along the base region are shown for three distinct applied voltages. Due to the lower lifetime compared to device #1, a significant carrier injection starts to manifest into the base at bias voltages around 3 Volt and the base becomes filled of the electron-hole plasma at voltages around 3.5 Volt.

The *J-V* curves of device #2 for a wide range of currents and temperature are shown in Fig. 33 using a half-logarithmic scale, while the behaviour at higher voltages is plotted in Fig. 34, in linear scale.

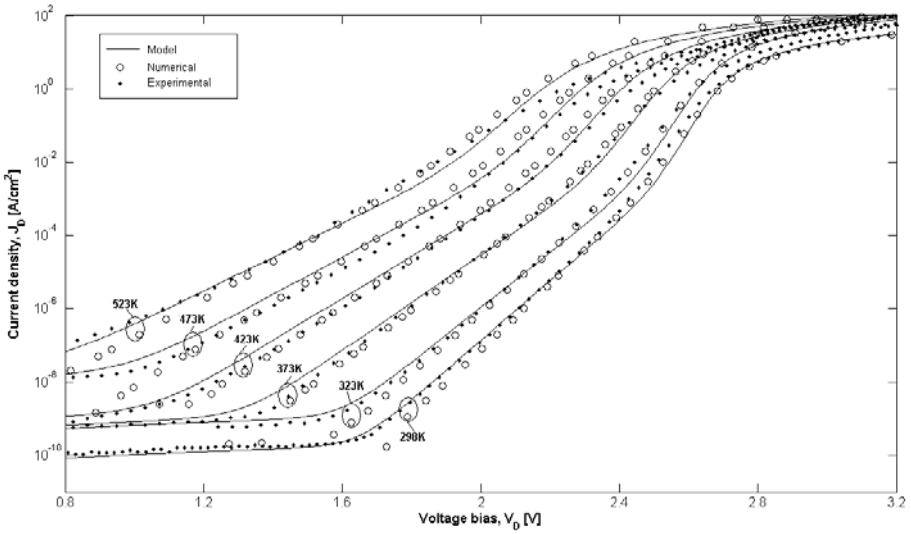


Fig. 33: Comparison between J_D-V_D analytical and numerical curves at different temperatures for devices #2 in Table 7

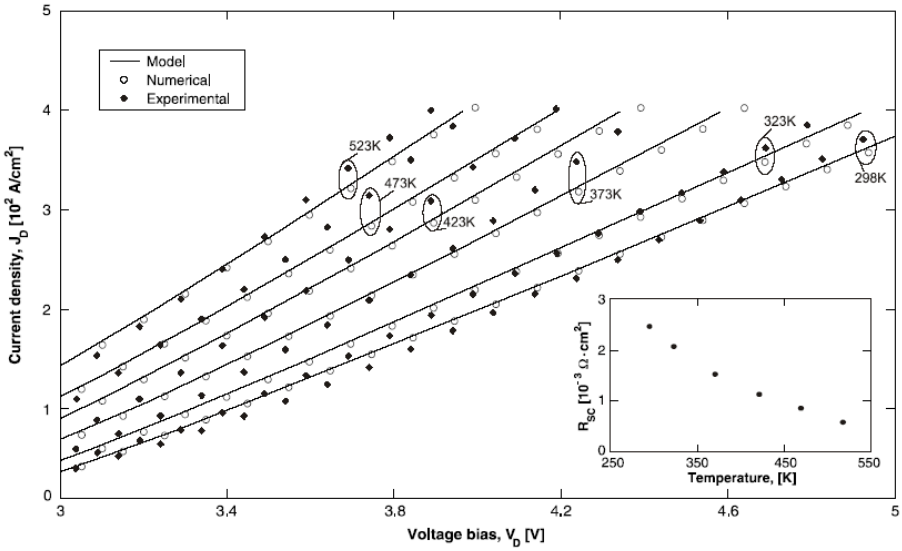


Fig. 34: Comparison between J_D-V_D analytical, numerical and experimental curves at different temperatures for devices #2 in Table 7 at high currents

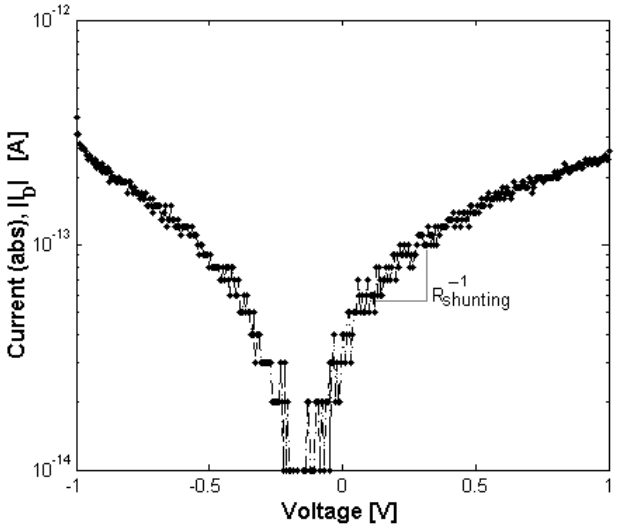


Fig. 35: Shunting resistance detected in the *I-V* characteristics of the sample diode

The used measurement equipment is substantially based on the employment of a HP4155B semiconductor parameter analyzer and a hot-plate to increase the temperature. Although the HP instrument is characterized by an output/measurement range of 100V/1A, a current limit of 400 A/cm^2 was imposed during the measurements to avoid excessive self-heating of the device, encapsulated in a *TO32* metal case and contacted with a 25 μm size-Al wire.

In the whole range of temperatures, from 298 K to 523 K, the analytical and numerical behaviours are in good agreement with the experimental data over several current decades. Note that, to better fit the lowest current branch of the measured curves in Fig. 33, behaving similarly as in [82], a leakage current due to a shunt resistance has been added in (3-9): its measured value at ambient temperature results of 10 TΩμm^2, as displayed in Fig. 35. Finally, in order to describe the curves at currents higher than 10 A/cm^2, the $R_S = R_{SC} + R_{EXT}$ resistance in Eq. (3-11) has been used as a unique adjusting parameter, both in the model and numerical simulations, to account for the temperature dependent contact resistance R_{SC} [69] and the parasitic contribution R_{EXT}.

Using for R_{EXT} the estimated value of 2.5×10^{-3} Ωcm^2, mainly due to wiring and soldering, the R_{SC} values found at the various temperatures are reported as inset in Fig. 34, showing a decrease by a factor of 5 [83] from ambient temperature to 523 K.

Besides the good agreement between model and simulations at any bias and temperature, it is interesting noting that, as the temperature increases, the *I-V* characteristics shift left and up, an explicit effect of the temperature dependence of the intrinsic carrier concentration n_i, which is fundamental in the calculation of the total voltage (3-11) and the current components in (3-9). The slope of the analytical and numerical curves slightly differs at the lowest currents, where the current component J_{RG} dominates. This should be related to the model assumption of a uniform doping density in the anode, which affects the amount of charge depletion width and hence the value of the current component (3-5c).

With the aim to give a more evidence to the versatility of our static model for investigating the behaviour in forward conduction of a diode with arbitrary geometrical and physical characteristics, we have been also applied the analytical results on already published 4H-SiC diodes. In detail, the comparison has been made respect to the numerical and experimental data presented in [73] and it is shown in Fig. 36.

The device under study is realized with a circular geometry of 500-μm diameter and exhibits a drift region with a width and doping of 50μm and $8x10^{14}$ cm^{-3}, respectively; the anode and cathode regions are both characterized by a doping of 10^{18} cm^{-3} at ambient temperature. Besides the information related to the device structure, note that also the 4H-SiC parameters and physical models have been set in our model for a tuning with the reported simulation results. Specifically, according to [73], the temperature dependence of τ_{0n} and τ_{0p} is also evaluated, while material parameters, carrier mobility model with doping and temperature dependencies and minority carrier lifetime have been keep consistent with reference [84], cited by [73]. Finally, the discussed earlier models for incomplete ionization and bandgap narrowing effects are still valid.

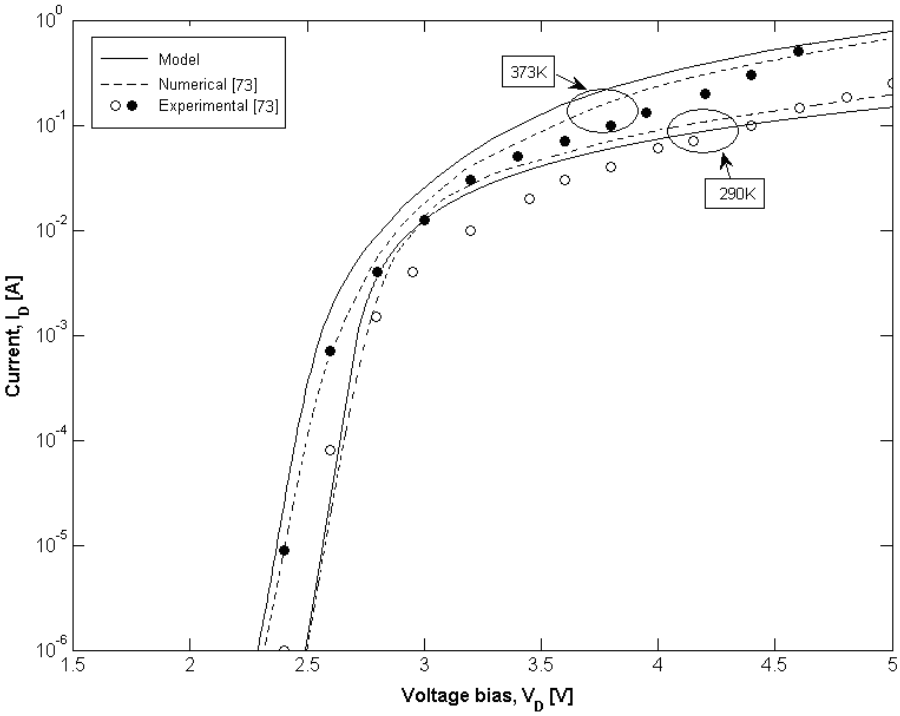


Fig.36: I_D-V_D characteristics calculated by our dc model are compared with experimental and numerical data provided in [73]

Due to the unavailability of other information related to the fabrication conditions, which are not included in [73], it is clear that the use of our model turns out a valid tool for an in depth investigation of otherwise unknown aspects: in this particular case, for example, the model suggest us that for obtaining a good match with simulated and measured data, P^+ region is characterized by a doping with a deep ionization energy level (of about 330 meV), probably attributable to the use of boron as acceptor.

Chapter 4

Modeling of Dynamic Electrical Behavior of 4H-SiC pin Diodes

In this chapter we describe our study on the dynamic electrical behavior of the 4H-SiC diodes. In particular, the purpose is to point out the physical causes that give rise to an abrupt variation of diode voltage due to an instantaneous interruption of the conduction current: although this situation is notably interesting for the study of the switching behavior of diodes, it is also traditionally used to extract more information about physical parameters, like the mean carrier lifetime. This occurs for example in the conventional *Open Circuit Voltage Decay* (*OCVD*) technique, where the voltage decay due to the current interruption is useful for an indirect measure of minority carrier lifetime in the epitaxial layer. Because of still existent uncertainty about carrier lifetime in the Silicon Carbide epi-layers, the OCVD method reveals itself a valid tool for monitoring this essential parameter.

Since a general dynamic model must incorporate an accurate description of the static *I–V* curves to properly account for the steady-state conditions of the device, the analytical model presented in the previous chapter represents a reliable starting point for modeling the dynamic electrical behavior of SiC pin diodes, being in this case the steady state injected carriers in the various regions a priori known.

With this in mind, we have developed a self-consistent model that, exploiting an improved method of the conventional OCVD technique, is able to predict, for a generic diode under test switched from an

arbitrary forward-bias condition, the spatial distribution of the majority and minority carrier lifetimes, besides the spatial minority carrier distribution in the epitaxial layer, at any injection regime.

Thanks to its versatility, the proposed model results a valid tool to individuate the proper measurement conditions for a given structure and to analyze the features of the OCVD response of the devices. In fact, it allows of resolving some ambiguities reported in the literature, such as the stated inapplicability of the OCVD technique on thick epilayers, the reasons of the observed nonlinear decay of the voltage with time, and the effects of junction properties on voltage transient.

The initial part of the chapter is focused on the traditional OCVD method: the basic theory of the technique is discussed in order to better introduce the measurement method on which is based the analysis for the extraction of carrier lifetime in SiC epilayers. After a detailed description about the developed model, comparisons with simulations and experiments are presented: they highlight the model accuracy for predicting the spatial–temporal variation of carriers and currents along the whole epilayer. With the imposition of right boundary conditions, it is finally shown how the developed model turns useful for extending the analysis and obtaining a physical insight respect to any arbitrary switching condition, such as in the case of the *Reverse Recovery* (*RR*) response.

4.1 Traditional Open Circuit Voltage Decay (OCVD) Method

Because of its influence on semiconductor performances, the recombination lifetime has been one of the most measured parameters during years. In the past, the great interest about it has provided many measurement techniques, which are been continuously improved also thanks to the availability of more accurate commercial equipments. Among these, the OCVD technique was presented for the first time in the 1955 [85], showing itself a useful method for extracting the recombination lifetime of minority carrier in the bulk of processed wafer, by observing the voltage decay, *V(t)*, across the junction diode when the polarization current is abruptly switched-off at a generic t_0 time, as displayed in Fig. 37 where the measurement arrangement is schematized.

A typical measured OCVD curve is reported in Fig. 38: here, after an ohmic drop due to an internal resistance, the voltage shows a behavior with the time at the first linear and then exponential.

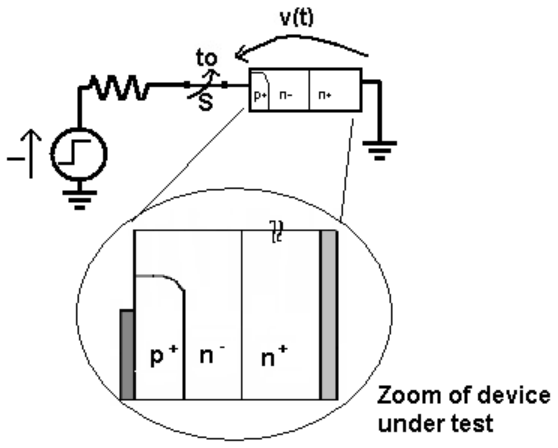


Fig. 37: Test structure schematic for OCVD measurements

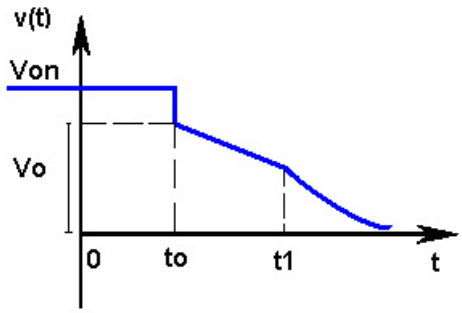


Fig. 38: Typical Open Circuit Voltage Decay curve

The slope of the linear variation results in an electrical measurement of the effective carrier lifetime. In fact, since in a directly polarized P^+N junction the internal current is dominated by the hole flow injected by the *n* region, defined p_0 and Δp respectively as the hole concentration at equilibrium and in excess, in the *n* region results:

$$p_n = p_0 + \Delta p = \frac{n_i^2}{n_n} + \Delta p \qquad (4\text{-}1a)$$

Contextually, from the junction theory, it can be assumed that the minority carrier density varies exponentially with the voltage:

$$p_n = p_0 e^{\frac{V(t)}{\eta V_T}} \qquad (4\text{-}1b)$$

Equalizing the (4-1a) and the (4-1b), results:

$$V(t) = \eta\, V_T \ln\left(1 + \frac{\Delta p}{p_0}\right) \qquad (4\text{-}1c)$$

With the assumption that the excess of minority carrier concentration decays exponentially according to the factor τ_{EFF}, it can be written:

$$\Delta p = \Delta p_0 \; e^{-\frac{t}{\tau_{EFF}}} \tag{4-2}$$

where Δp_0 is the hole concentration in excess at the time t_0. Evaluating the voltage in $t=t_0$, through the (4-1c), results:

$$V(t_0) = V_0 = \eta \; V_T \ln\left(1 + \frac{\Delta p_0}{p_0}\right) \tag{4-3}$$

and with the use of previous equations, the voltage becomes:

$$V(t) = \eta \; V_T \ln\left[1 + \left(e^{\frac{V_0}{\eta V_T}} - 1\right) e^{-\frac{t}{\tau_{EFF}}}\right] \tag{4-4}$$

For small values of t/τ_{EFF} and with $V_0 >> V_T$, the above equation becomes:

$$V(t) = V_0 - \eta V_T \frac{t}{\tau_{EFF}} \tag{4-5}$$

Considering that in the time interval $[t_0, t_1]$ the voltage decays linearly, the following expression can be written:

$$\tau_{EFF} = -\eta V_T \left(\frac{dV}{dt}\right)^{-1} \tag{4-6}$$

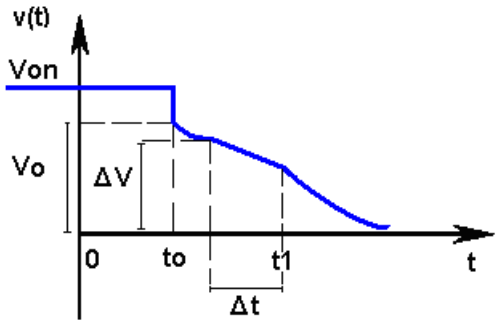


Fig. 39: Typical OCVD curve at high injection levels

with $\eta = 1 + \frac{p_n}{p_n + N_B}$ varying from 2 to 1 when the voltage diode decays from high to low injection levels. In obtaining the Eq. (4-6), the effect of carrier recombination in the space charge region (SCR) have been neglected; therefore, assuming that *V(t)* is the voltage across the only SCR region, i.e. neglecting the ohmic drop across the diode before the current switching-off, the Eq. (4-6) allows to directly calculate the recombination lifetime.

It must be noted that this relation is derived by (4-1b): this last expression is valid under the assumption of low or medium injection levels; consequently, the (4-6) is workable for the measurement of carrier lifetime just when the current level is suitably chosen to guarantee these injection regimes.

In the case of high injection levels, the voltage decay will be characterized by a behavior similar to that sketched in Fig. 39: here, after a "hump", there is the region where the minority carriers can be neglected respect to the majority carriers, so that the carrier lifetime can be expressed as:

$$\tau = -\left[\frac{1}{\eta V_T}\frac{\Delta V}{\Delta t}\right]^{-1} \qquad (4\text{-}7)$$

4.2 Why a New OCVD Model

The standardization of the OCVD method has converted the initial difficulties in performing measurements into the much more difficult interpretation of the experimental results.

In this perspective, although the Open Circuit Voltage Decay method is very old [85], it must be noted that almost all the OCVD models available in the literature [86-87] are limited either to high or low injection regime of diodes. Therefore, they are quite inadequate to provide an accurate insight of the electrical behaviour of the devices due to their inability of describing the full transient of OCVD measurements, namely from the current switching-off instant to the asymptotic zero voltage condition.

Moreover, in spite of the numerous mathematical approaches [87-89] for modelling the OCVD behaviour of Silicon devices, their accuracy to predict the spatial-temporal distributions of carriers and currents along the semiconductor layer has never been verified by numerical simulations, mainly because more attention has been reserved to the transient of the carrier density at the junction border, which is directly related to the decay of the diode voltage. That occurs for example in the recent work [90], where the OCVD-based measurement method proposed in [91-92] has been modelled by assuming uniform the lateral carrier distribution in the epilayer, thus ignoring the effect of the epilayer boundaries.

From the above considerations, it is evident that the weakness noticeable in the OCVD modelling of Silicon devices makes uncertain the extension of this method to novel materials, like the Silicon Carbide.

At the present, due to the attractiveness of the electrical properties related to 4H-SiC material for power applications, in literature the majority of the OCVD analysis carried out on SiC devices [93-94] are limited to their high injection operation and cannot be employed for an exhaustive interpretation of their transient behaviour at any injection regime.

Recently, it has been shown in [95] that a number of contradictions appear when the minority carrier lifetime of SiC is measured by Reverse Recovery or OCVD technique or, even, extracted from *I-V* curves. These contradictions should originate from the existence of a thin layer, located near to the metallurgical junction and with a very low lifetime, which speeds up the reverse recovery of diode without influencing the OCVD response, being this latter related to the bulk lifetime of the epilayer.

In [91], by presenting a novel OCVD-based measurement technique, it has been shown that more information can be achieved from the OCVD method if the analysis is not restricted, as solely occurs, to the temporal interval where the diode voltage linearly decreases with time: this conclusion is enforced by the theory developed in this chapter. Besides, the application of our model to SiC diodes shows that the recombination properties of the space charge region have stronger impact on the voltage transient than in Silicon diodes and that the expected duration of decay as longer as than several hours or days [95] is shortened by the unavoidable presence of a leakage current.

The developed self-consistent model turns useful to extend to SiC devices others dynamic measurement techniques traditionally proposed for Silicon [96], representing an accurate tool for the analysis of static and dynamic behaviour of SiC bipolar devices.

4.3 A Novel OCVD Analytical Model

Again referring to the generic 1D pin diode structure reported in Fig. 25 and rewriting the electron and hole current density in a quasi-neutral n-type region as a function of total current J_D (see Eq. 3-2), the hole-diffusion equation in the neutral epilayer can be expressed as:

$$\frac{\partial p(x,t)}{\partial t} = D_a \frac{\partial^2 p(x,t)}{\partial x^2} - U_P - \frac{\lambda_P}{q} \frac{\partial J_D(x,t)}{\partial x} \tag{4-8}$$

where U_p is the hole recombination-generation rate in the epilayer. If D_a and $\lambda_{P(N)}$ are assumed spatially constant for a generic time instant, with their values being taken at the junction border ($x=0^+$), the integration of (4-8) allows one to obtain the spatial–temporal variation of the carrier distribution at the arbitrary injection level imposed by the current.

Assuming, for simplicity, the anode region coincident with the switching terminal, once it has been opened, the current J_D becomes zero at the P^+ contact but continues to flow through the N^+ substrate terminal to sustain the displacement current localized at the two interfaces, though both of them become relevant when the voltage decay is controlled by the depletion capacitance.

From the physical viewpoint, the abrupt annulment of the total current in the P^+ neutral region can be justified through a contemporary modification of the electric field in order to give rise to a majority drift current for contrasting the electron component, remained unchanged due to the slow variation of the minority carrier density everywhere within the device. Since both carriers behave as minority and majority charge at the two extremities of the P^+N junction, the significant variation imposed on the hole and electron currents across the junction manifests itself with an extension of the built-in electric field towards the low doped side of junction and, hence, with a neutrality loss which leads the recombination rate to be more properly expressed as $U_P^I = \frac{\sqrt{pn}}{2\sqrt{\tau_{0p}\tau_{0n}}}$ [34], rather than as $U_P^{II} = \frac{p}{\tau_a}$. Note that, under high injection levels, the former expression can be simplified as $U_P^I = \frac{p}{2\sqrt{\tau_{0p}\tau_{0n}}}$. Therefore, to obtain a physical interpretation of the integral of (4-8), it can be expressed as sum of two different contributions, namely:

$$p(x,t) = p_S(x,t) + p_T(x,t) \tag{4-9}$$

where $p_S(x,t)$ describes the carrier density obtained by using the steady-state spatial distribution as initial condition, while $p_T(x,t)$ accounts for the carrier modification induced by the derivative term of the total current, assuming in this case the initial conditions equal to zero. It's clear from the above observations that, while the U^I contribution can be neglected in (4-8) for $p_S(x,t)$ calculation, in the matter of $p_T(x,t)$ the continuity equation (4-8) must be integrated using the equivalent lifetime term $\tau_{EQ}^{-1} = \tau_a^{-1} + \left(2\sqrt{\tau_{0n}\tau_{0p}}\right)^{-1}$, with τ_a evaluated at the junction border, as D_a.

Since the above integrals, which represent the homogeneous and non-homogeneous solution of (4-8), contribute differently to the shape of the decay curve, in the following they will be derived in separate paragraphs by using, for simplicity, an apex *"0"* for denoting the stationary values of carrier density and current.

4.3.2 Homogeneous Diffusion Equation

As discussed before, the integral $p_S(x,t)$ represents the solution of the continuity equation written in the following manner:

$$\begin{cases} \dfrac{\partial p_S(x,t)}{\partial t} = D_a \dfrac{\partial^2 p_S(x,0)}{\partial^2 x} - \dfrac{p_S(x,t)}{\tau_a} \\ p_S(x,0) = p^0(x) \end{cases} \qquad (4\text{-}10)$$

where $p^0(x)$ represents the stationary hole distribution existing in the epilayer ($0^+ \le x \le W_B$) before the current interruption: it has been derived in section 3.2 (see Eq. 3-4).

Using the variable separation method, the general solution of (4-10) can be written as:

$$p_S(x,t) = \left(A_o + A_1 x\right) e^{-\frac{t}{\tau_a}} + \\ + \sum_{n=1}^{\infty} \left[B_n \cos\left(\frac{k_n}{\sqrt{D_a}} x \right) + C_n \sin\left(\frac{k_n}{\sqrt{D_a}} x \right) \right] e^{-\frac{t}{\tau_a}\left(1+k_n^2 \tau_a\right)} \quad (4\text{-}11)$$

where the eigen values $k_n = \frac{n\pi}{W_B}\sqrt{D_a}$ are obtained using as boundary condition the constancy of the total current along the epilayer (see *Appendix D*), while the coefficients B_n and C_n are determined using the initial condition of current instead of carrier distribution, as normally occurs in the literature, as shown in *Appendix E*.

Finally, by equating the carrier density $p_S(0^+,0)$ and $p_S(W_B,0)$, both calculated from (4-11), with the stationary values $p^0(0^+)$ and $p^0(W_B)$, the coefficients A_0 and A_1 result given by:

$$\begin{cases} A_0 = p^0(0) - \sum_{n=1}^{\infty} B_n \\ A_1 = \dfrac{p^0(W_B) - A_0 - \sum_{n=1}^{\infty} B_n (-1)^n}{W_B} \end{cases} \quad (4\text{-}12)$$

4.3.2 Non-Homogeneous Diffusion Equation

Since the calculation of $p_T(x,t)$ requires the use of two different boundary conditions at $x = 0^+$ and $x = W_B$, in order to account for the presence of the P^+N space charge region and the NN^+ interface, it is convenient to split the $p_T(x,t)$ integral in two components obtained using the same previous analytical approach:

$$p_T(x,t) = p_{T0}(x,t) + p_{TW}(x,t) \quad (4\text{-}13)$$

For brevity, in the following only the $p_{T0}(x,t)$ derivation is shown and just the main differences regarding $p_{TW}(x,t)$ are evidenced. In principle, the individuation of $p_{T0}(x,t)$ in Eq. (4-13) requires the definition of a number of differential problems, to be solved in coupled way, which describe the effect of the epilayer termination at $x = 0^+$ and the derivative term of the total current in (4-8) at the same abscissa.

To overcome the mathematical complexity of such procedure which, however, doesn't ensure an analytical expression for $p_{T0}(x,t)$, Eq. (4-8) can be solved through the Laplace method by using the initial condition $p_{T0}(x,0^+) = 0$ and, for what said before, by describing the recombination rate with the equivalent lifetime term τ_{EQ} and neglecting the derivative of the displacement current J_D until the epilayer is under high injection:

$$\frac{\partial p_{T0}(x,t)}{\partial t} = D_a \frac{\partial^2 p_{T0}(x,t)}{\partial x^2} - \frac{p_{T0}(x,t)}{\tau_{EQ}} \qquad (4\text{-}14)$$

The Neumann condition at the boundary $x = 0^+$ can be individuated by recalling that the annulment of the total current J_D at the P^+ terminal requires the presence of a hole majority current in order to balance the stationary electron current, $J_N^0(0^-)$, at the junction border $x = 0^-$. Therefore, assuming practically unchanged the hole and electron currents through the metallurgical junction, the following equation holds:

$$-qD_a \left.\frac{\partial p(x,t)}{\partial x}\right|_{\substack{x=0^+ \\ t=0^+}} = -J_N^0(0^-) \qquad (4\text{-}15a)$$

or, similarly:

$$-qD_a\left.\frac{\partial p_{T0}(x,t)}{\partial x}\right|_{\substack{x=0^+\\t=0^+}} = J_0 = -J_N^0(0^-) + qD_a\left.\frac{\partial p_S(x,t)}{\partial x}\right|_{\substack{x=0^+\\t=0^+}} \quad (4\text{-}15b)$$

where $J_N^0(0^-) = J_{np+}(0^-)$ is obtained from the stationary model in the previous chapter (see Eq. 3-6) and the latter term can be evaluated from (4-11).

Consequently, if we observe that, according to the continuity equation in the space charge region $\frac{\partial p}{\partial t} = -\frac{p}{\tau_{EQ}}$, the carrier density varies exponentially with time and the carrier velocity is saturated, the previously current balance can be extended at any instant to obtain:

$$\left.\frac{\partial p_{T0}(x,t)}{\partial x}\right|_{x=0^+} = -\frac{J_0}{qD_a}e^{-\frac{t}{\tau_{EQ}}} \quad (4\text{-}16)$$

Therefore, by using (4-16) along with the initial condition $p_{T0}\left(x,0^+\right) = 0$, the solution of (4-14) can be written as:

$$p_{T0}(x,t) = \frac{J_0}{q\sqrt{\pi D_a}}e^{-\frac{t}{\tau_{EQ}}}\left[2\sqrt{t}e^{-\frac{x^2}{4D_a t}} - \sqrt{\frac{\pi x^2}{D_a}}erfc\left(\sqrt{\frac{x^2}{4D_a t}}\right)\right] \quad (4\text{-}17)$$

Similarly, for the absence of a "true" space charge region at the boundary $x = W_B$, as stated above, the $p_{TW}\left(x,t\right)$ integral can be obtained from (4-17) by replacing x and τ_{EQ} with $(W_B - x)$ and τ_a, respectively, and by using for J_0 the following expression:

$$J_0 = J_P^0(W_B) + qD_a\left.\frac{\partial p_S(x,t)}{\partial x}\right|_{\substack{x=W_B\\t=0^+}} \quad (4\text{-}18)$$

being $J_P^0(W_B) = J_{pC}(W_B)$ the stationary hole current shown in the static analysis (Eq. 3-7).

It is worthwhile noting that, in order to calculate the coefficients B_n and C_n of (4-11) and the current J_0 in (4-17), the stationary distributions of carriers and current components along the epilayer must be evaluated at the forced current, J_D.

The relations (4-11) and (4-17) allow to describe the hole distribution $p(x,t)$ along the epilayer until its operation occurs above the intermediate injection levels, namely for $p(0^+,t) \geq N_B$. As the carrier density $p\left(0^+,t\right)$ approaches the epilayer doping N_B, the contributions of the depletion region to the total recombination current and capacitance become comparable with the analogous terms of neutral regions, and that makes untreatable the diffusion equation because of their non linear voltage dependence. Since this part of transient has been already described in [92] using a simple charge control model, it is also adopted here with the aim of describing, in continuity with Eq. 4-11 and 4-17, the punctual decay of the carrier density $p\left(0^+,t\right)$, namely from the time instant when it equates the epilayer doping up to the complete vanishing of the diode voltage.

Hence, once $p\left(0^+,t\right)$ has been determined, typical curves employed in the OCVD method, such as the transitory of the diode voltage $V_D(t)$ and the effective lifetime $F_\tau(t)$ [83], can be derived as:

$$\begin{cases} V_D(t) = V_T \ln\left[\dfrac{p(0^+,t)\left[p(0^+,t)+N_B\right]}{n_i^2}\right] \\ F_\tau(t) = -\eta V_T \left(\dfrac{dV_D}{dt}\right)^{-1} = -\eta V_T \left[\dfrac{1}{p(0^+,t)}\dfrac{dp(0^+,t)}{dt}\left(1+\dfrac{p(0^+,t)}{p(0^+,t)+N_B}\right)\right]^{-1} \end{cases} \tag{4-19}$$

where η represents the ideality factor already presented in section 4.1. Therefore, in our analysis, instead of determining the lifetime value from the linear part of the decay curve, as traditionally done in the OCVD method, it is more suitable, as noted in [90], referring to the whole profile of the F_τ curve. Indeed, typical effective lifetime curves

show maximum and minimum peak values: they are respectively representative of the effective ambipolar lifetime, $\overline{\tau_a} = \overline{\tau_{0p} + \tau_{0n}}$, and the minority lifetime, $\overline{\tau_{0p}}$, spatially mediated in the entire epitaxial layer. This behaviour is better described in Fig. 40, where, as an example, the typical voltage decay and the relative effective lifetime curve, extracted from simulations performed at high injections, are reported.

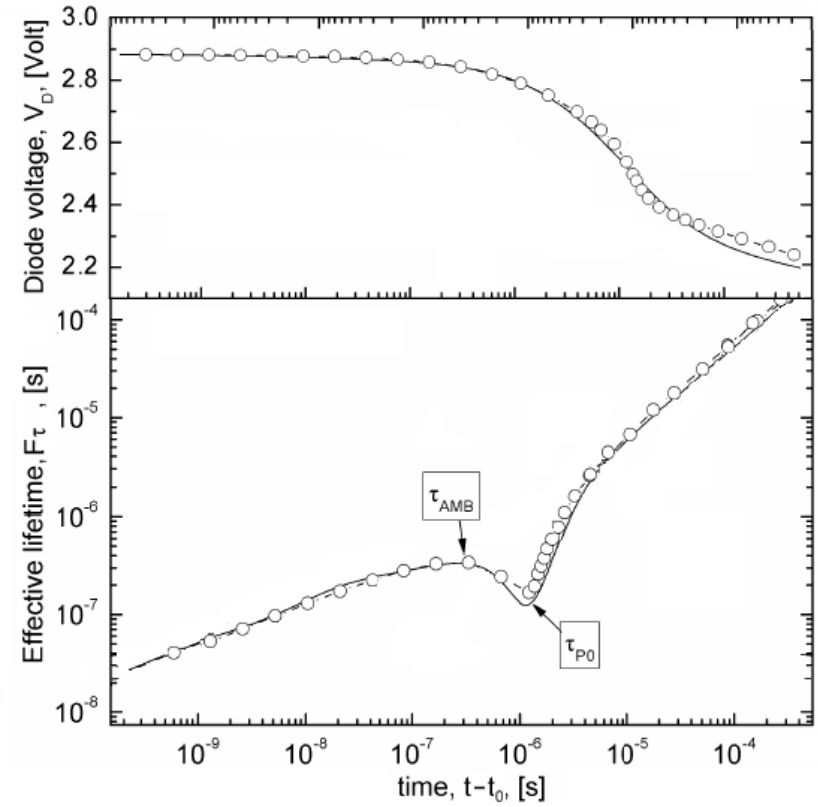


Fig. 40: Typical voltage and lifetime transient of OCVD measurements performed at high injection levels (in t_0 the current is switching-off)

4.4 OCVD Simulations and Model Comparison

For purposes of comparison, numerical simulations [80] were firstly performed on both Silicon and Silicon Carbide diodes, whose principal characteristics are resumed in Table 9. Here, the P^+NN^+ structures described are conceived to provide a wide variation of physical parameters; in detail, devices #1 represent the same version of diode structures realized both in Si and 4H-SiC; device #2SiC differs from #1SiC for a lower lifetime, while devices #3 are representative of two sets of structures realized in Si and SiC.

Device			***Theoretical***			***Experimental***	
Parameter		***unit***	***#1SiC***	***#1Si***	***#2SiC***	***#3SiC***	***#3Si***
Epilayer	τ_{0n} τ_{0p}	*nsec*	*500* *100*		*50* *10*	*15* *15*	*1.1E5* *0.7E5*
	N_B	cm^{-3}	*1E14*			*3E15*	*2E14*
	W_B	μm	*10*			*5*	*50*
P+ region	N_{P+} N_A	cm^{-3}	*7E17* *1E20*	*1E20* *1E20*	*7E17* *1E20*	*5.4E17* *6E19*	*2E18* *2E18*
	W_A	μm	*5*			*~1.2*	*~3*
N+ region	N_{N+} N_D	cm^{-3}	*1.6E19* *5E20*	*5E20* *5E20*	*1.6E19* *5E20*	*4.9E18* *5E19*	*1E19* *1E19*
	W_C	μm	*100*			*300*	*250*
	Device area	μm^2	*1*			*9.6E4*	*2E4*

Table 9: Geometrical and physical parameters of the examined devices for OCVD analysis

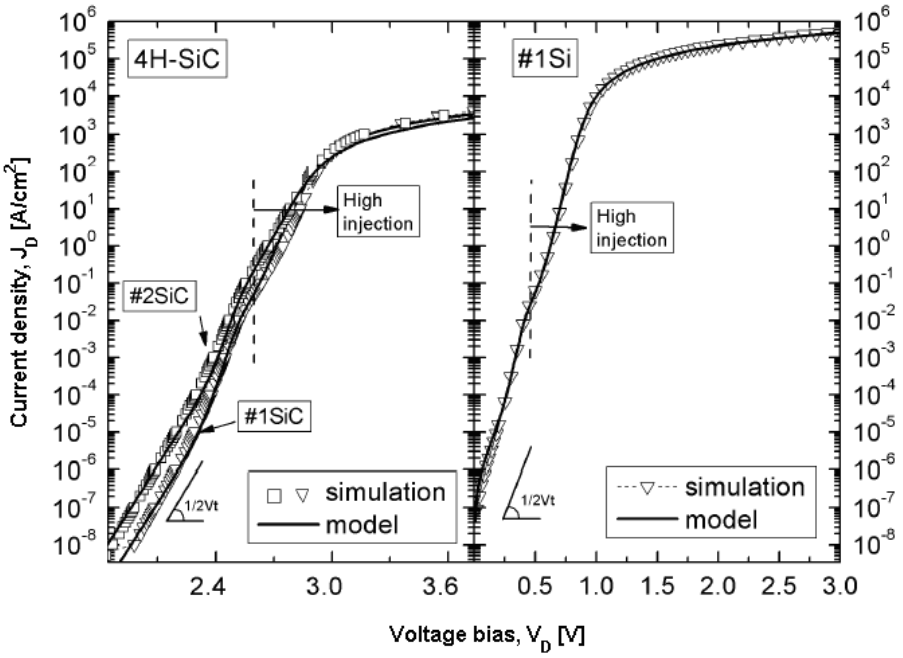


Fig. 41: Comparisons between numerical simulations and model of the *I-V* curves for devices #1SiC, #2SiC and #1Si of Table 9

It must be observed that, as similarly done in the static analysis, the numerical values of all the physical parameters have been set equal in the model and the simulator according to the references given in the previous chapters and that none fitting parameter has been used in the comparisons. In detail, the used models for SiC are those presented in chapter 3, while they are as in [80] for Si. Note that the doping is assumed fully ionized in Si, whereas it is calculated in SiC as in [46] to account for the partial activation of doping.

Fig. 41 compares the *I-V* curves of devices #1SiC and #1Si, with the vertical line indicating the voltage $V^* = V_T \ln(N_B / n_i)$ where $p^0(0^+) = N_B$. It's worth nothing that, besides the higher threshold voltage of SiC diodes due to the high ratio $n_{io}^{Si} / n_{io}^{SiC} = 6.1 \times 10^{17}$, the lower current density at highest voltages comes from the incomplete doping ionisation of 4H-SiC, which is more pronounced for p-type

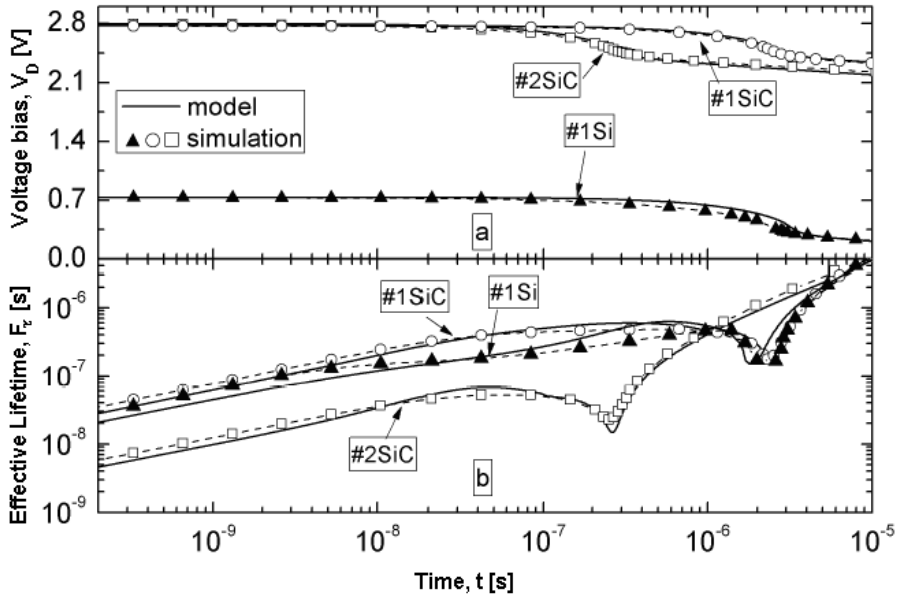


Fig. 42: a) Decay of the diode voltage and b) Effective lifetime curve of devices #1SiC, #1Si and #2SiC of Table 9, switched with J_D density current of 2, 20 and 20 A/cm^2, respectively

regions [46] (see N_{P^+} and N_{N^+} values in Table 9) and intervenes to limit the holes injection from the anode region.

Being intrinsically relevant in the application of the OCVD measurement method, the voltage transient and the effective lifetime F_τ (4-19) for diodes #1SiC, #2SiC and #1Si are displayed in Fig. 42. The switched current level has been chosen 2 A/cm^2 for #1SiC and 20 A/cm^2 for diodes #2SiC and #1Si: these values are relatively high to ensure a steady-state high injection regime with negligible ohmic drops (3-11), whose occurrence could invalidate Eq. (4-19).

However, in the case of higher current levels, it must be observed that a remedy for rejecting the ohmic drop effects, especially for short lifetime measurements, is to add a third terminal on the diode structure, as shown in [91-92]. This can be obtained in practice by providing the measurement set-up with a probe circuit which makes the analogue differentiation of the acquired diode voltage via hardware [97].

By referring to the F_τ curves of devices #1SiC and #2SiC displayed in Fig. 42.b, both peaks return the right values of τ_{0p} and τ_{0n} reported in Table 9, independently of the different J_D currents used for measurements, while the coincidence of the F_τ peaks for #1SiC and #1Si, as expected for the equality of lifetimes in Table 9, proves the validity of this criterion even when the linear decay tends to disappear, as occurs in the curve of #1Si.

The different behaviour of the $V_D(t)$ curves of #1SiC and #1Si is somehow anomalous since, with the mobilities values employed for comparisons: μ_n=962 cm^2/V/s, μ_n=125 cm^2/V/s for SiC and μ_n=1443 cm^2/V/s, μ_p=484 cm^2/V/s for Si, the W_B / L_a ratio results 0.54 for #1SiC and 0.3 for #1Si, and, hence, fulfil in both cases the condition $W_B / L_a < 1$ required for the linear dependence of $V_D(t)$ [85-98].

This condition has been invoked in [95] for demonstrating the existence of a thin layer with very low-lifetime within the metallurgical junction of SiC diodes. On the other hand, by observing that the $V_D(t)$ curve of #2SiC, with $W_B / L_a = 1.71$, exhibits the desired linear decay, we must conclude that the value of the W_B / L_a ratio is quite irrelevant for the $V_D(t)$ behaviour and that the difference of #1SiC and #1Si must be attributed to other reasons, such as, the different current values used in the measurements.

To enforce our conclusion, for all the examined devices the carrier density $p(x,t)$ and the hole current, obtained from Eq. 3-2 with J_D=0, are compared with simulations in Fig. 43 and Fig. 44, where the upper curves, at $t=t_0$, refer to steady state condition. As shown for device #1Si in Fig. 44.c, once the current has been switched-off, the impulsive expansion of the built-in electric field towards the right side of the junction pushes the holes towards the P^+ region and induces the slightly bending of the curves in Fig. 43.c at $t=t_1$, which justifies the presence of the negative hole current at the junction boundary in Fig. 44.c. This current is equal to the steady state electron current $J_N(0^+)$ for all the devices and is nearly vanished at the instant $t=t_3$ when $V_D(t)$ linearly varies in Fig. 42. On the contrary, the hole current at

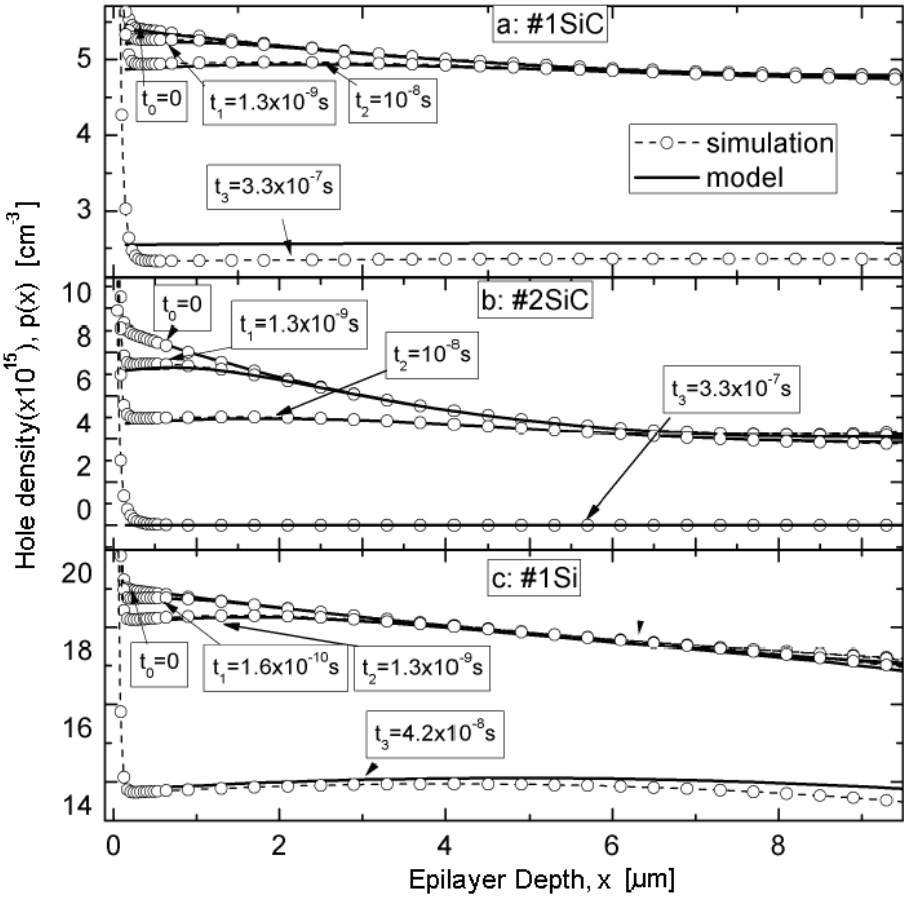


Fig. 43: Transitory of the hole distribution in the epilayer of device a) #1SiC b) #2SiC and c) #1Si, for the same values of J_D current of Fig. 42 (2 A/cm^2 for #1SiC; 20 A/cm^2 for #1Si and #2SiC)

$x=W_B$ remains significant only for #1Si and contributes along with $J_P(0^+,t)$ to the holes removal from epilayer and, hence, to the slope variation of $F_\tau(t)$ for #1Si in Fig. 42.b.

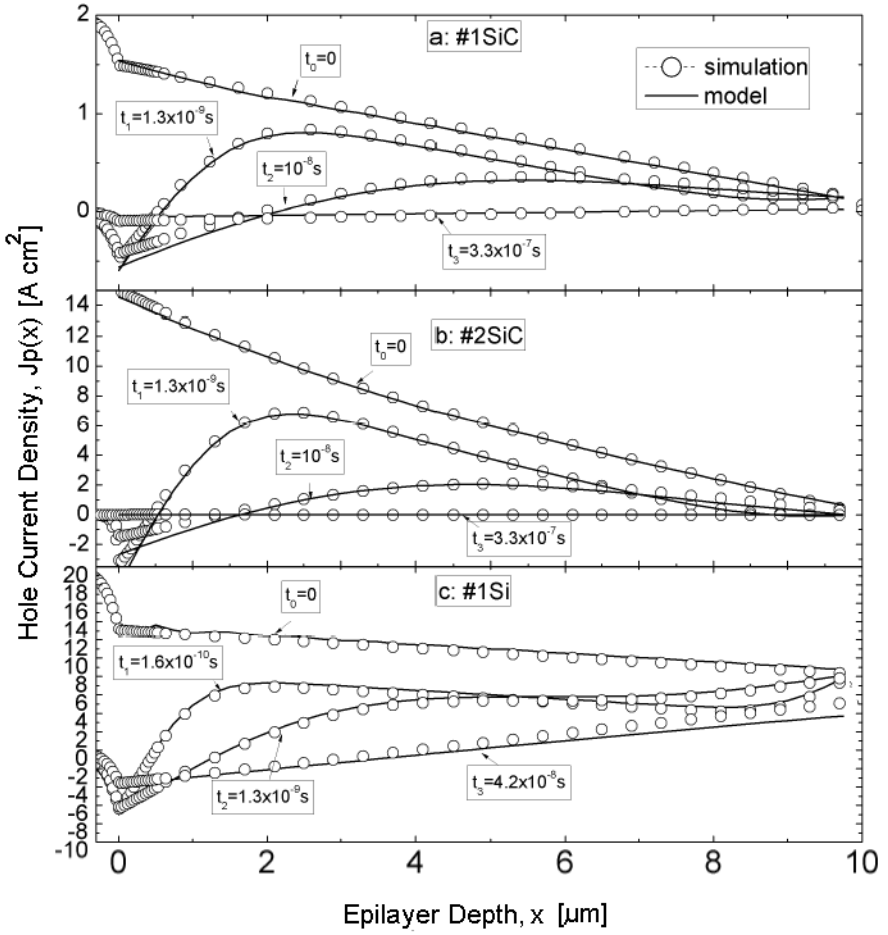


Fig. 44: Transitory of the hole current distribution in the epilayer of device a) #1SiC b) #2SiC and c) #1Si for the same values of J_D current of Fig. 43 (2 A/cm^2 for #1SiC; 20 A/cm^2 for #1Si and #2SiC)

The effects of a low injection efficiency of P^+ and N^+ regions on the shape of the $V_D(t)$ curve of #1Si can be better analysed by observing the behaviour of the F_τ curves in Fig. 45 calculated from (4-19) by considering separately the contribution of $p_T(0^+,t)$ and $p_S(0^+,t)$ to the total carrier $p(0^+,t)$, until $p(0^+,t) \geq N_B$.

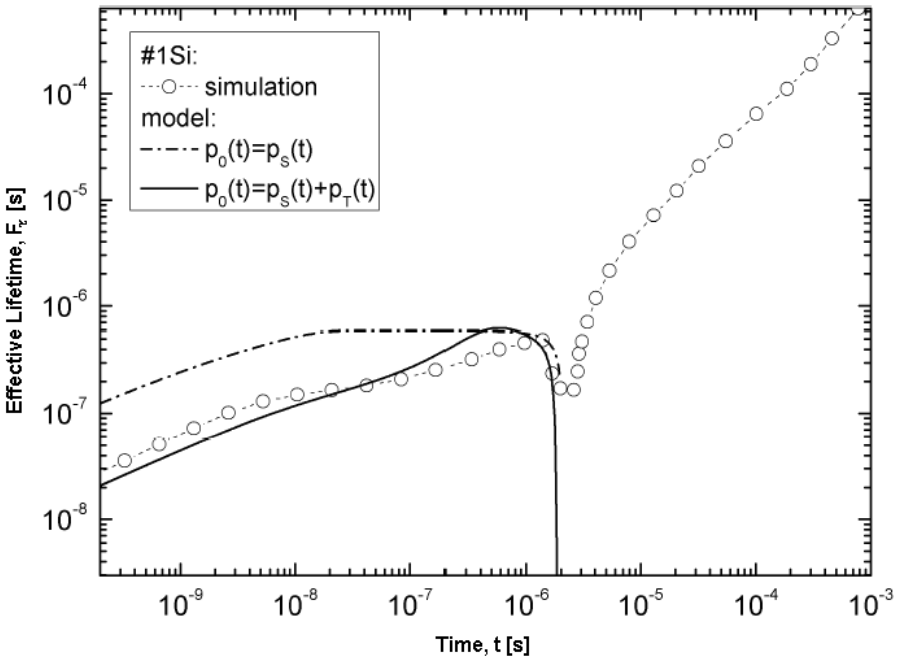


Fig. 45: Effective lifetime curves of #1Si, for different *p(x,t)* approximations in the range $p(0^+,t) \geq N_B$

By comparing the dashed and the solid curves in Fig. 45, it is clear that the contribution of $p_T(0^+,t)$, which de facto models the hole removal operated by the currents $J_N(0^-)$ and $J_P(W_B)$ in Fig. 44.c, is the only reason of the shrinkage, for more than one decade, of the time interval where $V_D(t)$ of #1Si linearly varies in Fig. 44.b. In this case, in spite of a favourable $W_B / L_a < 1$ ratio, the detection of the linear portion of the voltage decay can become difficult or, even, impracticable at still higher J_D values.

Above considerations suggest that the proposed model can turn useful in determining the limit conditions to perform feasible measurements on a given structure with an expected lifetime.

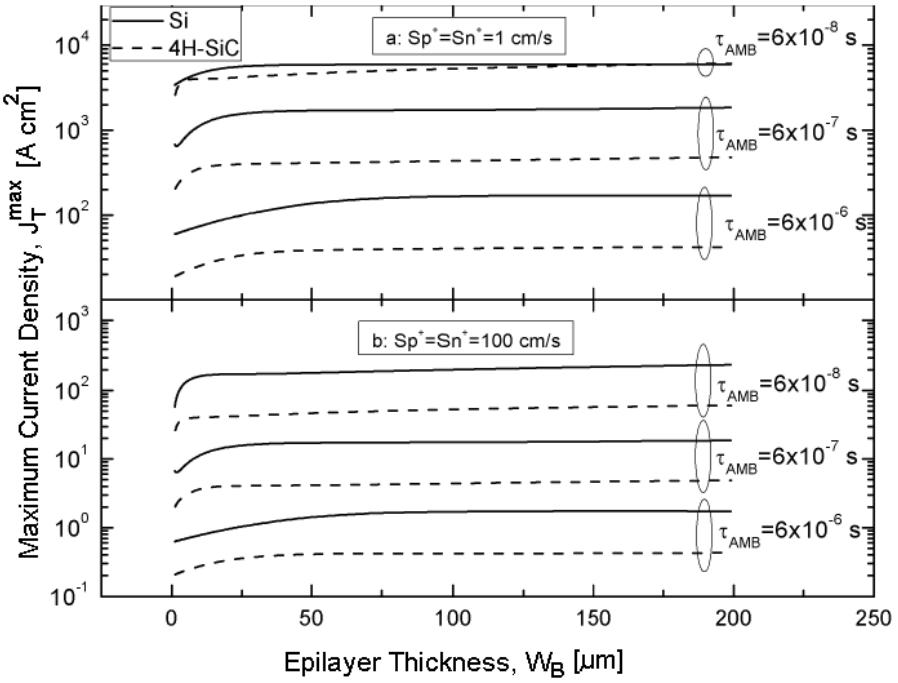


Fig. 46: $J_D^{\max}$ values required for linear voltage decay, as function of W_B and for different τ_a and $S_{N^+} = S_{P^+}$ values, using the epilayer doping $N_B = 10^{14}\ cm^{-3}$. The curves have been obtained imposing $|p_T| = p_S / 2$ at $t = \tau_a / 10$

In this perspective, in fact, by observing in Fig. 42 a strict correlation between the peak values and the instant when they occur for all the devices, the limit condition can be obtained by calculating the maximum value of the bias current, $J_D^{\max}$, which verifies the condition $|p_T(0^+,t)| < p_S(0^+,t)$ at a given instant, chosen reasonably lower than τ_a. Results of such approach are shown in Fig. 46 where, for two values of the effective recombination velocities $S_{N^+} = S_{P^+}$ of terminal regions, $J_D^{\max}$ is plotted as a function of W_B for three expected τ_a values, by imposing $|p_T(0^+,t)| = p_S(0^+,t)/2$ at $t = \tau_a / 10$.

The decrease of $J_D^{\max}$ with $S_{N^+} = S_{P^+}$ and τ_a can be justified by observing that an increase of these parameters rises the ratio of the total current injected in the terminal region $J_N^0(0^+) + J_P^0(W_B) = J_{nA} + J_{pC}(W_B)$ (see Eq. 3-5a and 3-7) to the recombination current in epilayer (see Eq. 3-9) and that, because of the quadratic dependence of the former currents with carrier density, can be compensated with a reduced injection level and, hence, with a lower $J_D^{\max}$ value.

More simply, the higher $J_D^{\max}$ values observed for silicon originates from the lower carrier mobilities of SiC, which leads to a greater J_0 and to a fourth times lower D_a in the coefficient of (4-16), whose increasing can be mitigated with a reduction of the injection level, and, hence, of $J_D^{\max}$ as before.

Finally, it is worth noting that, using the parameter values reported by the authors in [95], the S_{P^+} and S_{N^+} values of the diodes examined, having an epilayer $6\text{x}10^{14}$ cm^{-3}-doped and 50 μm-thick and an ambipolar lifetime of 0.138 μs, result 826 cm/s and 666 cm/s respectively. Comparing the resulting ratios $S_{P^+(N^+)} / N_B$ with results in Fig. 46, it can be concluded that the $J_D^{\max}$ value in this case should not be greater than 100 A/cm^2, which is one order of magnitude lower than that used in [95] in order to confirm the inapplicability of OCVD technique in homogeneous structures with $W_B / L_a > 1$ [98].

Moreover, by observing that the temporal decay of $p_{T0}(x,t)$ (see Eq. 4-17) is determined by the time constant $\tau_{EQ}^{-1} = \tau_a^{-1} + \left(2\sqrt{\tau_{0n}\tau_{0p}}\right)^{-1}$, being the latter term the generic lifetime in the space charge region, our analysis permits also to justify the reason of a linear decay observed on the same structure in [95] if a thin layer with a very small lifetime, estimated around *20 ns*, is located within the metallurgical P^+N junction while the lifetime in the neutral epilayer remains unchanged.

4.5 OCVD Experimental Results

Experimental tests of the OCVD technique have been carried out on the diode structures #3SiC and #3Si in Table 9. It must be observed that the devices #3SiC are the same proposed for the static analysis (see Table 7), while device #3Si [99] have a stripes geometry with the p^+ fingers 15μm wide, 4μm thick and 2x10^{18} cm^{-3} doped. The epilayer is 50μm thick and 2x10^{14} cm^{-3} doped, while the N^+ substrate is 10^{19} cm^{-3} doped and terminated by Aluminum contact.

The OCVD response of both kinds of devices have been obtained with the measurement setup proposed in [97] equipped with a mercury relays triggered by an HP8114 pulse generator to assure galvanic insulation of the switched diode during the voltage decay with a resistance as high as 100MΩ. As shown ahead, the lifetime τ_{0n} and τ_{0p} resulted 15 *ns* for #3SiC and 100 μs for #3Si: both sets of values coincide with those measured in [71-72] on the same SiC diodes by using the reverse recovery technique and on the same silicon diodes by means of scanning measurement technique [92].

The experimental *I-V* characteristics at ambient temperature of #3SiC and #3Si diodes, measured by means of the Agilent 4155B instrument, are compared in Fig. 47 with the numerical and analytical curves obtained using the measured values τ_{0n} and τ_{0p} for describing the doping-dependent lifetime in the different regions of the two devices (see Eq. 2-15).

Note that a current density of about 100 A/cm^2 at V_D=4 Volt has been also measured on the high-voltage SiC diodes employed for the analysis in [95].

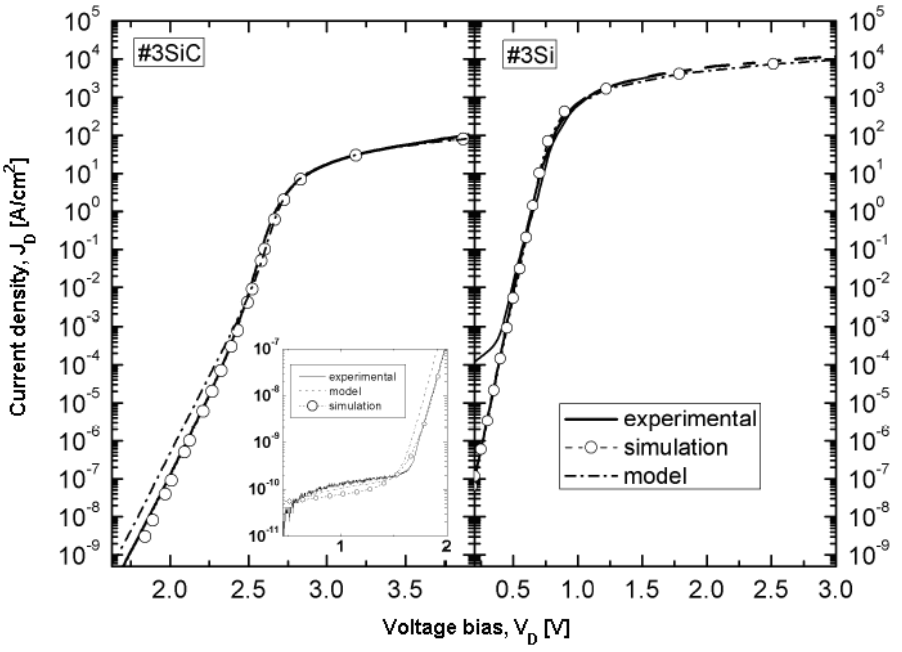


Fig. 47: Comparison between experimental, simulated and analytical *I-V* curves of device #3SiC and #3Si. The inset shows the effect of a shunt resistance at lowest injection

For the device #3SiC, the voltage transient and the effective lifetime measured for a J_D value of 10.4 A/cm^2, corresponding to the injection level $p^0(0)/N_B = 20$, are compared in Fig. 48 with the simulated and the analytical curve, showing also the effect of the addition of a lumped shunt resistance of $10T\Omega$ across the junction. Although such very high resistance is not significant on the normal operation of device, its presence speeds up significantly the voltage decay of many orders of magnitude with respect to the ideal behaviour, expected as long as hours or days [95] due to the lower intrinsic carrier concentration than silicon. The presence of such resistance has been already confirmed in the static analysis (see inset of Fig. 47), where the lowest branch of the *J-V* curves has been modelled including the resistance contribution in Eq. (3-11).

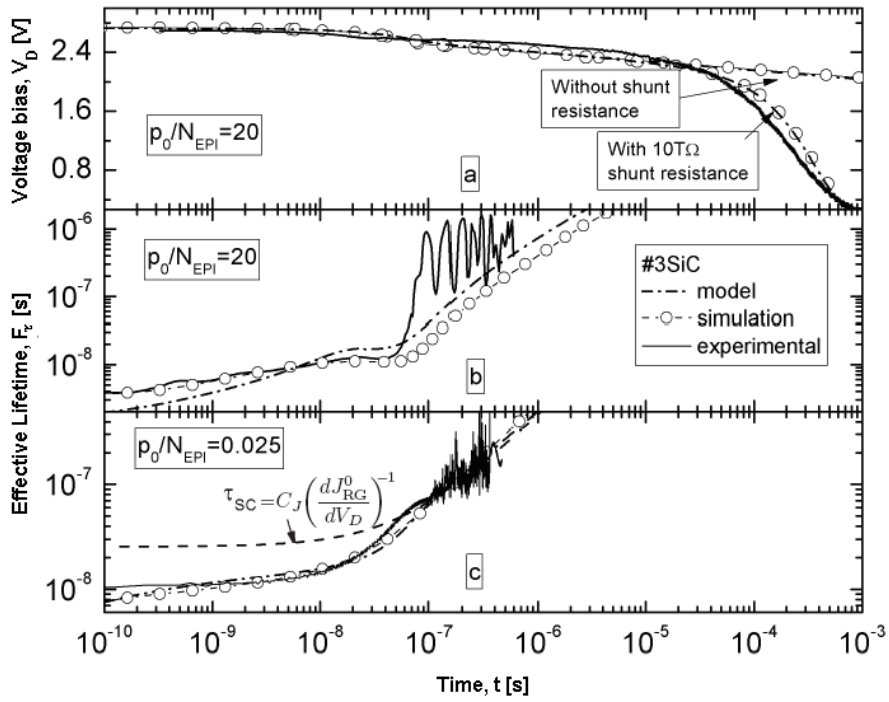


Fig. 48: Comparison between analytical, simulated and experimental curves of a) diode voltage decay b) effective lifetime for device #3SiC, measured with a switched current $J_D = 10.4\ A/cm^2$. Curves c) shows the effective lifetime measured with $J_D = 83\ mA/cm^2$

As shown from Fig. 48, the lifetime extraction procedure presented in [97] and based on the peaks of the $F_\tau(t)$ curves becomes almost mandatory in the case of SiC diodes because of the reduced percentage of the total voltage involved in the linear decay in consequence of the higher threshold voltage of SiC with respect to Silicon.

The noisy behaviour of the experimental $F_\tau(t)$ curve in Fig. 48.b in the range of hundreds nanoseconds is a consequence also of the higher resistance of SiC at low injection regime, thus suggesting the use an electrometer in the measurement set-up [97] for SiC characterization. The accuracy of the model at low injection regime

can be better analysed by observing in Fig. 48.c the curves obtained with J_D=*83mA/cm*^{2} which impose the steady-state injection $p^0(0)/N_B = 0.025$. Though the F_τ curve does not exhibit any peak, allowing just the extraction of the term τ_{0p} from the knee of the curve, the tail of the F_τ curve can be adequately exploited to obtain information on the carrier lifetime of the metallurgical junction, since the recombination current J_{RG}^0 and the capacitance $C_J = \varepsilon / W_{SC}$ of the depleted region dominate in this case.

For this purpose, by defining the time constant associate to the space charge region as:

$$\tau_{SC} = C_j \left(\frac{dJ_{RG}^0}{dt} \right)^{-1} = \frac{C_j V_T}{J_S} e^{-\frac{V_D}{2V_T}} \qquad (4\text{-}20)$$

its plot in Fig. 48.c allows justifying the exponential asymptotic behaviour of the F_τ curves and confirms the usefulness of Eq. (4-20) for accurately interpreting this branch of the OCVD response.

For completeness, results of the OCVD analysis performed on #3Si diodes using a switched current of 50 A/cm^2, corresponding to the injection level $p^0(0)/N_B = 130$, are shown in Fig. 49. By observing that the measured lifetimes $\tau_{0p} = \tau_{0n} = 100\ \mu s$ represent in this case the mean value of the electron and hole lifetime in the whole epilayer volume, these are congruent with the lifetime profile obtained in [97] on similar samples by using the scanning lifetime technique [91].

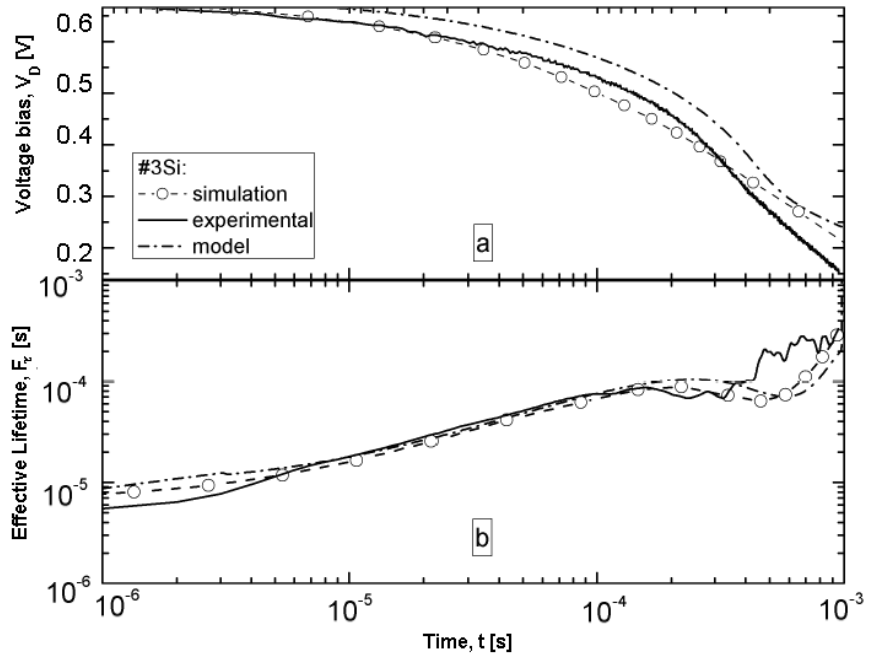


Fig. 49: Comparison between the analytical, simulated and experimental curves of a) diode voltage decay, b) effective lifetime, obtained for device #3Si at the injection level $p^0(0)/N_B = 130$

4.6 RR Analysis

As done for the analysis of OCVD transient, starting from Eq. (4-8) it is possible to obtain a closed form analytical expression for the minority carrier concentration in the neutral base, taking into account the right boundary and initial conditions.

In particular, considering that the vanishing of carriers into the epilayer during the reverse recovery occurs through three different mechanisms, related to the local recombination in the epilayer, the extraction operated by the junction electric field and the diffusion in the cathode, the general solution of (4-8) can be newly written as superposition of two integrals:

$$p(x,t) = p_S(x,t) + p_T(x,t)$$

where $p_S(t)$ represents the homogeneous solution of (4-8) obtained imposing null the derivative of total current and thus expressed by Eq. (4-11), while $p_T(t)$ has an analytical expression similar to Eq. (4-10), since it is calculated by means of the Laplace method using a null initial carrier distribution, thus $p_T(x,0^+)$=0, with the Neumann condition at the two epilayer extremities defined by:

$$\left.\frac{\partial p_T(x,t)}{\partial x}\right|_{x=0^+,W_B} = -\frac{J^0_{0+,WB}}{qD_a} e^{-\frac{t}{\tau_{EQ}}} \tag{4-21}$$

where $J^0_{0+,WB}$ are constants and dependent on the forward (J_D) and the reverse (J_R) current density at $t=0$.

Once the carrier density $p(0^+,t)$ has been obtained, the decay of the diode voltage $V_D(t)$ is obtained from Eq. (3-11) and the total current results:

$$I_D(t) = \frac{V_G - V_D(t)}{R_{EXT}} \tag{4-22}$$

being V_G and R_{EXT} the voltage source and the resistance used in the test equipment, respectively.

As observed before, when the low injection level is approached, the junction capacitance and the recombination J_{RG} in the depletion region dominate the transitory and the voltage decay varies as shown in [92]:

$$V_D(t) = V_D(t_0) + \frac{J_{RG}(t)}{G(t)}\left[e^{-\frac{G(t)}{C_j(t)}(t-t_0)} - 1 \right] \tag{4-23}$$

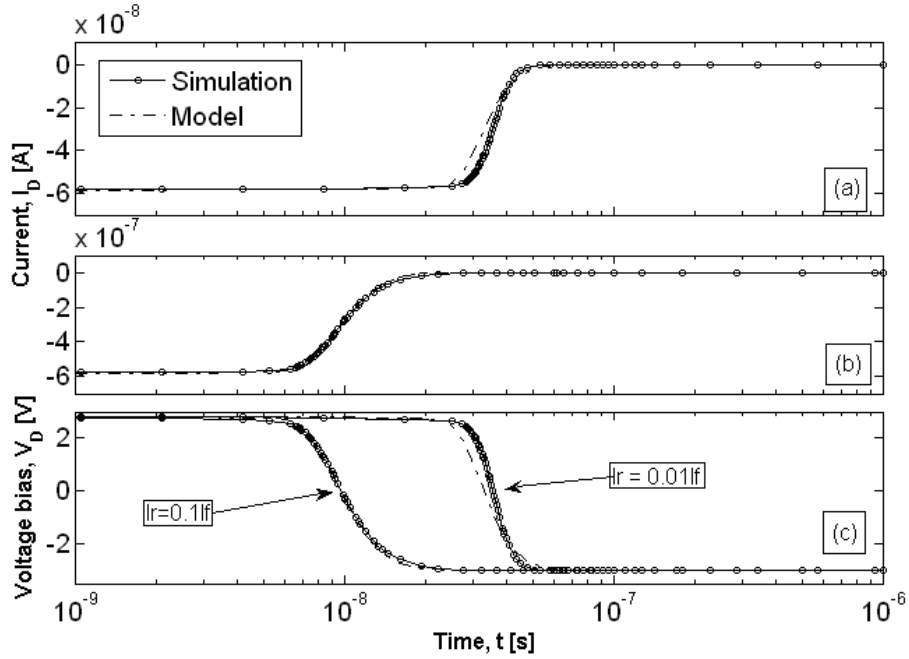


Fig. 50: Current [(a),(b)] and voltage (c) decay curves of #3SiC using I_F=208 A/cm^2 and a) I_R=5.38 A/cm^{2}and b) I_R =58.3 A/cm^2

where $G(t) = g_{SC} + R_{EXT}^{-1}$, with $g_{SC} = dJ_{RG}/dV_D$ and $C_J = \varepsilon / W_{SC}$, and t_0 is the instant for which $p(0^+,t)$ reaches N_B value.

For the validation of above considerations, the diode structure used for simulation has the main geometrical and physical parameters reported in Table 9 for device #3SiC; in fact, it has been chosen similar to the experimental one proposed, differing only for having assumed ‘’box’’ the profile of the implanted P^+ region.

In Fig. 50, current and voltage transients obtained for simulated device when it is forward biased at a current I_F = 208.2 A/cm^2 (corresponding to the injection level $p^0(0^+)$=2.4x10^{16} cm^{-3}) and then switched with a current $|I_R|$=5.83 A/cm^2 and $|I_R|$=58.3 A/cm^2 (i.e. 0.01I_F and 0.1I_F) are reported. For the same structure, observing the carrier distributions in Fig. 51, it is interesting noting that, while the

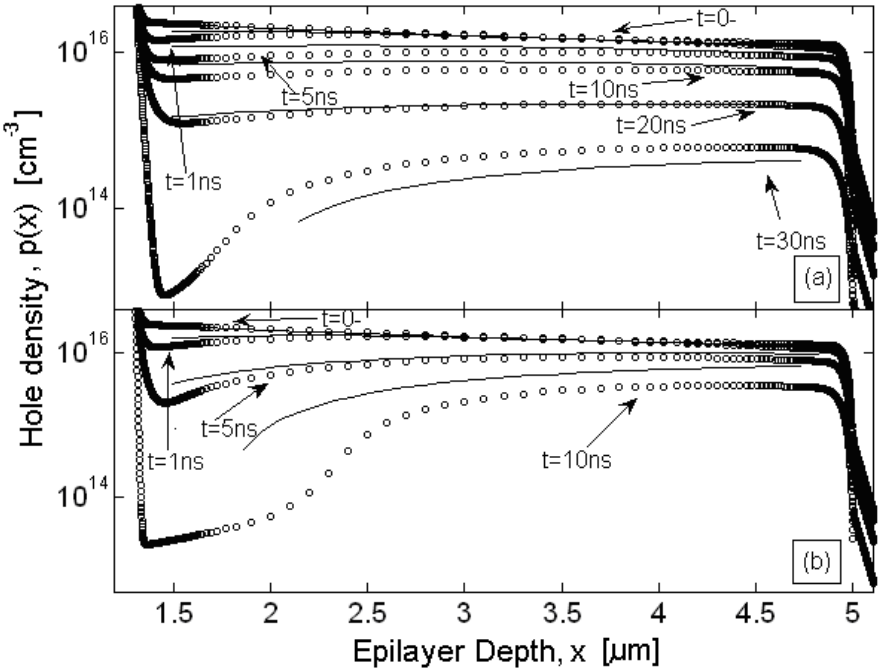


Fig. 51: Transitory of the hole distribution in the epilayer of #3SiC using I_F=208 A/cm^{2}and a) I_R=5.38 A/cm^{2}and b) I_R=58.3 A/cm^2

hole carriers are swept in proximity of the P^+N junction, their value at the NN^+ interface remains high during the whole turn off of the diode.

It must be remarked that, once the storage interval is completed, the operation of the diode goes into the low injection regime and, hence, only the voltage and the current decay can be evaluated according to Eq. (4-22) and Eq. (4-23), because in this part of the transitory the series external resistor and the junction capacitance define the time constant.

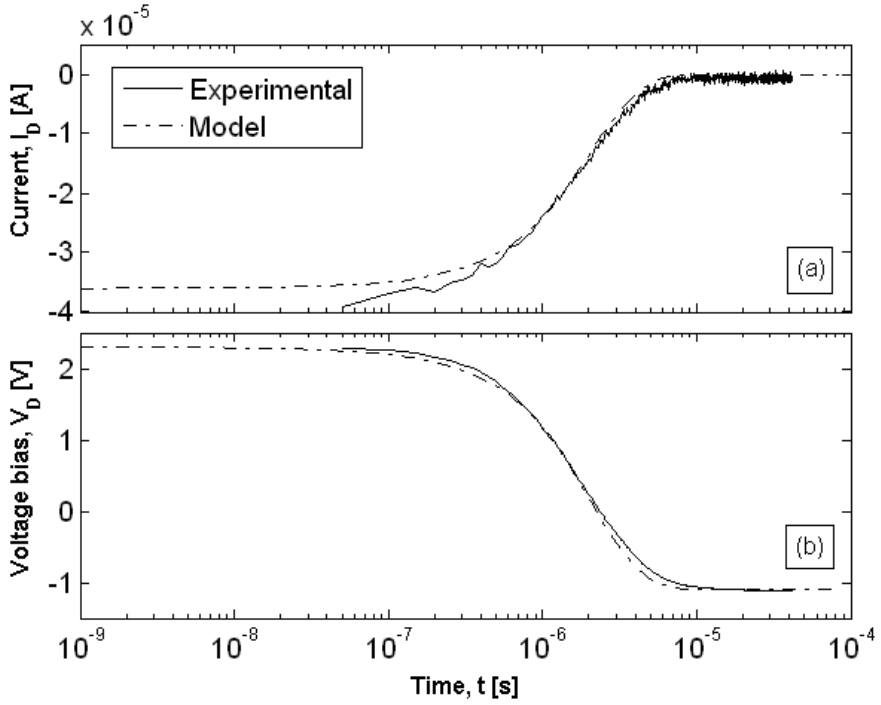


Fig. 52: Current (a) and voltage (b) decay curves of #3SiC using I_F=146 mA/cm^2 and I_R=37 mA/cm^2

In order to validate the model with measurements, the results of the reverse recovery transients performed on #3SiC sample using HP8114A pulse generator are reported in Fig. 52 and compared with the analytical prevision. The significant agreement observed in this case is a clear proof of the validity of the model and confirms its usefulness for better understanding the switching behavior of SiC diodes.

Chapter 5

Further Research Activity: Design of FPGA-based Systems

Due to the need of satisfying the request of high speed of system and hardware cost constraints, in the past few decades the number of hardware implementations based on Field Programmable Gate Arrays (FPGAs) is increasing, because they allow the building of rapid prototypes, reducing development time and board area. However, since FPGAs have limited available resources, area consumption must be improved to satisfy speed and size constraints; besides, it is not immediate that these devices could satisfy low-power consumption constraint.

These considerations show that an efficient design on FPGAs is a crucial aspect to increase the overall performance and integration level of the system. Following these issues, this chapter presents the techniques to obtain an optimization area consumption considering as case of study a new Context-Adaptive Variable Length Coding (CAVLC) encoder architecture: this solution is particularly aimed to be implemented with Field Programmable Logics (FPLs) like FPGAs. For its design, different approaches are adopted with the aim to minimize the area cost as well as to speed up the coding efficiency, allowing to obtain real time compression of 1080p HDTV video streams coded in YCbCr 4:2:0 format.

In detail, with an appropriate attention to the circuital planning to increase the parallelization degree in the elaboration phase of the input data, it has been favoured the limitation of the overall number of clock

cycles needed for the elaboration, while the employment of the Arithmetic Table Elimination (ATE) technique has led to a resource minimization, by the elimination of 18 of the 38 tables traditionally needed for coding. As shown, the design achieves real time elaboration with an operation frequency of only 63MHz and occupies 2200 LUTs when implemented on a low-cost, low-end XILINX Spartan 3 FPGA, thus overcoming the most recent designs proposed for FPL implementation and making this encoder comparable both in terms of area and speed with some recently proposed ASIC implementations and IP cores.

5.1 Case of Study: Context-Adaptive Variable Length (CAVLC) Encoder for Real-time Video Compression

5.1.1 Motivation

The Variable Length Coding (VLC) is by time the most used method of applying entropy coding to large amount of data to be electronically stored or transmitted [100]. It achieves an effective lossless compression through the elimination of redundant information by assigning shorter codewords to most likely occurring symbols with respect to less likely occurring [101]. However, its compression effectiveness strongly depends on the availability of consistent information about the statistical occurrence of symbols and on the capability of implementing large tables to associate that information with codewords. To these issues, the most recent VLC variant, namely the *Context Adaptive Variable Length Coding* (*CAVLC*) [102-103], adds a high computational demand ascribed to the adaptive selection of codewords from several tables during the elaboration of a symbol, on the basis of previously coded symbols, in order to achieve unprecedented compression ratios. As a consequence, the inclusion of the CAVLC in the ITU-T H.264/MPEG-4 Part 10 Advanced Video Coding (AVC) [104], which is imposing as the leading standard for

video compression thanks to the good efficiency and the high flexibility which extend its application to HDTV, videoconferencing and portable media, has promoted an intense research activity aimed to find the optimal architecture for an effective hardware implementation of the CAVLC encoder.

As a result, a number of papers have been published concerning the VLSI architectures of the encoder especially addressed to ASIC implementations in order to obtain high frequency of operation, reduced area and real time coding of high-definition video streams [105-108]. The design in [105] implements algorithms to compress the codeword tables for reducing the memory demand and to calculate on-the-fly some of the codewords; that in [106] implements a SIPO buffer to elaborate two levels contemporaneously along with a fast look-up table matching algorithm to increase the data throughput rate; the encoder in [107] is based on a two-stage block pipelining scheme in order to superimpose the pre-coding and the coding phase; finally, in [108] table elimination techniques and table packers have been implemented to reduce the overall area occupation of the encoder.

Such approaches, however, usually obtain real-time encoding through the increment of the elaboration frequencies which is not the optimal choice to implement the encoder with FPGA platforms, representing the core of modern System-on-Programmable-Chip (SoPC), which are of great interest nowadays for realizing embedded HW/SW multimedia systems, as attested by a number of commercial IP solutions for supporting video applications, particularly suited for FPGA implementation [109-111].

In this context, the development of FPGA-based architectures capable of satisfying the high computational demand of the CAVLC algorithm, in order to obtain good compression performances and high flexibility, represents a high challenging objective because of the limited physical resources of FPGA logics that strongly penalize the performances as happens, for example, in the H.264 encoder proposed in [112] where the limited number of available logic blocks compelled to implement the CAVLC module via software to be executed by an embedded ARM processor.

With the aim to reduce the area occupancy and power dissipation which can be very high when the encoder is implemented with FPGA

logic, a number of scientific works have been published [113-115]. In [113] arithmetic manipulations have been implemented with the aim to eliminate some of the large tables conventionally used for coding the non-zero coefficients; in [114] the tables have been reduced by applying a split and share approach; in [115] a table compression technique have been implemented which uses two small tables and a pointer circuitry for substituting the conventional codewords tables.

However, in these works a minor attention has been pointed to speed performance, since these designs are able to elaborate in real-time only CIF (352x288 pixels) frame, thus attesting the need of further improvements in order to match better speed performances in conjunction with reduced area occupancy and power dissipation.

To this aim, we propose a new CAVLC encoder architecture designed to achieve real time operations on 1080p HDTV frames through the utilization of different approaches in order to minimize the area cost as well as to speed up the coding efficiency and to reduce the power consumption also when implemented on a low-cost, low-speed FPGA platform. The proposed encoder employs redundant circuitry to implement priority cascading logics which allows to highly improving the degree of parallelism of the circuitry devoted to the extraction of symbols from the input coefficients. Such approach is not trivial because of the sequential nature of the CAVLC algorithm which requires a careful alignment of the extraction and coding procedures, for correctly producing the output bitstream and its variable length.

In order to balance the area cost related to the unavoidable replication of logic blocks needed to increase the parallelism, also the Arithmetic Table Elimination (ATE) technique is employed to eliminate a large portion of the area demanding tables needed in the encoding phase. Our implementation results overcome other encoders recently proposed for high-end FPGA implementation [113-115] and quietly compare with the ASIC designs proposed in [106-108].

5.1.2 CAVLC Algorithm

For better understanding the CAVLC algorithm, an example of coding is shown in Fig. 53. The algorithm is based on the encoding of

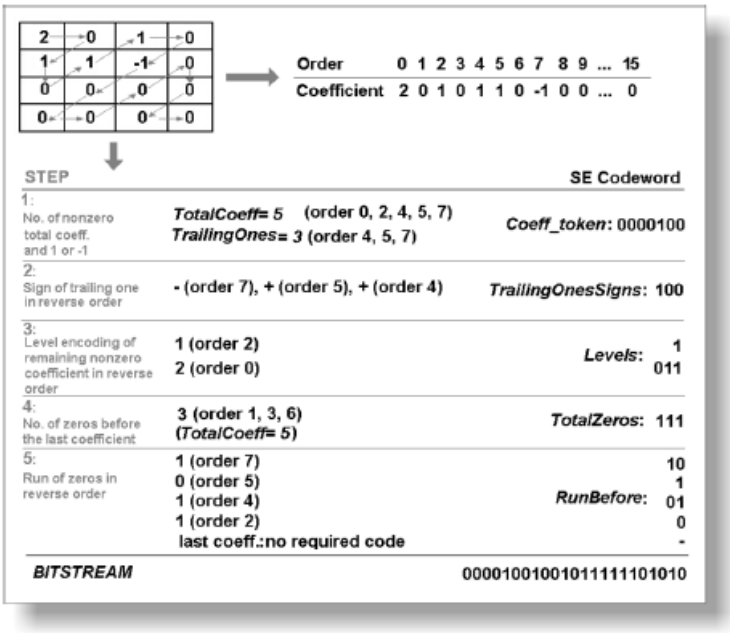


Fig. 53: Example of the CAVLC algorithm

five symbols extracted by reading in reverse order the vector of coefficients obtained by *zig-zag* reordering the input matrix of residuals, 4×4 for Luma and 2×2 for Chromas [102]. Such reordering is required to position the most recurrent coefficients, coded with shorter codewords, in the more significant positions.

The symbols of interest are named with conventional terms: *Coeff_token* encodes both the *TotalCoeff*, i.e. the number of the total non-zero coefficients, assuming values in the range [0,16] and the *TrailingOnes*, i.e. the number of consecutive ±1, up to three, obtained by reading the input vector in reverse order; further ±1 residuals are considered as normal non-zero values. *TrailingOneSigns* are the signs of the trailing ones, 1 for negative and 0 for positive; *Levels* are the values of the non-zero coefficients other than the trailing ones; *TotalZeros* is the total number of zero coefficients after the first non-zero in reverse reading order. Finally, *RunBefore* is the number of total zeros between two consecutive non-zero coefficients.

TotalCoeff is the first syntax element to be considered since other symbols, like *Coeff_token* and *TotalZeros*, are encoded by means of tables indexed with its value. In the case of Luma, *Coeff_token* is coded with codewords taken from 4 tables, 3 tables of variable length codewords (VLC) and 1 of fixed length codewords (FLC), while for Chroma only 2 VLC tables are employed.

nC	***Tables***
$0 \le nC < 2$	*Table 1*
$2 \le nC < 4$	*Table 2*
$4 \le nC < 8$	*Table 3*
$8 \le nC$	*Table 4*

Table 10: *nC* values used for the choice of the *Coeff_token* coding table

The choice of the table is based on the value of $nC = (nA + nB + 1) >> 1$ according to the criteria reported in Table 10, where *nA* and *nB* represent the *TotalCoeff* values of the left and the upper previously coded block. As a particular case, if *nA*=0 (*nB*=0) then *nC*=*nB* (=*nA*).

The *TrailingOneSign* symbol is directly coded by reading the MSB of the trailing one coefficient. The *Level* (sign and magnitude) is coded by means of 7 bi-dimensional VLC tables indexed by *TotalCoeff* and *TrailingOnes*. Usually, the statistical distribution of the coefficient values increase towards the more significant positions of the reordered vector: according to this characteristic, the CAVLC algorithm adaptively selects the table for encoding a level to the value of that previously coded. The *TotalZeros* symbol is encoded with 15 mono-dimensional VLC, selected on the basis of the *TotalCoeff* value. The *RunBefore* symbol is encoded by indexing 7 VLC mono-dimensional tables selected on the basis of the *ZeroLeft* syntax element which represents the remaining number of zero coefficients after the current non-zero coefficient. Two exceptions occur: the *RunBefore* of the last coefficient is not encoded and, if ∑(*RunBefore*)= *TotalZeros*, no other values must be encoded.

More details about the tables will be given in the following, when the reduction algorithm will be presented.

5.1.3 Proposed Design

According to the CAVLC algorithm, which separates the elaboration in a pre-coding phase to extrapolate the symbols to be coded from the input residuals and a subsequent coding phase to encode those symbols in the output codewords, the proposed design has been divided in two stages as shown in Fig. 54.

The first stage receives as inputs the block to be elaborated, the *nA* and *nB* coefficients needed to contextualize the coding of the *Coeff_token* and the *Luma/Chroma selector* to adapt the coding to the Luma or Chroma block and to enable the encoder operation. In the second stage the extracted symbols are encoded with codewords of

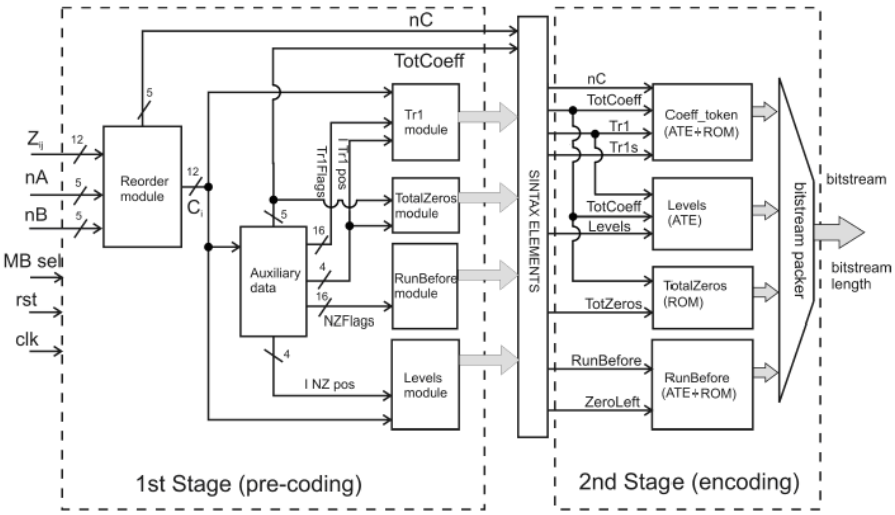


Fig. 54: Architecture of the proposed encoder. The pre-coding and the coding stages are evidenced

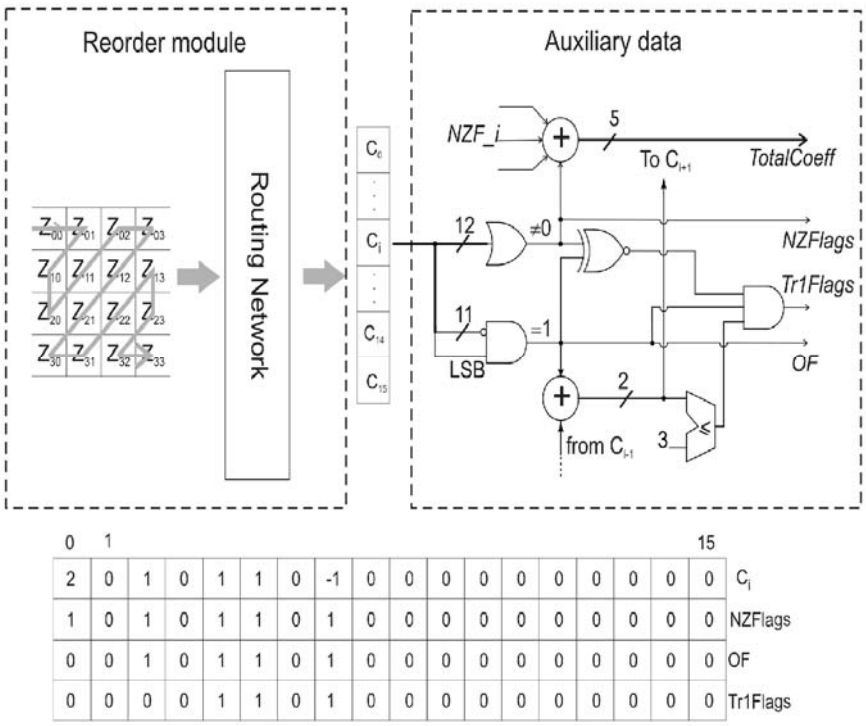
statistical variable length, producing the final packed bitstream. In the following, both stages are described, indistinctly referring to Luma or Chroma coefficients if not otherwise specified.

5.1.3.1 Architecture design of the pre-coding stage

The straightforward implementation of the pre-coding phase would require at least one sequential scanning of the reordered input vector with large amount of statistic buffers and a consequent large area consumption; alternatively, several sequential scanning would significantly increase the computational delay.

In literature, some authors have improved such trivial approaches by proposing solutions particularly aimed to increase the encoder frequency of elaboration by means of elaborate pipeline structures and the optimization of the statistic buffers [105-108]. On the contrary, our approach is aimed to improve the parallelism of the elaboration through redundant circuitries organized in priority cascading structures where sequential elaborations are required, in order to avoid the employment of serial scanning buffers and reduce the number of required clock cycles, thus making the proposed encoder much closer to a SIMD machine. This solution allows to reduce the demand of high frequencies and helps to limit the power dissipation also.

As shown in the block diagram of Fig. 54, the pre-coding stage is composed of six modules: the *Reorder* module, which provides the zig-zag reordered vector from the input blocks and the *nC* coefficient; the module for the production of auxiliary data needed to optimize the symbol extraction, which also generates the *TotalCoeff* symbol, and four other modules, operating in parallel, each devoted to the extraction of a different symbol.



	0	1															15	
2	0	1	0	1	1	0	-1	0	0	0	0	0	0	0	0	0	0	C_i
1	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	NZFlags
0	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	OF
0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	Tr1Flags

Fig. 55: Block diagram of the Reorder module and the schematic of the circuitry needed for auxiliary data calculation of the *i-th* coefficient

In Fig. 55 the *Reorder* module is schematized: it receives as inputs sixteen or four 12bit coefficients, respectively in the case of Luma and Chroma MBs [117] and provides the 16x12b vector of C_i reordered according to the zig-zag criterion by means of a simple routing network. The circuit for *nC* calculation is not shown since it simply require a 5bit adder and a shifter; the *Auxiliary data* operates in parallel on every C_i to provide four vectors of auxiliary data, employed for the operations of the subsequent modules; in Fig. 54 these vectors are indicated as *NZFlags*, *Tr1Flags*, which respectively specify if C_i is not null or it is a trailing one, and as *ITr1Pos*, *INZPos* which give the position of the first trailing one and of the first *Level*, respectively.

According to the circuitry of Fig. 55, where also the initial example is retrieved for continuity, the *NZFlags* is obtained by the bitwise OR of each residual: the usefulness of the auxiliary information suddenly appears in the calculation of the *TotalCoeff* syntax element since it requires the simple bitwise addition of the elements belonging to this first extracted register.

Being context adaptive, the *Tr1Flags* requires a more complex calculation: to this aim, the employment of the *OF* intermediate register in Fig. 55, calculated by the AND of the LSB of C_i with the complement of the remaining more significant 11 bits, permits to define the necessary subset of conditions for rightly detecting the trailing ones. In detail, the AND of the current bit of the *OF* register with the output of the XNOR of *OF* and *NZFlags* permits to reveal if the *i*-th residual is a trailing one. The *OF* is also added to that coming from the previous, less significant, coefficient in order to evaluate if the total number of ±1 is greater than 3, in which case the *Tr1Flags* is reset by the output AND.

Finally, as reported in Fig. 56, two additional registers, named *LD_TR1* and *LD_NZ*, are used to point out the positions of the leading ones: starting from them, two priority encoders (PE), each implemented according to the scheme of Fig. 57, are used to extrapolate the positions of the first trailing one (*ITr1Pos*) and the first non-zero coefficient (*INZPos*), respectively.

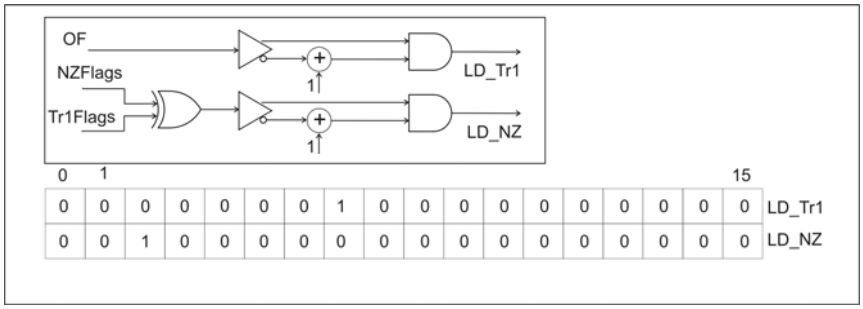


Fig. 56: Circuit schematic for the generation *LD_TR1* and *LD_NZ*

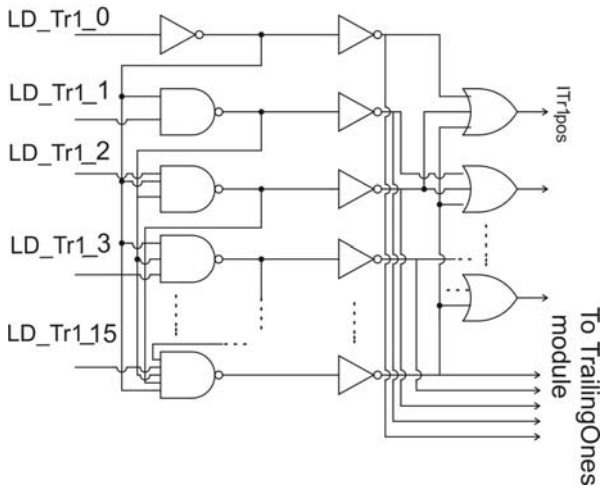


Fig. 57: Circuit schematic of the priority encoder. Auxiliary signal are sent to the *TrailingOne* module to extrapolate the second and the third trailing one positions

The output of the *Reorder* and *Auxiliary-data* modules are available one clock period after the elaboration has been enabled. It's worth observing that the use of auxiliary data can remind to the approach presented in [118] where the authors derive all the symbols from logical operations on side information with the purpose of reducing the power dissipation given from numerous memory accesses. However, the complete derivation of all SE from the side information in [118], balances the reduction of memory access with a large number of logical operations, thus reducing its performances to process in real time only CIF frames when implemented in ASIC.

The *TR1* module receives as inputs the coefficients C_i, the *Tr1Flags* and the position of the first trailing one, and provides, in a single clock cycle, the numbers of trailing ones, the 2 bit width *TrailingOnes* symbol, and their signs, the 3 bit width *TrailingOnesSigns* symbol. Similarly to *TotalCoeff*, the *TrailingOnes* symbol is calculated by bitwise adding the *Tr1Flags* elements. The positions of the trailing ones, needed to extract the *TrailingOneSigns* symbol, are calculated by using the circuitry schematized in Fig. 58 which employs two PEs with the same topology of Fig. 57.

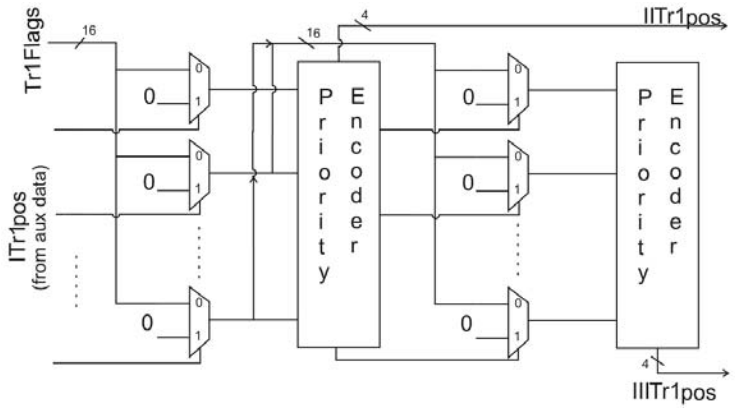


Fig. 58: Scheme of the *TrailingOnes* module

Signals from the PE used for revealing the position of the first trailing one (see Fig. 57) are used to reset the corresponding bit of the *Tr1Flags*, so that a second PE operating on the modified flag vector can reveal the position of the second trailing one. This procedure is repeated by a third PE to reveal the position of the last trailing one. The *TrailingOnesSigns* symbol is finally obtained by reading the MSB of the C_i taken at the obtained positions.

The value of *TrailingOnes* also specifies the *TrailingOneSigns* length.

The *Total_Zeros* module receives as input *TotCoeff* and *Tr1Flags* and provides a 4bit word showing the total number of zero after the first non zero coefficient. The implementation of this module simply requires the cascade of two adders to calculate:

$$TotalZeros = ITR1Pos + 1 - TotCoeff\ .$$

The *RunBefore* module operates on the *NZFlags* and provides a vector of 16 *Runbefore* symbols of variable length, giving for each non zero coefficient the number of zeros between this and the previous non zero coefficient. The generic *Runbefore(i)* must be coded with a number of bits given by *ceil*(lg*i*), namely the first integer higher than the 2 base logarithm of its position. The circuitry implemented for its calculation consists of n=*ceil*(lg*i*) operating in parallel, each

receiving as input the *NZFlags* in the interval [0,*i*], and providing a bit of the *Runbefore(i)* word. The *RunBefore* module also provides *ZeroLeft* by subtracting *Runbefore(i)* from *TotalZeros*.

Both *Total_Zeros* and *RunBefore* modules calculate all the output symbols during the second clock period after the pre-coding phase has been initiated, namely once the auxiliary data have been calculated.

The circuit for *Levels* extraction is shown in Fig. 59. The scheme has been divided in three sections: the *new index generator* is built with cascaded connecting PEs which detect, in each clock cycle, the positions of the two subsequent non zero coefficients by calculating their distance from the current coefficient. The position of the first coefficient is derived by the reorder data module and eventually updated with the last trailing one position; the *first* and the *second coefficient selector*, alternatively enabled by a T-FF, are implemented with register banks in order to store the coefficient positions and with multiplexers used to select the appropriate levels.

Since CAVLC requires that levels must be sequentially processed, due to the context adaptivity of the algorithm, the capability of the proposed *Level* scheme to elaborate two levels during one clock cycle

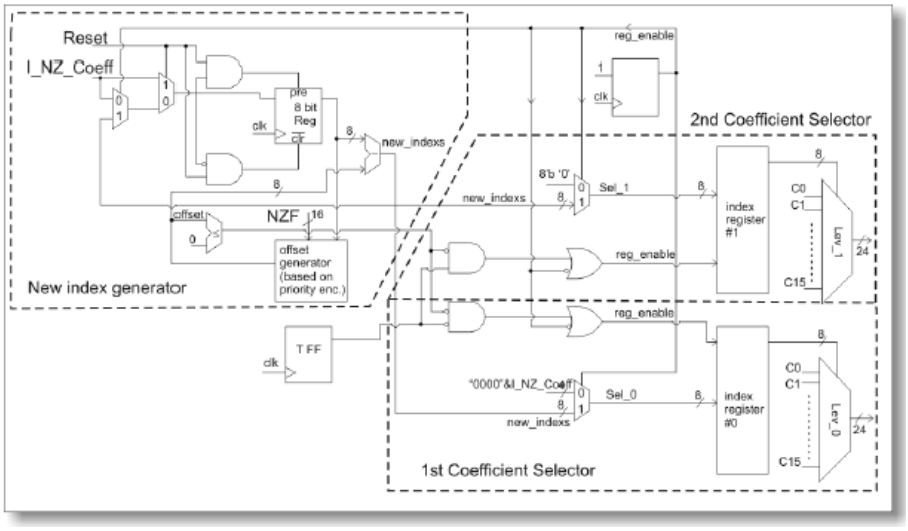


Fig. 59: Scheme of *Levels* module

gives a high improvement to the encoder throughput, with negligible effects on the maximum frequency achievable. Nevertheless, the presented solution allows to easily skip the elaboration of zero levels with beneficial effects on the effective computational delay, in particular in the case of high definition videos, when high bit rates are required.

5.1.3.2 Architecture design of the second stage

The second stage is devoted to the encoding of the SE calculated by the first stage, while the *Bitstream packer* provides for compacting these codewords into the output bitstream and for calculating the overall length.

The encoding process is accomplished by means of a large number of tables storing codewords of variable length, related to the different SE. However, a serious concern arises when the hardware implementation of such tables is required, as appears by the values reported in Table 11, where the memory costs needed to store all the variable length codewords are reported for each SE. It's worth noting that these values don't account for the additional memory requirement to store also the length of each codeword. A way of lighten the memory cost consists in the table elimination by means of arithmetic manipulations of the codewords.

Symbol	***Memory cost [bits]***
Levels	*1.72M*
RunBefore	*347*
TotalZeros	*1.209k*
Coeff_token	*4.446k*

Table 11: Memory cost to encode the syntax elements

In the proposed encoder the second stage is essentially composed of combinatorial circuitry implementing the ATE algorithms and memory elements to store the tables or part of them that cannot be completely removed by arithmetic manipulations. More precisely, the adopted ATE technique consists in detecting relationships between codewords of a table having a corresponding simple, and hence convenient, circuital implementations, in order to reconstruct the entire table from arithmetic operations on the addressing data or, alternatively, on a subset of codewords when the table cannot be completely eliminated.

By using this approach, we achieved the elimination of 18 of the 38 tables required by the standard (7 for *Levels*, 7 for *RunBefore*, 18 for *TotalZeros* and 6 for *Coeff_token*), while the remaining 20 tables have been compressed up to reduce their memory demand of about 30%.

In the following, emphasis will be given to the derived algorithms rather than to their simple circuital implementations.

At the first, note that codewords from the seven Lev-VLC tables, from which are taken the appropriate codewords to encode each *Level*, have a maximum width of 28 bits, arranged as:

$$code = \underbrace{0...0}_{Prefix\_length}\ 1\ \underbrace{x...x}_{Suffix\_length}\ s$$

where *s* is the level sign, 1 for negative and 0 for positive, the sequence of zeros on the left of 1 and the sequence of bits on its right are the *Level_prefix* and the *Level_suffix* respectively, whose lengths, *Prefix_length* and *Suffix_length*, distinguish the codewords. As a particular case, codewords from *Lev-VLC0* have only the prefix.

The context-adaptive algorithm requires that the number of the Lev-VLC table, *N* (ranging from 0 to 6), must be the same used to encode the previous level or it's eventually incremented if the magnitude of the level itself satisfies the inequality *|Level|>[000011<<(N-1)],* being "<<" the left-shift operator. The first level starts with *N=0* (*Lev-VLC0*), except if *TotalCoeff>10* and *TrailingOnes<3*, in which case starts with *N=1* (*Lev-VLC1*). An inspection of the *Lev-VLC0* table, shown in Table 12, reveals that its

Code Number	*Codeword for Lev-VLC0 Table*	*Level*	*Range*
0	1	1	
1	01	-1	
2	001	2	
3	0001	-2	
…	…	…	A
10	000 0000 0001	6	
11	0000 0000 0001	-6	
12	0 0000 0000 0001	7	
13	00 0000 0000 0001	-7	
14	000 0000 0000 0001 xxxs	±8 ÷ ±15	B
15	0000 0000 0000 0001 xxxx xxxx xxxs	±16 →	C

Table 12: Codewords for *Lev-VLC0* Table

codewords can be divided in three subsets: one set (range A) composed by codewords with only a prefix, and two regions (range B and C) reserved for encoding levels with magnitude greater than 7 and 15, respectively (*escape* codes). In Table 13 is reported, for each subset, the pseudo-code implemented for calculating each codeword and its length. Codewords of the remaining *Lev-VLC1:6* tables, which are not reported for ease of brevity, are univocally identified once |*Level*| and *N* are known, according to the pseudo-code reported in Table 13.

The direct circuital implementation of this pseudo-code has allowed the elimination of all the seven *Lev-VLC* tables.

Lev-VLC	*Range*	*Coding Algorithm*
N=0	A	$code = \underbrace{0\ldots0}_{Prefix\_length}\ 1$ *Prefix_length=(|Level|<<1)-2+s Suffix_length=0* *Size= Prefix_length+1*
	B	$code = \underbrace{0\ldots0}_{Prefix\_length}\ 1\ \underbrace{\underbrace{xxx}_{Suffix\_length}\ s}_{Level\_suffix}$ *Prefix_length=14* *Suffix_length=3* *Size= 19* *Level_suffix= Binary value(|Level|)*
	C	$code = \underbrace{0\ldots0}_{Prefix\_length}\ 1\ \underbrace{x..x}_{Suffix\_length}\ s$ *Prefix_length=15* *Suffix_length=11* *Size= 28* *Level_suffix= |Level|-1-[15>>(N-1)]*
N=1÷6	All	$code = \underbrace{0\ldots0}_{Prefix\_length}\ 1\ \underbrace{x..x}_{Suffix\_length}\ s$ *if (|Level|-1)<[15<<(N-1)] then* *Prefix_length=(|Level|-1)>>(N-1)* *Suffix_length=N-1* *Size= Prefix_length+ Suffix_length* *Level_suffix= |Level-1|%2^N-1* *else* *as case VLC0 Range C* *end if*

Table 13: Coding algorithm for *Levels* symbol

For a luma block the encoding of *TotalZeros* employs 15 one-dimensional tables (*TZ-VLC0÷14*) selected according to the *TotalCoeff* value. The use of the ATE technique has allowed the elimination of the first table, corresponding to *TotalCoeff*=1, composed of 15 codewords, and the elimination of the last two tables, corresponding to *TotalCoeff*=14 and *TotalCoeff*=15, which however give negligible advantages being these table composed of 3 and 2 codewords respectively. While the codewords of the last two tables are derivable directly from the *TotalZeros* value, the codewords of the first table are obtained by implementing the pseudo-code in Table 14.

Coding Algorithm
if $TotalZeros = 15$ *then*
$suffix\_length = 0$
$prefix\_length = (TotalZeros >> 1) + TotalZeros(0)$
$code = \underbrace{0_1 \ldots 0_M}_{prefix} 1$
$size = prefix\_length + suffix\_length + 1$
else if $TotalZeros = 0$ *then*
$suffix\_length = prefix\_length = 0$
$code = size = 1$
else
$suffix\_length = 1$
$prefix\_length = (TotalZeros >> 1) + TotalZeros(0)$
$code = \underbrace{0_1 \ldots 0_M}_{prefix} 1 \,\&\, TotalZeros(0)$
$size = prefix\_length + suffix\_length + 1$

Table 14: Coding algorithm for *TZ-VLC0* Table

The remaining 12 tables have been constructed by using the technique proposed in [115]: briefly, the technique consists in creating classes of consecutive codewords having the same length and in allocating for each class only the first codeword. The reconstruction of the table requires just a circuitry for symbols mapping module in order to determine the offset of a codeword with respect to the first codeword of a class. Using this approach, we reduce the memory

requirement from 1173 bits to 348 bits, that means a memory reduction of about 70% at cost of just a combinatorial logic for the offset calculation needed to link the relative codeword into a class. Tables for chroma DC 2x2 blocks have not been elaborated since their small sizes would make inefficient any compression algorithm.

TotalCoeff	*TrailingOnes*	*Codeword for FLC Table*
1	0	0000 00
1	1	0000 01
2	0	0001 00
2	1	0001 01
2	2	0001 10
3	0	0010 00
3	1	0010 01
3	2	0010 10
3	3	0010 11
4	0	0011 00
…	…	…
TC	TR1	4b(TC-1)**&**2b(TR1)

Table 15: Subset of the codewords of the *CT-VLC3*=FLC Table

Also for the *Coeff_token* encoding has been used the technique in [115] for compressing 5 (three for luma and two for chroma) of the total 6 tables, addressed by *Total_Coeff* and *TrailingOnes*. The last table, instead, corresponding to the fixed length table (FLC table), has been eliminated. Indeed, as shown in Table 15, when *TotalCoeff* is not null, the codewords in the FLC table can be easily calculated as:

$$code = (TotalCoeff - 1) \,\&\, TrailingOnes\,.$$

Since, together with the *Lev-VLC* tables, the *CT-VLC* tables are the most memory demanding, it's interesting to estimate the effects of our approach on the area occupancy. This estimation is reported in Table 16, which shows both the original *CT-VLC* cost in terms of bit

	Tables	*Memory Cost for Standard Tables [bits]*	*Memory Cost for Compressed Tables [bits]*	*Saving [%]*
LUMA	CT-VLC0	1240	285	21.47
	CT-VLC1	1116	221	20.13
	CT-VLC2	868	98	17.31
	FLC	558	-	12.55
CHROMA	CT-VLC4	154	77	1.73
	CT-VLC5	510	187	7.26
	TOTAL	**4446**	**868**	**80.47**

Table 16: Memory cost for *Coeff_token* symbol encoding of our encoder compared to standard design

required for storing the codewords, and that employing our approach, that allows a memory cost reduction from 4.4kb to 868b.

Finally, to encode *Runbefore* symbol, seven one-dimensional tables are required, addressed by *ZeroLeft*. All these tables have been substituted by a combinatorial circuitry implementing the simple code in Table 17.

ZeroLeft	*Coding Algorithm*
<3	*if RunBefore(i)=0 then* *code=1* *size=1* *else* *code=Zeroleft(i)-RunBefore(i)* *size=Zeroleft(i)* *End*
≥3 and <6	*if RunBefore(i)≤6-Zeroleft(i) then* *code=3- RunBefore(i)* *size=2* *else* *code=Zeroleft(i)-RunBefore(i)* *size=3* *End*
=6	*if RunBefore(i)=0 then* *code=3*

	size=2 *elseif RunBefore(i)=1 then* *code=0* *size=3* *elseif RunBefore(i)=6 then* *code=4* *size=3* *else* *if LSB[RunBefore(i)]=0 then* *code=RunBefore(i)>>1* *else* *code= RunBefore(i)* *end if* *size=3* *end*
>6	*if RunBefore(i)<6 then* *code=7- RunBefore(i)* *size=3* *else* *code=1* *size=RunBefore(i)-3* *end*

Table 17: Coding algorithm for *RunBefore* symbol

5.1.4 Synthesis and Results

The proposed CAVLC encoder has been targeted on a low-end XC3S4000-4FG676 FPGA from the Xilinx Spartan 3 family [120]. The architecture has been described with the VHDL language and the Xilinx ISE 10.1i suite has been used for synthesis. Results of the synthesis in terms of hardware cost are reported in Table 18 for each module. Memory reduction in terms of number of bits needed to store the codewords of the encoding stage can be appreciated in Table 21 where the memory cost of each stage, when implementing ATE and the compression technique, are compared with that of the original tables. It's worth noting that the achieved memory reduction has allowed to store all the tables in the slice registers and that none external, distributed or RAM blocks have been used.

Pre-coding Stage	***Slice***	***Slice Register***	***LUTs***
Reorder & aux. data	310	243	386
TrailingOnes	174	12	285
Levels	254	20	481
TotalZeros	79	77	103
RunBefore	50	48	92
subtotal	*867*	*400*	*1347*
Encoding Stage			
Coeff_token	181	15	340
Levels	148	12	270
TotalZeros	58	8	112
RunBefore	69	12	131
subtotal	*456*	*47*	*853*
TOTAL	**1323**	**447**	**2200**

Table 18: Hardware cost profile of the proposed CAVLC encoder

Symbol	***Tables***	***Adopted Strategy***		***Memory Cost [STD vs Optimized]***	***Saving [%]***
		ATE	***Compressed***		
Levels	Lev- VLC0÷6	All	-	1.792Mb vs 0	100
RunBefore	RB- VLC0÷6	All	-	347b vs 0	100
TotalZeros	TZ- VLC0÷14 (Luma)	VLC0 VLC13 VLC14	VLC1÷12	1.209kb vs 384b	68.2
	TZ- VLC15÷17 (Chroma)	-	-		
Coeff_token	CT- VLC0÷3 (Luma)	VLC3	VLC0÷2	4.446kb vs 868b	80.47
	CT- VLC4÷5 (Chroma)	-	VLC4÷5		

Table 19: Memory cost for symbol encoding of the proposed CAVLC encoder compared to standard design

Encoding Stage	*LUTs (direct implementation)*	*LUTs (with ATE and Compression)*
Coeff_token	1098	340
Levels	1147	270
TotalZeros	357	112
RunBefore	375	131
Total	2977	853
SAVING	**71.34%**	

Table 20: LUTs cost profile of our second stage respect to a direct implementation

The overall hardware resource required from each module of the second stage is given in Table 20, where the hardware cost profile, in terms of LUTs, required by the proposed approach is compared with a straightforward, unoptimized implementation. Results show an overall area saving of about 71%, which accounts also for the additional circuitry required to reconstruct the codewords. It's worth observing that the achieved area reduction of the second stage has compensated for an unavoidable increasing in the area demand of the first stage, due to the employment of redundant circuitry and cascade logic.

In terms of performance, synthesis results give a maximum operating frequency of 63MHz, i.e. 15.9*ns* critical path delay, determined by the *Levels* detection and coding path, 41% of which are for logic elaborations and 59% for routing. The elaboration of a Luma 4×4 block and two 2×2 Chroma blocks, considering the worst (unrealistic) case that all coefficient are *Levels*, requires 16 clock periods and a latency of 254*ns*, distributed according to the temporal diagram in Fig. 60. Therefore, the elaboration of an entire 1080p video frame would require about 33*ms*.

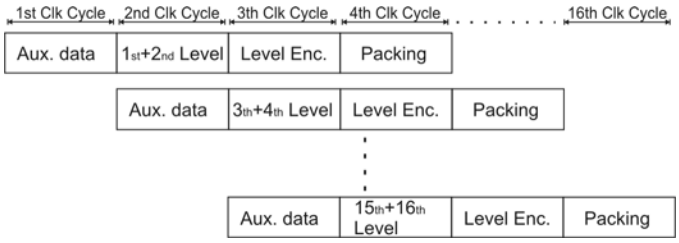


Fig. 60: Temporal diagram related to the elaboration of video block

The comparison between our encoder and other existing designs [110-114] in terms of hardware cost and processing speed is displayed in Table 21. As can be seen, the proposed encoder outperforms the others solutions presented in [113-114] where the area advantage is compensated by the lower speed which is insufficient for processing real-time HDTV frame for the same compressed bit-rate.

In spite of the lack of a detailed information from the datasheets about area cost of the single CAVLC encoder, which makes impracticable a direct comparison in terms of resource utilization respect to the IPs that the H.264 encoder industry offers, it is possible to note in Table 21 that our encoder is a good concurrent also to commercially available IP cores [110-111], enabling the highest quality HD H.264 encoding although it employs a low-end Spartan 3 FPGA.

	[110]	***[111]***		***[113]***	***[114]***	***Proposed***
FPGA	StratixII	Virtex4	Spartan 3-4	Virtex2		Spartan3
Freq. [MHz]	166	110	50	53	60	63
Max Spec.	720p 20fps	720p 30fps	4CIF 30fps	CIF 30fps	CIF 30fps	1080p 30fps
LUTs	N/A	N/A	N/A	1733	1533	2200

Table 21: Comparison with other published solutions

Conclusions

The research activity reported in this thesis mainly concerns with the development of a new, self-consistent, analytical model to describe the electrical behavior of 4H-SiC power diodes. The basic theory of the chemical and physical characteristics of the Silicon Carbide has been introduced by referring to the models developed in the last years for this innovative material. Proceeding in this way, the extraction of fundamental parameters of Silicon Carbide has been allowed, and, at the same time, the analysis of their impact on static device performance has been feasible. The developed d.c. analytical model has been discussed and also both numerical and experimental results have been reported to show its accuracy. Further, to give more evidence of the versatility of the model to describe the *I-V* curve of a diode with generic structure, also comparisons with already published data have been done. The model results able to accurately predict the carrier transport in diffused regions as function of the injection level and turns also useful for better understanding the influence of physical parameters, some of which depend in a significant way from the processed material.

The dynamic model has been then introduced; in particular, an improved method of the conventional OCVD technique has been shown, justifying the development of a new model to accurately describe the relationships between the several parameters influencing the lifetime measurements and to give a correct physical interpretation of the measurement procedure. The model, in fact, resolves some ambiguities reported in the literature, such as the stated inapplicability of the OCVD method on thick epitaxial layers, the reasons of the observed nonlinear decay of the voltage with time, and the effects of junction properties on voltage transient.

The overall model performances are compared to both device simulations and experimental results performed on Si and 4H-SiC rectifier structures with various physical and electrical characteristics. From the comparisons, the model show good predictive capabilities

for describing, for a generic diode under test switched from an arbitrary forward-bias condition, the spatial distribution of the majority and minority carrier lifetimes, besides the spatial minority carrier distribution in the epitaxial layer, at any injection regime.

In the future work, it is expected that the developed model will be a computationally efficient method for investigating more complex SiC bipolar power devices embedding a p-i-n structure.

Moreover, a further research activity was developed: the design of a new CAVLC architecture, particularly aimed to be implemented with FPGAs. It was also demonstrated that the proposed solution outperforms encoders already presented in literature, both in terms of area reduction and image processing speed.

APPENDIX A

SYMBOLS	
D_a	Ambipolar diffusion coefficient ($cm^2\ s^{-1}$)
D_{nA}	Electron diffusion constant into the anode ($cm^2\ s^{-1}$)
D_{pC}	Hole diffusion constant into the cathode ($cm^2\ s^{-1}$)
$D_{n,p}$	Carrier diffusion constant into the base ($cm^2\ s^{-1}$)
E_C (E_V)	Conduction (valence) band edge (eV)
$E_{Fn,p}$	Fermi energy level (eV)
E_a (E_d)	Acceptor (donor) impurity energy level (eV)
E_g	Bandgap energy (eV)
E_{G0}	Bandgap energy at the reference temperature (eV)
g_d (g_a)	Degeneracy factor of conduction (valence) band
J_B	Recombination current density into the neutral base region (A cm^{-2})
J_D	Total current density (A cm^{-2})
J_{nA}	Sum of the J_{RG} and the J_{np+} current densities (A cm^{-2})
J_{RG}	Recombination current density into the $p+/n-$ depletion layer (A cm^{-2})
J_{pC}	Hole current density into the cathode (A cm^{-2})
J_{np+}	Electron current density into the anode (A cm^{-2})
k	Boltzmann constant (eV K^{-1})
L_a	Ambipolar diffusion length in the base (μm)
L_{nA}	Electron diffusion length in the anode (μm)
L_{pC}	Hole diffusion length in the cathode (μm)
n	Electron concentration (cm^{-3})
N	Local impurity concentration (cm^{-3})
N_{aA}	Active acceptor concentration into the anode (cm^{-3})
N_B	Doping density in the base (cm^{-3})
$N_{C,V}$	Effective density of states (cm^{-3})
N_d (N_a)	Donor (acceptor) concentration (cm^{-3})
N_d^+ (N_a^-)	Ionized donor (acceptor) concentration (cm^{-3})
N_{dC}	Active donor concentration into the cathode (cm^{-3})
N_{eff}	Effective doping (cm^{-3})
N_i	Intrinsic carrier concentration (cm^{-3})
$N^{REF}_{crit\ n,p}$	Reference doping concentration in the carrier lifetime expression (cm^{-3})
$N_{n,p}$	Caughey and Thomas reference doping concentration (cm^{-3})

p	Hole concentration (cm^{-3})
q	Electron charge (A s)
R_B	Injection-dependent resistance of the modulated base (Ω cm^2)
R_{n+} (R_{p+})	Distributed resistance of the n_+ (p_+) region (Ω cm^2)
R_S	Distributed contact resistance (Ω cm^2)
S_{P+} (S_{N+})	Anode (cathode) recombination velocity (cm s^{-1})
T	Temperature (K)
T_o	Reference temperature (K)
U	Recombination rate (s^{-1} cm^{-3})
V_D	Voltage bias (V)
V_T	Thermal voltage (V)
V_{bi}	Built-in voltage of the p_+/n_- junction (V)
V_{nn+}	Voltage drop across the n_-/n_+ junction (V)
V_{pn}	Voltage drop across the p_+/n_- junction (V)
W_A	Anode width (μm)
W_B	Base width (μm)
W_C	Cathode width (μm)
W_{SC} p_+/n_-	Depletion layer width (μm)
$\alpha_{n,p}$	Caughey and Thomas mobility model fitting coefficient
$\beta_{n,p}$	Caughey and Thomas mobility model fitting coefficient
$\gamma_{n,p}$	Caughey and Thomas mobility model fitting coefficient
$\delta_{n,p}$	Caughey and Thomas mobility model fitting coefficient
ΔE_a	Energy distance of acceptor level from valence band (eV)
ΔE_d	Energy distance of donor level from conduction band (eV)
ΔE_{gA}	Effective bandgap narrowing into the anode (eV)
ΔE_{gC}	Effective bandgap narrowing into the cathode (eV)
ε	Dielectric constant (F cm s^{-1})
ε_r	Specific dielectric constant
$\mu_{0n,p}$	Carrier mobility at the reference temperature (cm^2 V s^{-1})
$\mu_{n,p}$	Carrier mobility (cm^2 V $s^{-1}{}_1$)
ξ_D (ξ_A)	Donor (acceptor) ionization grade
τ_a	Ambipolar lifetime in the base (s)
$\tau_{n,p}$	Carrier lifetime into the base (s)
τ_{nA}	Carrier lifetime into the anode (s)
τ_{pC}	Carrier lifetime into the cathode (s)

APPENDIX B

The third order polynomial to be solved for obtaining $p(W_B)$ as a function of $p(0)$ is:

$$\left[\frac{p(W_B)}{p(0)}\right]^3 + a\left[\frac{p(W_B)}{p(0)}\right]^2 + b\left[\frac{p(W_B)}{p(0)}\right] + c = 0 \qquad \text{(A-1)}$$

with coefficient given by:

$$a = \left[S_{N+}(1+2b) + \frac{2D_n}{L_a}\coth\left(\frac{W_B}{L_a}\right) + D_p \frac{1+\dfrac{p(0)}{p(0)+N_B}}{L_a \sinh\left(\dfrac{W_B}{L_a}\right)} \right] \frac{N_B}{S_{N+}(1+b)p(0)} \qquad \text{(A-2)}$$

$$b = \left\{ \left[S_{N+}b + \frac{D_n}{L_a}\coth\left(\frac{W_B}{L_a}\right) \right] \frac{N_B}{p(0)} - S_{P+}\left[1+\left(1+\frac{1}{b}\right)\frac{p(0)}{N_B}\right] + \right.$$
$$- \frac{J_{RG}}{qp(0)}\left[1+\frac{\mu_p p(0)}{\mu_n\left(p(0)+N_B\right)}\right] - \frac{D_p}{L_a}\left[1+\frac{p(0)}{p(0)+N_B}\right]\coth\left(\frac{W_B}{L_a}\right) +$$
$$\left. - 2\frac{D_n}{L_a \sinh\left(\dfrac{W_B}{L_a}\right)} \right\} \frac{N_B}{S_{N+}(1+b)p(0)} \qquad \text{(A-3)}$$

$$c = -\frac{D_n \left[\frac{N_B}{p(0)}\right]^2}{L_a \sinh\left(\frac{W_B}{L_a}\right) S_{N+}(1+b)}. \qquad \text{(A-4)}$$

The analytic solution of (A-1) results [63]:

$$p(W_B) = \left\{ 2\sqrt{\frac{\left|b - a^2/3\right|}{3}} \cos\left[\frac{\pi}{3} - \frac{1}{3}\arctan\left(\frac{2\sqrt{|h_2|}}{|h_1|}\right)\right] - \frac{a}{3} \right\} p(0) \quad \text{(A-5)}$$

with:

$$h_1 = 2\left(\frac{a}{3}\right)^3 - \frac{ab}{3} + c$$

$$h_2 = -\frac{1}{3}\left(\frac{ab}{6}\right)^2 + \left(\frac{c}{2}\right)^2 + \left(\frac{b}{3}\right)^3 + \left(\frac{a}{3}\right)^3 c - \frac{abc}{6}.$$

APPENDIX C

Using the carrier distribution (3-4) in (3-12), the resulting ohmic resistance $R_B = \int_{0^+}^{W_B} \frac{dx}{q\left[\left(\mu_n + \mu_p\right)p(x) + \mu_n N_B\right]}$ can be written as:

$$R_B = \frac{2L_a}{q(b+1)\mu_p\left(k_1 + p(0^+)\right)\sqrt{-D}}\left[arctg\left(\frac{e^{W_B/L_a} + k_2}{\sqrt{-D}}\right) - arctg\left(\frac{1+k_2}{\sqrt{-D}}\right)\right] \quad \text{(B-1)}$$

if $D \le 0$; else:

$$R_B = \frac{L_a}{q(b+1)\mu_p\left(k_1 + p(0^+)\right)\sqrt{D}}\ln\left(\frac{\left(e^{W_B/L_a} + k_2 - \sqrt{D}\right)\left(1 + k_2 + \sqrt{D}\right)}{\left(e^{W_B/L_a} + k_2 + \sqrt{D}\right)\left(1 + k_2 - \sqrt{D}\right)}\right) \quad \text{(B-2)}$$

if $D > 0$,

where $k_1 = \frac{p(W_B) - p(0^+)\cosh(W_B / L_a)}{\sinh(W_B / L_a)}$, $k_2 = \frac{bN_B}{\left(b+1\right)\left(k_1 + p(0^+)\right)}$ and $D = k_2^2 + \frac{k_1 - p(0^+)}{k_1 + p(0^+)}$.

APPENDIX D

By referring to the sum of electron and hole continuity equations:

$$\frac{\partial(J_N + J_P)}{\partial x} = q\left(\frac{\partial(n-p)}{\partial t}\right) + q(U_N - U_P) \qquad \text{(C-1)}$$

by assuming $U_N = U_P$ and neglecting the small difference of the electric gradients along the neutral epilayer, it follows that the total current must be zero, that is:

$$\frac{\partial J_N}{\partial x} + \frac{\partial J_P}{\partial x} = 0 \qquad \text{(C-2)}$$

By writing the electron and hole current densities in terms of the diffusion and drift components, Eq. (C-2) becomes:

$$(D_p - D_n)\frac{\partial^2 p_S}{\partial x^2} = (\mu_p + \mu_n)\frac{\partial p_S}{\partial x} \qquad \text{(C-3)}$$

where $D_{n,p}$ and $\mu_{n,p}$ are assumed spatially constant. Since eq. (C-3) is verified contemporaneously at $x=0^+$ and $x=W_B$, it is valid the following equivalence:

$$\frac{\left.\frac{\partial^2 p_S}{\partial x^2}\right|_{x=0^+}}{\left.\frac{\partial^2 p_S}{\partial x^2}\right|_{x=W_B}} = \frac{\left.\frac{\partial p_S}{\partial x}\right|_{x=0^+}}{\left.\frac{\partial p_S}{\partial x}\right|_{x=W_B}} \qquad \text{(C-4)}$$

By using the general solution of (4-10) in Eq. (C-4):

$$\frac{B}{C} = \frac{B\cos\left(\frac{k}{\sqrt{D_a}}W_B\right) + C\sin\left(\frac{k}{\sqrt{D_a}}W_B\right)}{-B\sin\left(\frac{k}{\sqrt{D_a}}W_B\right) + C\cos\left(\frac{k}{\sqrt{D_a}}W_B\right)} \qquad \text{(C-5)}$$

Since $B \neq C$, Eq. (C-5) is verified only if $\cos\left(\frac{k}{\sqrt{D_a}}W_B\right) = 1$ and $\sin\left(\frac{k}{\sqrt{D_a}}W_B\right) = 0$, which implies $k_n = \frac{n\pi}{W_B}\sqrt{D_a}$ with n=0, 1, 2 ….

APPENDIX E

Using (3-4) for evaluating the variation of the recombination current under stationary conditions:

$$\Delta J_P^0(x) = J_P^0(x) - J_P^0(W_B) = q\int_x^{W_B} \frac{p^0(x)}{\tau_a}\,dx \qquad \text{(D-1)}$$

$\Delta J_P^0(x)$ can be expanded into Fourier-series and compared, term by term, with the corresponding spatial variation calculated at $t=0^+$ from (4-10):

$$\Delta J_P^0(x,0^+) = J_P(x,0^+) - J_P(W_B,0^+) = q\int_x^{W_B} \frac{\partial p_S(x,0^+)}{\partial t} + \frac{\partial p_S(x,0^+)}{\tau_a}\,dx$$

with $p_S(x,0^+)$ expressed from (4-11). From this comparison, the coefficients B_n and C_n which compare in (4-11) can be written as:

$$B_n = \frac{W_{EPI}}{L_{AMB}(n\pi)^2} \times \frac{p^0(0^+) - p^0(W_{EPI})\cosh\left(\frac{W_{EPI}}{L_{AMB}}\right)}{\sinh\left(\frac{W_{EPI}}{L_{AMB}}\right)} \times \left[(-1)^n - 1\right] +$$

$$+ \frac{L_{AMB}}{W_{EPI}\left[1+\left(\frac{L_{AMB}n\pi}{W_{EPI}}\right)^2\right]} \times \left\{ \frac{p^0(W_{EPI})\left[\cosh\left(\frac{W_{EPI}}{L_{AMB}}\right)(-1)^n - 1\right] + p^0(0^+)\left[\cosh\left(\frac{W_{EPI}}{L_{AMB}}\right) - (-1)^n\right]}{\sinh\left(\frac{W_{EPI}}{L_{AMB}}\right)} \right\}$$

$$C_n = \frac{p^0\left(0^+\right)}{n\pi} \times \left[\frac{\cosh\left(\frac{W_{EPI}}{L_{AMB}}\right)(-1)^n - 1}{1+\left(\frac{L_{AMB}n\pi}{W_{EPI}}\right)^2} \right] + \frac{(-1)^n}{n\pi} \times \frac{p^0\left(W_{EPI}\right) - p^0\left(0^+\right)\cosh\left(\frac{W_{EPI}}{L_{AMB}}\right)}{1+\left(\frac{L_{AMB}n\pi}{W_{EPI}}\right)^2}$$

Related Publications

International

- S. Bellone, **L. Freda Albanese**, and G.D. Licciardo, "A self consistent Model of the OCVD Behavior of Si and 4H-SiC P+NN+ Diodes", IEEE Trans. on Electr. Dev., Vol. 56; pp. 2902-2910, 2009.

- S. Bellone, **L. Freda Albanese**, and G.D. Licciardo, "Limitations of the Open-Circuit Voltage Decay technique applied to 4H-SiC diodes", Semiconductor Conference, 2009, CAS-2009, Vol. 2, pp. 409-412, Sinaia (Romany), 12-14 Oct. 2009.

- F. Pezzimenti, **L. Freda Albanese**, S. Bellone, and F.G. Della Corte, "Analytical model for the forward current of Al implanted 4H-SiC p-i-n diodes in a wide range of temperatures", IEEE Bipolar/BiCMOS Circuits and Technology Meeting, 2009, BCTM-2009, pp. 214-217, Capri (Italy), 12-14 Oct. 2009.

- S. Bellone, F.G. Della Corte, L. Di Benedetto, **L. Freda Albanese**, and G.D. Licciardo, "A Self-Consistent Model of the static and switching behaviour of 4H-SiC Diodes", Semiconductor Conference, 2010, CAS-2010, pp. 405-408, Sinaia (Romany), 11-13 Oct. 2010.

- **L. Freda Albanese** and G.D. Licciardo, "High Speed CAVLC Encoder Suitable for Field Programmable Platforms", 7th IEEE International Conference on Signals and Electronic Systems-ICSES 2010, pp. 327-330, Gliwice (Poland), 7-10 Sept. 2010.

- **L. Freda Albanese** and G.D. Licciardo, "An Area Reduced Design of the Context-Adaptive Variable-Length Encoder Suitable for Embedded Systems", 5th International Symposium on I/V Communications and Mobile Network (ISVC), pp. 1-4, Rabat (Marocco), 30 Sept.-2 Oct. 2010.

- S. Bellone, F.G. Della Corte, **L. Freda Albanese**, and F. Pezzimenti,, "An analytical model of the forward I-V characteristics of 4H-SiC p-i-n diodes valid for a wide range of temperature and current", IEEE Trans. On Power Electr. (in print).

- **L. Freda Albanese** and G.D. Licciardo, "Design of a Context-Adaptive Variable Length Encoder for Real-time Video Compression on Reconfigurable Platforms", IEEE Computer Society (submitted).

National

- **L. Freda Albanese** and G. D. Licciardo, "Architecture Design of CAVLC Encoder for Real-Time Applications", Libro GE08, June 2008-Otranto.

- **L. Freda Albanese**, S. Bellone, and G.D. Licciardo, "An area efficient architecture of the context adaptive variable length coding for video applications", Libro GE09, June 2009-Trento.

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