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TESI DI DOTTORATO

Analysis and Design of 4H-SiC Bipolar Mode Field Effect Power Transistor (BMFET)

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To my love

Contents

List of Figures

Acknowledgments

Although it was very hard and difficult at the beginning of these three years, I had the opportunity to work side-by-side or, better, *pen-by-pen* with one of the better experts in electron devices, from which I tried to *absorb* some of his boundless knowledge. What I learned cannot be substituted by other experiences. He was not a tutor, but more a *master*. Thanks You, Prof. Salvatore Bellone.

Along my course I met many people with which I discussed, compared, grew up. So, I would like to thank the people of my group and of Laboratory I7, Gian Domenico, Mario, Rosalba and Prof. Rubino, but also Prof. Della Corte, Dr. Roberta Nipoti and Dr. Michelina Festa. Moreover, all my colleagues of XI Ciclo and, in specially way, Dr. Giovanni Massa which has *lost* part of his time for my talk.

I would to thank my family.

... and to the only person who believed in me, supported me and knows the passion that I put into this work. *My Love, Chiara*.

Abstract

Analysis and design of a new 4H-SiC bipolar power transistor are the main topics of this Ph.D. thesis. The device is the Bipolar Mode Field Effect Transistor (BMFET) and exploits the electric field due to the channel punching-through in order to have a *normally-off* behavior and the minority carrier injection from the Gate regions to the channel in order to obtain the channel conductivity modulation. The structure of the transistor is oxide-free and its advantages are due to the lower conduction resistance, to the higher output current density and blocking voltage and to the elevated switching frequency, which make it competitive with commercial 4H-SiC JFETs or BJTs.

These activities, which have been completed with the definition of the main process steps and of the mask layouts, are supported by a technology activity and by an intense modeling activity of BMFET electrical characteristics, which has been validated by comparisons with the results of numerical simulator (ATLAS Silvaco) and the measures of commercial devices having a similar structure, like Vertical Junction Field Effect Transistors.

In the former activity, in order to obtain an integrated free-wheeling diode in antiparallel configuration to BMFET, an original 4H-SiC Schottky rectifier has been fabricated; precisely, for the first time in the literature, DiVanadium PentOxide (V_2O_5), a Transition Metal Oxide, has been used as anode contact of the rectifier. The device is a heterojunction between a thin V_2O_5 layer, which is thermally evaporated and has a thickness of around *5nm*, and a 4H-SiC *n*-type low doped epilayer. By analyzing the J_D-V_D and C_D-V_D curves, the structure has a rectifier behavior with a high/low current ratio higher than seven order of magnitude and its transport mechanism is described by the thermoionic emission theory characterized by a Schottky barrier height and an ideality factor

between *0.78eV* and *0.85eV* and between *1.025* and *1.06*, respectively, at room temperature.

Because the gate doping concentration greatly influences the BMFET performances, as input resistance, DC current gain and blocking voltage, Aluminum ion implantation process, used to realize the Gate regions, is strongly analyzed in terms of the dose concentrations and of the annealing temperature. It will show as the necessity of a low BMFET on-resistance, which is possible with highly conductive gate regions in order to permit high injection levels of the minority carriers, is counteracted by the Aluminum incomplete ionization in 4H-SiC. This phenomenon together with the band-gap narrowing effect limits the hole carrier density from gate to channel. The analysis, in collaboration with the Institute for the Microelectronics and Microsystems (IMM) of CNR in Bologna, Italy, consists to reveal the effects of various different doses at different temperature annealing (*1920K* and *2170K*) on the gate injection efficiency and on the input current density.

Since the introduction of the first normally-off Si JFET in '80 years, the description of the potential barrier height into the channel has been unresolved due to the complex relations with the channel geometry and bias conditions. In the second activity an analytical model of the potential barrier height in the channel is proposed and compared with the numerical simulation results by changing the channel length and width, respectively in the range $0.1 \div 6\mu m$ e $0.5 \div 3\mu m$, the channel doping concentration, between $10^{14} \div 10^{17} cm^{-3}$, and the output and input bias voltages. Moreover, it has been also validated by using Silicon as semiconductor material, permitting to extend it to other devices with similar structures, like BSITs, VJFETs and SITs. From this model the trans-characteristics of the transistor in sub-threshold condition and in unipolar conduction is developed and its validity is verified comparing its results with numerical simulations and experimental data.

Finally, the analysis of the input diode during the switching-off has been performed because the switching capability of the BMFET depends on the storage charge into the channel during the "on" state. The result is the development of an analytical model that describes the spatial distributions of the electric field, of the minority carrier

concentration and of the carrier current densities into the epilayer at each instant during the switching, in addition obviously to the current and voltage transients. It is shown as the combination of this model with another static model just developed in a previous Ph.D. thesis is an useful instrument to understand how physical parameters, which are dependent on the manufacturing processes, as carrier life-time and doping concentrations, can affect the dynamic behavior.

Thesis Outline

After a brief introduction on the state-of-art of the 4H-SiC power devices, in Chapter 1 BMFET operating principle is shown with the motivations and the interests in this kind of transistor.

Chapter 2 is dedicated to the analysis of the channel potential barrier and to the comparisons between the results of the proposed model and of the numerical simulator for numerous values of the physical and geometrical channel parameters and of voltage bias conditions.

The model of I_D-V_G characteristics in sub-threshold condition have been developed from the previous model and shown in Chapter 3. Its accuracy to predict the electrical behaviour of simulated and commercial structures is reported.

From the analysis of the switching performances the influence of the intrinsic *p-i-n* diode is highlighted and in Chapter 4 the dynamic model of the reverse recovery of the diode is shown.

Chapter 5 covers on the results of the analysis of the Aluminium ion implantation doses which can affects the performances both of the BMFET due to the Gate injection efficiency and of the maximum *p−i−n* diode current density.

The mask layouts and the mainly process steps to realize a BMFET transistors are described in Chapter 6.

Finally, in Chapter 7 the fabrication process and the experimental results of the free-wheeling V_2O_5 diode in are reported. Diode current−voltage and capacitance−voltage curves have been used to extract the main physical parameters of the Schottky Barrier Junction, i.e. barrier high, ideality factor and serie resistance. The measurements have been performed in a temperature range between *100K* and *425K*.

Chapter 1

4H-SiC and Bipolar Mode Field Effect Transistor

In this chapter an overview of 4H-SiC power transistors and of its main physical parameters precedes the description of the operating principles of Bipolar Mode Field Effect Transistor (BMFET) in order to highlight the motivations and advantages of this kind of device. Results of numerical simulation are used as instruments of investigations.

1.1 4H-SiC for High Power Transistors

Silicon technology has always dominated the power electronic in terms of semiconductor devices, which are able to operate in a broad spectrum of power levels and frequencies. Two-terminals devices, like *p-i-n* and Schottky Rectifiers, and three-terminals devices, like Gate Turn-Off (GTO) Thyristors or Bipolar Junction (BJT), Insulated-Gate Bipolar (IGBT) and Field Effect (FET) Transistors, exist. Each of them has its own field of application ranging from communications to power transmissions as identified by the capability of managing power and frequency of operation as shown in Fig.1.1, including variable speed motion control, electric vehicle drives, uninterruptible power supplies (UPS), up to the high power distribution, transmission and traction markets. However, the need for devices with higher switching

frequency, high voltage capability and small area is growing, especially, for military and advanced power conversion. Additionally, the intrinsic physical properties of Silicon limits the operating junction temperature to *423K* and it means the mandatory employment of cooling system, which increases the cost and the circuit area, and the difficulty to satisfy the require performances in harsh environments.

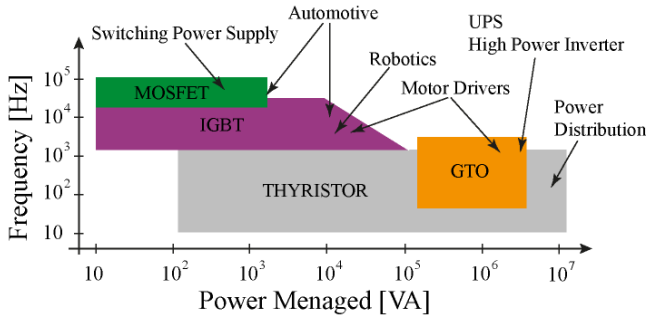

Fig.1.1. Application of Silicon power devices.

Therefore, it needs to consider other semiconductors with better performances respect to Silicon in terms of critical electric field (E_C), saturation velocity (v_{SAT}) and thermal conductivity (λ). These are the wide band-gap semiconductors, in particular Gallium Nitride (GaN) and Silicon Carbide (SiC), whose most relevant physical parameters are compared in Table 1.1.

PARAMETERS	UNITS	Si	3C-SiC	4H-SiC	6H-SiC	GaN
ε_R		11.9	9.72	9.66	9.66	8.9
χ	$[eV]$	4.05	-	3.7	3.4	4.1
$E_G^{300°K}$	$[eV]$	1.1	2.36	3.26	3	3.39
E_C	$[MV/cm]$	0.3	~1	$3 \div 5$	$3 \div 5$	~5
v_{SAT}	$[x10^7 cm/s]$	1	2	2.2	1.9	2.6
$\mu_n\|_{N=10^{16}cm^{-3}}$	$[cm^2V^{-1}s^{-1}]$	1500	≤ 800	≤ 900	≤ 400	≤ 1000
$\mu_p\|_{N=10^{16}cm^{-3}}$	$[cm^2V^{-1}s^{-1}]$	480	≤ 320	≤ 120	≤ 90	≤ 200
λ	$[Wcm^{-1}K^{-1}]$	1.5	3.2	3.7	3.6	1.3

Table1.1. Electrical parameters of some wide band-gap materials compared with Si [1], [2].

With respect to Silicon, the higher critical electric field of wide band-gap semiconductors can lead to power devices with higher breakdown voltages, or, for the same breakdown voltage, too much thinner drift layer that, in conjunction with the high v_{SAT}, reduces the storage charged and, hence, the delay intervals increasing the switching frequency of devices. Considering also the higher thermal conductivity in the case of 4H-SiC, SiC devices operate at very high temperatures and high-medium power densities at medium-high frequency switching applications [3]–[4]. Moreover, SiC dissemination has been favored: *i)* by fabrication processes very similar to Si, being SiC the only wide band-gap semiconductor with a native oxide (SiO_2); *ii)* by the availability of high-purity commercial wafers [5]; *iii)* by the continuous technology improvement from the epitaxial growth to the ion implantation processes.

Depending on the stacking order of the Silicon and Carbon atoms, over 200 crystal structures exist, which are called polytype, but a few of them are reproducible in laboratory, stable and with interesting physical properties for electronic applications: they are 3C–SiC, 6H–SiC and 4H–SiC (see Tab. 1.1). If 3C–SiC wafers suffer of low quality of the substrate, 6H–SiC and 4H–SiC wafers are commercially available, but the last has a higher carrier mobility, which is preferred to reduce the conduction losses.

In order to design new devices by using new semiconductor, the role of numerical device simulators is fundamental and, although the same general equations used for modeling conventional semiconductors can be applied to wide band–gap, a number of peculiar phenomena, having a marginal influence on Si device operations, must be accounted for. In particular, effects like incomplete ionization of doping atoms, band-gap narrowing, mobility along with their temperature and doping dependences must be accurately modeled. In this thesis each of these phenomena with the relative physic model are accurately considered and recapitulated in APPENDIX A.

In spite of the favorable aspects, at present, 4H–SiC is employed in a reduced number of commercial power devices, like Schottky diodes, FETs and BJTs. Schottky diodes are commercially available for the rectifiers market, reaching maximum voltage and current of

1200V and *40A* [5]–[8], while state-of-the-art of MOSFETs [5], JFETs [9] and BJTs [10] are capable to manage blocking voltage between *1200V* and *1700V* and forward current up to *100A*. The capability to realize a gate oxide of good quality has defined the success of MOSFETs as the main power transistor in Si technology due to the high input impedance, which simplifies the design of the control circuits. For this reason, it seems to be the most promising device, but the scarce quality of the SiO_2/SiC interface limits its large diffusion. Although JFETs and BJTs are commercially available, they are still under study in order to improve both the technology and the performances, which are superior for high power applications, thanks to the lower forward voltage drop and higher blocking voltages than Silicon counterparts.

This scenario gives an idea of the excitement around SiC that involves both industries and research institutes. In the following, the main 4H-SiC power devices are shown.

1.1.1 Unipolar devices

Unipolar devices have been the first topology developed and commercialized in 4H–SiC. They are Schottky rectifiers and FETs family: MOSFETs and JFETs.

1.1.1.1 Schottky rectifiers

Schottky Barrier Diodes are metal-semiconductor junctions and the diode current-voltage dependency is due to the potential barrier at the interface. By choosing the metal with the appropriate work function, a low forward voltage is allowed by lowering the potential barrier. Otherwise, a reduced potential barrier determines a higher leakage current and, hence, a lower blocking voltage. A trade-off between the conduction losses and the reverse conditions is required [11], especially at high temperature conditions. Due to the absence of the minority carriers, the switching off is defined by the space charge capacitance, proposing these devices for high frequency applications. Being the first 4H–SiC device commercially available, maximum voltage and current are *1200V* and *40A* [5]–[8], respectively.

1.1.1.2 JFET

The first proposed commercial transistor is the unipolar Junction Field Effect Transistor from SemiSouth Laboratories Inc. [9], whose investigation shows good blocking and dynamics behaviors [12]–[14], but the typical problems of an unipolar transistor, which concern high R_{ON} and low current density comparing with those of the bipolar family, currently stay. In Fig.1.2 the cross-section view of a Vertical channel-JFET is reported and, depending on the channel width, normally-on or normally-off behavior are possible due to the channel pinched-off at zero bias condition. This topology does not use gate oxide avoiding problems from oxide reliability and mobility reduction by interface states, which makes VJFET interesting also for high temperature applications. Although JFETs with interesting performances have been developed (V_{BL}=*1700V*, R_{ON}=*2.77mΩcm*^{2} [15] and V_{BL}=*1900V,* R_{ON}=*2.8mΩcm*^{2} [14]), the capability to reach very high blocking voltage is limited by the conduction losses that increase with it due to the unipolar conduction, as for example the device in [13] has V_{BL}=*11kV* and R_{ON}=*130mΩcm*^{2}.

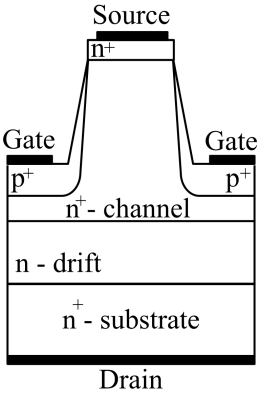

Fig.1.2. Cross section view of a Normally-Off VJFET structure.

1.1.1.3 MOSFET

Thanks to the SiO_2 formation, MOSFETs have been developed in 4H–SiC in different topology [16], which can be summarized in

Double Implantation MOSFET Fig 1.3a and UMOSFET Fig 1.3b. Both of them suffer of: *i)* premature failures at high reverse voltages, due to the high electric field at the oxide interface; *ii)* the injection of hot carriers into the oxide due to the smaller band offset among the conduction bands of the two materials; *iii)* the scarce quality of the interface, which induces a weak control of the channel mobility and of the threshold voltage.

DIMOSFET is realized by a Double Implantation for the *p*-well and n^+-source regions and, then, by an oxide formation for the gate. This structure is planar and easily realizable, but is also limited, in addition to the aforementioned problems, by the reach-through problem into the *p*-well region, which limits the blocking voltage capability.

The second structure is realized by trenching the $p-$well and n^+-source epilayers with a U-shaped and by growing a native oxide for the gate oxide. Although its specific on-resistance is lower than DIMOSFETs, its limitation is due to the extremely high electric field at the corners of the trench, that causes a poor long term reliability.

Until now, DIMOSFETs with $V_{BL}=1.2kV$ and $R_{ON}=9m\Omega cm^2$ [17] have been developed as well as UMOSFETs with $V_{BL}=1.4kV$ and $R_{ON}=15.7m\Omega cm^2$ [18], but, like JFETs, it is needed a tread-off between conduction loss and blocking voltage as shown in [19] where a *10kV*-class DMOSFET has a ON-specific resistance of $123m\Omega cm^2$.

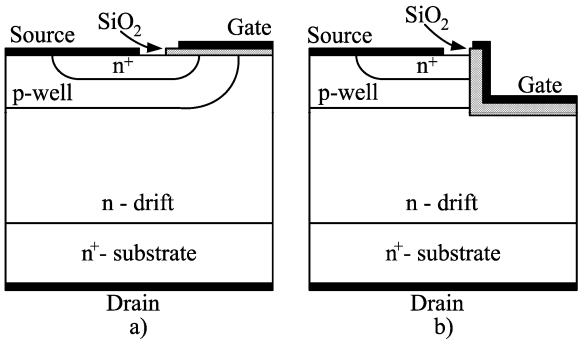

Fig.1.3. Cross section view of DIMOSFET (a) and UMOSFET (b) structures.

1.1.2 Bipolar devices

Bipolar devices are interesting for high voltage applications due to the conductivity modulation phenomena, which permits to have a thick and low-doped drift layer, in order to support high blocking voltages in the range of *10kV*, with very low ON-specific resistances, less than $100m\Omega cm^2$. Naturally, the injection of the minority carriers needs a maintenance input current during the on-state, making complex the gate driver circuit, and the injected carriers into the drift layer have to be extracted during the switch-off of the device, causing a poor dynamic performance.

1.1.2.1 *p-i-n* rectifiers

p-i-n power diode is a vertical structure in which two high doped p^+ (anode) and n^+ (cathode) regions are divided by a high resistive *n*-type layer. In reverse bias the voltage mainly drops in the intermediate region, indeed, in forward conditions the ON-resistance of the drift region is lowered by the minority carriers injection from the anode. The former is known as punch-through configuration, indeed, the second is the modulation conductivity phenomena, which is peculiar to the bipolar devices. Otherwise, *p-i-n* diode operates at low switching frequency due to the slow reverse recovery, which is necessary to remove the stored carrier from the drift layer, and shows a high forward overvoltage during the switch-on due to the low doping concentration of the *i*-region.

Thank to the higher critical electric field, 4H-SiC *p-i-n* diodes have drift region with higher doping concentration and thinner thickness than Si counterparts, improving dynamic and static performances, in addition to operate at higher temperature. Although high-voltage 4H-SiC *p-i-n* diodes have been fabricated having blocking voltages of *6.5kV* [20] or *10kV* [21] and $R_{ON}=34m\Omega cm^2$ at $J_D=100A/cm^2$, their performances are degraded by the nucleation of the Schockley Stacking Faults from the basal plane dislocations in the substrate during forward bias stress [22]. This phenomena is known as bipolar degradation and consists in a reduction of the carrier life-time

and/or in an increasing of the forward diode voltage drop due to the creation of recombination centers.

1.1.2.2 BJT

Typical silicon BJTs architectures are not easily realized in SiC, mainly due to the lacking of a reliable technology for the activation of acceptor species. On the other side, if the doping of p-type base region were done by implantation, the lifetime of the carriers would be very low, giving rise to a decrease in the obtainable current gain. To avoid these drawbacks, the architecture of bipolar transistors proposed in the literature relies on multiple epitaxial layers [23]-[25] as in Fig. 1.4, but it presents high manufacturing costs.

Actually, BJTs have been developed with $V_{BL}=1.2kV$, $R_{ON}=5.2m\Omega cm^2$ and $h_{FE}=60$ [26], $V_{BL}=2.8kV$, $R_{ON}=4.5m\Omega cm^2$ and $h_{FE}=55$ [27], $V_{BL}=9.2kV$, $R_{ON}=33m\Omega cm^2$ and $h_{FE}=7$ [28].

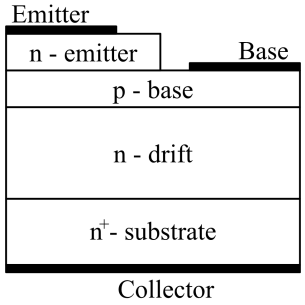

Fig.1.4. Cross section view of a BJT structure.

1.1.2.3 IGBT

Insulated Gate Bipolar Transistor combines the low forward voltage drop due to the conductivity modulation, which places it among bipolar devices, with the high input impedance of the voltage controlled MOSFET. It has been classified in the bipolar devices and is limited by high switching losses due to the extraction of the minority carriers from the drift layer. Because the process to obtain a low interface state density is actually better for *n*-MOSFET, *n*-channel IGBT is the preferred to the *p*-channel IGBT, but it needs of a

high−quality *p*-type substrate which is not available in large diameter and high doping concentration. In [29] n-IGBT shows $V_{BL}=13kV$ and $R_{ON}=22m\Omega cm^2$.

1.1.2.4 GTO

Gate Turn-Off thyristors permits to reduce the turn-off time by reversing the gate drive current at the expense of large current tails, limiting its use to high power DC applications. The possibility to realize a 4H-SiC GTO leads to manage very high blocking voltages at higher junction temperatures [30].

1.2 4H-SiC BMFET

Bipolar Mode Field Effect Transistor (BMFET) combines the normally-off behavior of a Vertical JFET with the conductivity modulation of a bipolar transistor. Briefly, the operating principle is based on the superposition of the Space Charge Regions, SCRs, formed by *p-n* junctions, which induce a potential barrier in the channel blocking electron flow from source to drain when the transistor is in OFF state; during the conduction mode, instead, hole carriers are injected in the channel from gates in order that the output resistance reduces for the conductivity modulation effect.

Device structure is reported in Fig. 1.5, where X_{CH} represents the channel width coincident with the gate-to-gate distance and Y_G is the depth of gate placed Y_R away from the bottom of source. Although it is similar to a VJFET structure (Fig.1.2), epilayer doping concentration, N_{EPI}, is less than the typical VJFET value of $10^{16}cm^{-3}$ [14] in order to have a high potential barrier height, $V_{S/CH}$, with shallow junctions, since doping thermal diffusion coefficients are negligible under $1800°C$ [31]. Potential barrier dependency on the geometric and physic parameters is analyzed in detail in the next chapters.

The following BMFET electrical characteristics have been obtained by numerical simulations [32] for a similar structure to that in Fig. 1.5, whose geometrical and physical parameters are reported in Tab. 1.2; the implemented physical models are in APPENDIX A. It is worth to note that, since ion-implantation is the most critical device

process, gate region parameters are related to Al ion-implanted *p-n* junctions analyzed in Chapter 4 and 5.

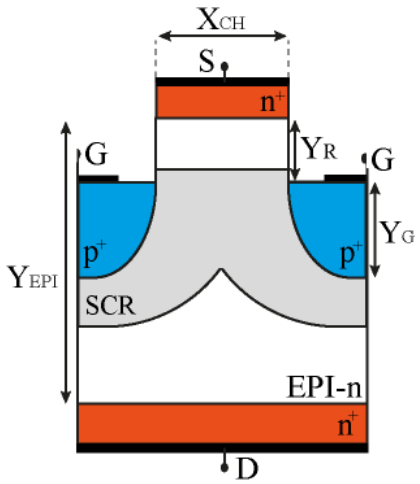

Fig.1.5. Cross section view of a BMFET structure.

REGIONS	DEVICE PARAMETERS		*4H-SiC*
EPILAYER	N_{EPI}	$[cm^{-3}]$	10^{15}
	X_{CH}	$[\mu m]$	0.9
	Y_R	$[\mu m]$	1
	$Y_{CH} = Y_R + Y_G$	$[\mu m]$	2
	Y_{EPI}	$[\mu m]$	10
GATE	N_{aG}	$[cm^{-3}]$	$6 \cdot 10^{19}$
	N^{-}_{aG}	$[cm^{-3}]$	$5.5 \cdot 10^{17}$
	$N_{eff,aG}$	$[cm^{-3}]$	$3.3 \cdot 10^{17}$
	Y_G	$[\mu m]$	1
SOURCE/DRAIN	$N_{dS/dD}$	$[cm^{-3}]$	10^{19}
	$N^{+}_{dS/dD}$	$[cm^{-3}]$	$2 \cdot 10^{18}$
	$N_{eff,dS/eff,dD}$	$[cm^{-3}]$	$6.6 \cdot 10^{17}$
	$Y_{S/D}$	$[\mu m]$	0.7/30
	R_{n+}	$[\Omega cm^2]$	10^{-4}
	R_{p+}	$[\Omega cm^2]$	10^{-5}
	$\tau_{0n,0p}$	$[ns]$	150
	Z	$[\mu m]$	1

Table1.2. Main physical and geometrical parameters of the structure in Fig.1.5.

1.2.1 Normally-off behavior

Depending on the channel geometry and doping concentration both normally-on and normally-off behaviors are allowed. Let us consider a BMFET structure of Tab.1.2 and the circuit schematic in the insert of Fig. 1.6, where source and gate terminals are to ground and a forward drain–source voltage, V_{DS}, is applied; the blocking voltage is defined as V_{DS} value for which drain current densities, J_D, reaches a maximum allowed value, which is $100\mu A/cm^2$ in our case. In Fig. 1.6, for wide channel ($X_{CH}=1.2\mu m$), the maximum J_D value is reached at $V_{bl}=364V$ when the gate current density, J_G, is still low meaning that the channel opens due to the decreasing of the potential barrier; instead, by reducing the channel width, the blocking voltage increases ($V_{bl}=860V$) with $V_{S/CH}$ in the case of $X_{CH}=1\mu m$, until to detect the gate-drain diode breakdown at $X_{CH}=0.9\mu m$ with $V_{bl}=1257V$.

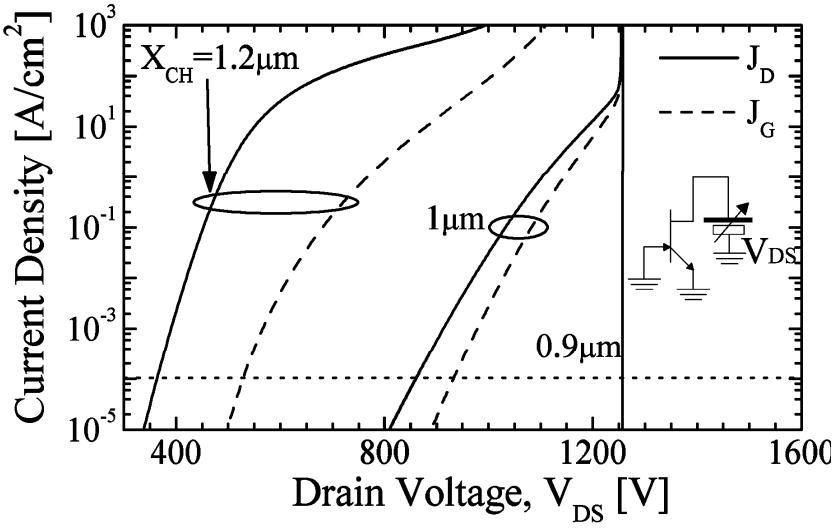

Fig.1.6. J_D and J_G as function of V_{DS} for different X_{CH} values at $V_{GS}=0V$. In the insert the circuit schematic is shown.

1.2.2 Conduction state

In Fig. 1.7 Gummel plot is reported for a BMFET structure of Tab.1.2 at $V_{DS}=20V$. J_G-V_{GS} characteristics is typical of a *p-n* junction, which is in medium and high hole injection regime for $V_{GS}\geq 2V_T ln(N_{EPI}/n_i)\approx 2.6V$; over this voltage, channel conductivity modulation is obtained as shown to the further increasing of J_D between 10^2 and $10^3 A/cm^2$. About the lower part of the output current, the exponential behavior is due to the modulation of the potential barrier height by applying V_{GS}. It is known as sub-threshold region and will be addresses in Chapter 3.

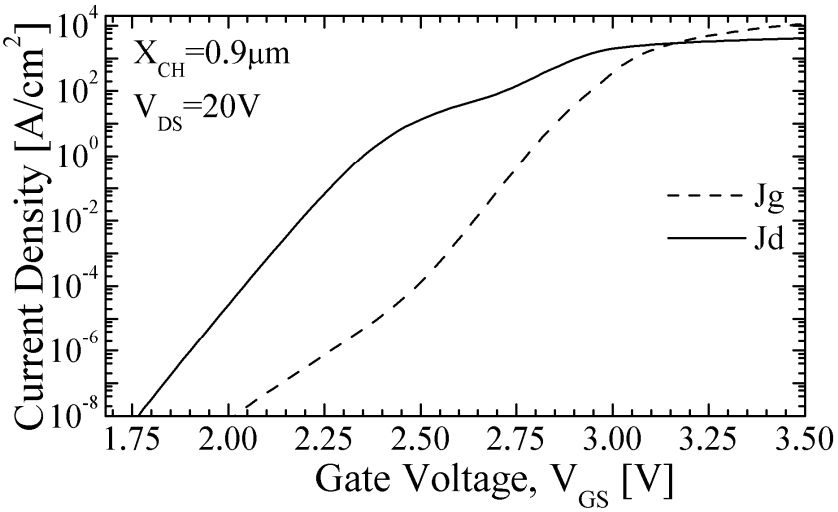

Fig.1.7. Gummel plot of BMFET with $X_{CH}=0.9\mu m$ at $V_{DS}=20V$.

Output characteristics are reported in Fig. 1.8 and, for $h_{FE,forced}=12$ and $J_D=100A/cm^2$, $V_{DS,SAT}$ is $0.35V$ in the saturation region that means an on-resistance of $3.5m\Omega cm^2$, which is much lower than the intrinsic on-resistance [16]:

$$r_{ON,Unipolar} = \frac{Y_{CH}}{q\mu_n N_{EPI}}\left(1+\frac{X_G}{X_{CH}}\right)\left[1+\frac{X_{CH}}{2Y_{CH}}\ln\left(1+\frac{X_G}{X_{CH}}\right)+ + \frac{Y_{EPI}-0.5X_{CH}}{Y_{CH}}\frac{X_{CH}}{X_{CH}+X_G}\right] \quad (1.1)$$

equal to $8.2 m\Omega cm^2$. This is due to the conductivity modulation appearing when hole carriers are injected in the channel once *p-n* junction is forward biases. Moreover, the ratio between J_D and J_G defines the common source current gain, h_{FE}, and is reported in Fig. 1.9 for the same structure and electrical condition of the previous device; h_{FE} values of *86* and *44* are at J_D equal to $355A/cm^2$ and $585A/cm^2$, respectively.

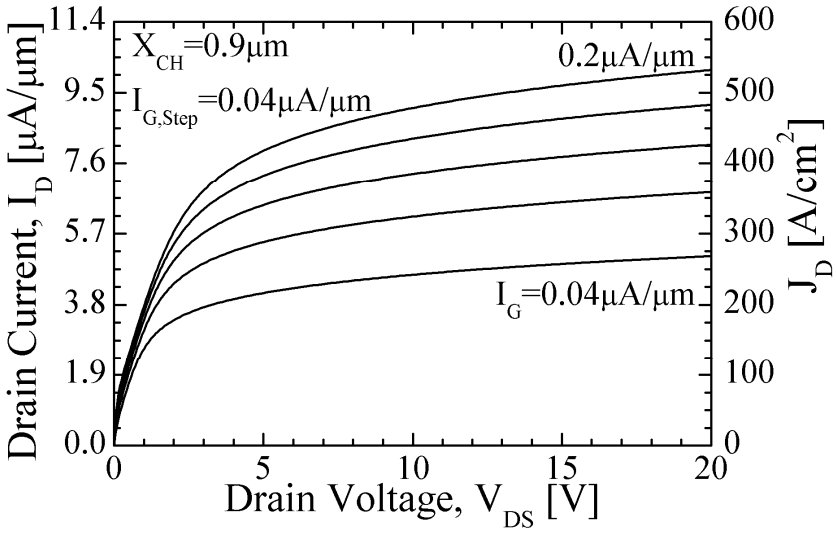

Fig.1.8. J_D-V_{DS} characteristics of BMFET with $X_{CH}=0.9\mu m$ at room temperature.

Each single cell is connected in parallel on the same die in order to achieve the desiderated output current and, therefore, a thermal stability have to be reached to avoided thermal runaway, which can destroy the device. This thermal property is shown in Fig.1.9 for a temperature range of *300÷523K* and, similarly to 4H-SiC BJTs [33], is the results of combined temperature dependences of carriers lifetime and ionized dopant density, whose impurity energy levels have been set *190meV* and *70meV* (see APPENDIX A) for acceptor and donor, respectively. Moreover, in Fig. 1.10 the thermal stability of BMFETs is confirmed also in the saturation region, where $r_{DS,ON}$ increase with temperature originates from decrease of the electron mobility in the drift region contrasting the thermal runaway.

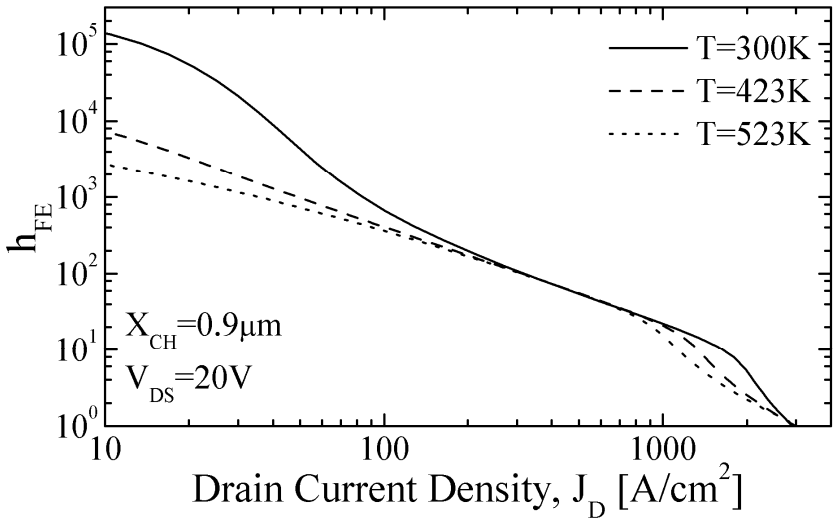

Fig.1.9. h_{FE}-J_D of BMFET with X_{CH}=*0.9μm* at V_{DS}=*20V* for different temperatures.

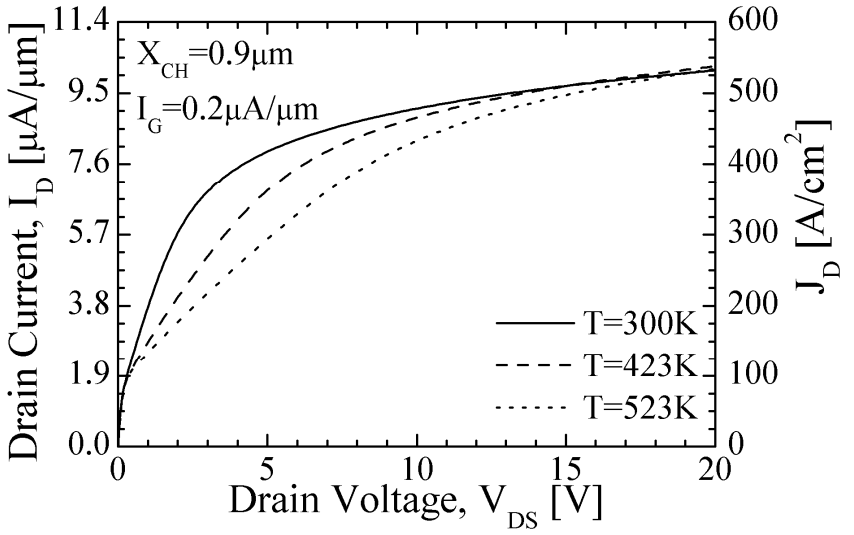

Fig.1.10. J_D-V_{DS} characteristics of BMFET with $X_{CH}=0.9\mu m$ at different temperatures.

1.2.3 Switching

In Fig. 1.11 and 1.12 input and output transients are reported for BMFET driving a clamped inductive load during the switching on and off, respectively. The inductive load has been modeled with a constant current source and an ideal diode in series with a voltage source, as in the insert of Fig. 1.11.b. When BMFET is in OFF-state, the load current, I_{LOAD}, imposed by the ideal current source, flows through the free−wheeling diode and the high external voltage, V_{DC}, drops across the device, then, when BMFET is in ON−state, the input voltage source with a series resistance applies gate current in order that BMFET is in saturation region and the low drain voltage is able to turn off the diode absorbing I_{LOAD}. This last has been chosen equal to $100A/cm^2$ and the clamping voltage is $600V$, which are typical values assumed to test a medium-high power transistor. Moreover, the bias conditions are to have a $h_{FE,forced}$ of 8.5 and a $V_{DS,SAT}$ of $0.39V$. The device structure is the same of Table 1.2 with $X_{CH}=0.7\mu m$ and $Y_{EPI}=15\ \mu m$.

During the switching on, a voltage step is applied to the gate as

reported in Fig. 1.11 and I_G instantly increases, showing a spike due to the input capacitance. After a delay time, t_D, of *0.63ns*, at first I_D sharply reaches its ON−state value, while V_{DS} softly falls to $V_{DS,SAT}$ in *4.8ns* owing to the charging of the gate−drain capacitance and to the injection of the hole carriers. Overall, the ON transient stands *5.7ns*, t_{ON}, and the ON switching energy, E_{ON}, is *0.19mJ/cm*^{2}.

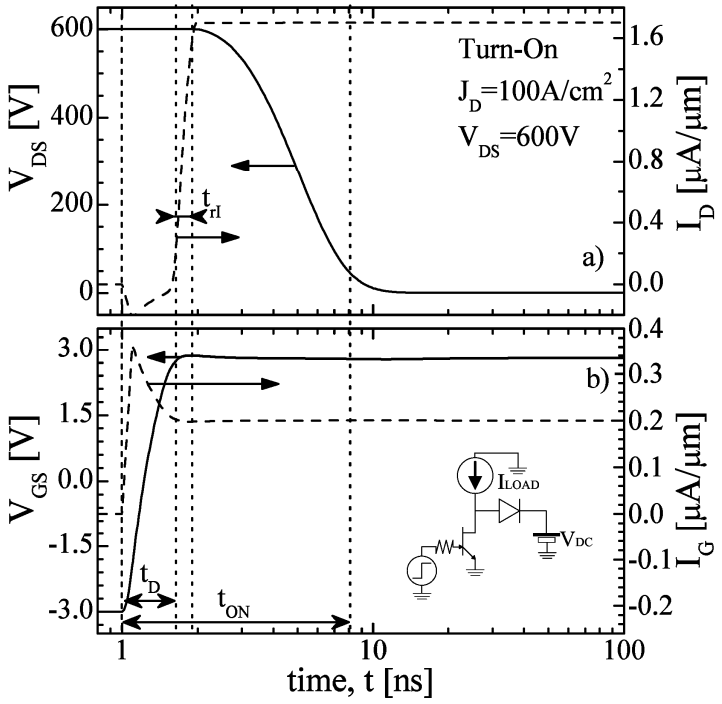

Fig.1.11. *600V/100Acm*$^{-2}$-inductive load a) output and b) input switching-on transients of a BMFET with X_{CH}=*0.7µm* and Y_{EPI}=*15µm*. *T=300K*.

Like all bipolar device, during the turning off the injected minority carriers have to be extracted and it is evident that the OFF time, t_{OFF}, which is equal to *34.8ns*, corresponds largely to the reverse recovery. Although t_{OFF} is longer than t_{ON}, V_{DS} sharply rises to the clamped voltage (t_{rV}~*6.2ns*) at the end of the storage and, once this condition is reached, I_{DS} instantly falls to the leakage value. This drain current behavior is a peculiarity of BMFET because, differently from BJT in

which the current fall is due to the extraction of the remaining electron carriers stored into the base [34], once V_{DS} reaches the clamping voltage, the formation of the barrier in the BMFET forces the removal of holes from gate and electrons from source. The disappearance of the current tail permits to have low energy loss during turning-off, $E_{OFF,}$ which in this case is $0.18mJ/cm^2$.

It is worth to note that, due to the high drain-gate current ratio, both ON and OFF input switching energy are three order of magnitude lower than those of the output, having the input and output conduction power losses P_{Cond} equal to $33W/cm^2$ and $40W/cm^2$, respectively.

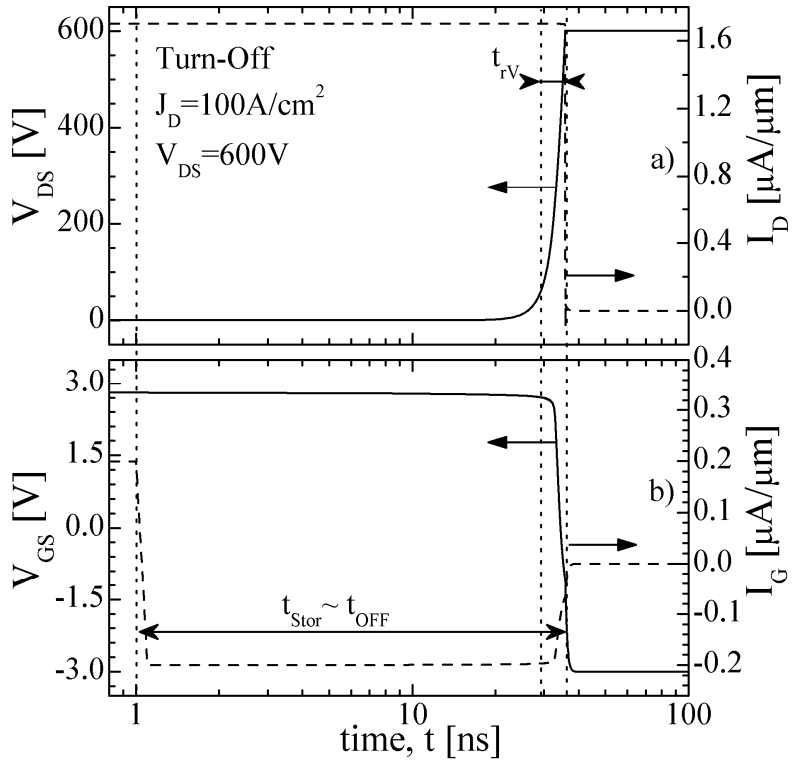

Fig.1.12. $600V/100Acm^{-2}$-inductive load a) output and b) input switching-off transients of a BMFET with $X_{CH}=0.7\mu m$ and $Y_{EPI}=15\mu m$. $T=300K$.

1.3 Conclusion

After a brief introduction on the fields of applications of 4H-SiC power device and on the state-of-art of available transistors, Bipolar Mode Field Effect Transistor structure is shown and main physical principles are described by using electrical characteristics. From this analysis three aspects are relevant:

- Potential barrier height dependency on geometrical and physical device parameters, which plays both in the OFF-state and in sub-threshold regime;
- Extraction of injected hole carriers during the storage time of switching-off;
- Hole injection efficiency of the p-type gate region, which is necessary for the channel modulation conductivity.

They are deeply addresses in the Chapters 2-3, 4 and 5, respectively. Moreover, being essential the presence of an integrated freewheeling diode in anti-parallel to BMFET, a Schottky diode is proposed in Chapter 7 by using an innovative material as anode contact, which is PentOxide DiVanadium (V_2O_5).

Chapter 2

Potential Barrier Model

The main topics of this thesis is on the development of a model which can describe the potential barrier height into the channel of a vertical structure, like BMFET, VJFET and BSIT, for any physical, geometric and electric configurations. That permits both to understand the physics behind the operation of this topology of transistors and to have an instrument to design the channel of the transistor.

2.1 Motivation

Since the introduction of Static Induction Transistor (SIT) in the early 1970s [35], which first demonstrated the feasibility of short depleted channel to realize normally-off behaviour JFETs, the effectiveness of the gate topology is become an important issue for controlling the output current of other JFET-like transistors, as BSIT [36] and BMFET [37], rectifiers [38], [39] and, more recently, Silicon Carbide JFETs [9], [40], [41] and BSITs [42]. Basically, the current controlling mechanism in these devices can be explained by observing that, as the channel width is reduced, the space charge regions of the two lateral gates overlap underneath the source by inducing in this way a voltage barrier which opposes to the electron injection from the source and increases the minority carrier density in the channel. Due to the complexity of the problem, design rules has been analyzed so far only by numerical methods to obtain the two-dimensional potential and carrier distributions within the channel [43]-[46]. Considering the proposed analytical models [36], [47]-[50], the solution derived in [36], [47]-[49] for the two-dimensional potential distribution are quite

inadequate for the assumption of a fully depleted channel, while the model proposed for the potential barrier in [50] using the Doping-Voltage Transformation [51]-[52] has been demonstrated valid only for a well defined BMFET structure. It must be observed that the absence of models describing the barrier height and free carriers concentration in the channel of BSITs for an arbitrary channel geometry and bias condition nullifies the effectiveness of numerous analytical models [48], [49], [53]-[55] published to describe the transfer characteristics of BSITs, stimulated probably from the similarity of the depletion regions overlapping and the holes accumulation, respectively, with the punch-through phenomenon of BJTs [56] and the inversion mechanism of MOSFETs. In fact, some of them [48],[49] support a description of the barrier height as function of the channel geometry and the applied voltage using a depleted channel approximation, the others [53]-[55] give analytical expressions of the output current which include, however, quantities achievable only by numerical simulations. Therefore, as follows from the above observations, the electrical behaviour of BSITs structures, represented by their input, output and transfer characteristics, still waits to be adequately modelled.

2.2 Theory of the Potential Barrier Height Model

In order to extend the validity of this model to recessed-gate JFETs topologies, the channel geometry used in our analysis has been chosen as in Fig. 2.1, where X_{CH} represents the channel width coincident with the gate-to-gate distance and Y_G is the depth of gate placed Y_R away from the bottom of source.

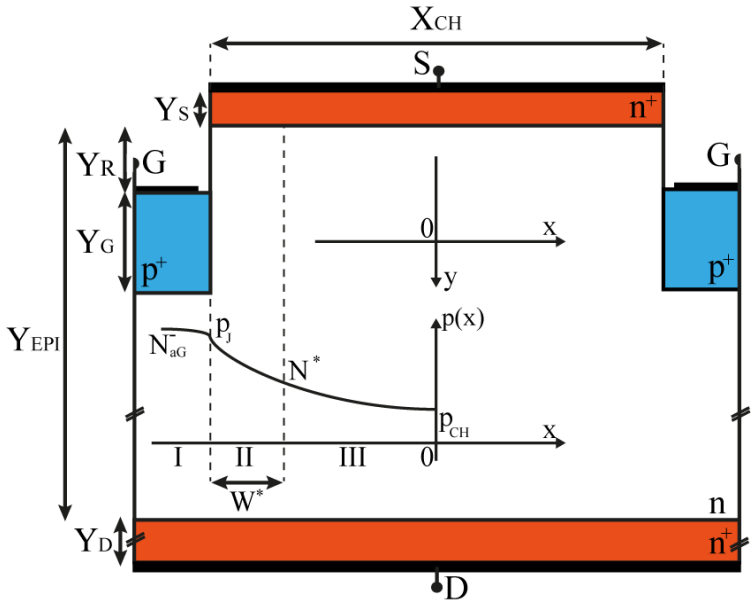

Fig.2.1 Cross section of the p^+-n-p^+ structure cell with the sketch of the hole carrier distribution at $y=0$.

Moreover, to avoid the numerical integration of the two-dimensional Poisson equation for the need of including the mobile carriers, the analytical solution has been obtained by evaluating the gate-channel voltage $V_{G/CH}$ as the sum of the voltage drops across the three subzones encountered from the p^+ region to the saddle point at the center *(0,0)*, namely:

$$V_{G/CH} = V_I + V_{II} + V_{III} \tag{2.1}$$

With the help of the carrier profile sketched in Fig. 2.1, the zone *I* represents the gate region where the hole density varies from the ionized doping value, N_{aG}^-, to the unknown holes value p_J at the metallurgical interface, the zone *II* corresponds to the channel region closer to the interface with an holes density much higher than the epilayer doping, namely $p(x) \geq N^* \gg N_{EPI}$, and, finally, the zone *III* represents the region where the hole density is comparable with

doping and disappears when the hole density at the saddle point, p_{SP}, is greater than N^*. It should be emphasized that, once $V_{G/CH}$ has been evaluated, the height of the source-channel barrier $V_{S/CH}$ can be obtained as follows:

$$V_{S/CH} = V_{bi} + V_{n^+n} - V_{G/CH} \tag{2.2}$$

being $V_{bi} = V_T \ln\left(N_{eff,aG} N_{EPI} / n_i^2\right)$ the built-voltage of the gate-channel diode, $V_{n^+n} = V_T \ln\left(N_{eff,dS} / N_{EPI}\right)$ the built-voltage of the high-low source-channel junction, V_T the thermal voltage, $N_{eff,aG(dS)}$ the effective gate (source) doping and n_i the intrinsic concentration.

In deriving the model, these zones will be treated with the following assumptions:

a) after demonstrating that V_I differs of a few millivolts from V_T, it is taken, for simplicity, equal to the thermal voltage, V_T, so that the unknown holes value at the metallurgical interface can be put equal to $p_J = N_{eff,aG} e^{-1}$;

b) the zone *II* coincides with the channel portion where the hole density, starting from p_J, remains greater or at least equal to $N^*=20N_{EPI}$, to which its maximum width W^* occurs;

c) the carrier transport in the zone *III* is governed by the drift and diffusion mechanism and the electric field varies likely a depleted region, namely:

$$E_X(x, y) = E_M \frac{2x}{\left(X_{CH} - 2W^*\right)} \tag{2.3}$$

where E_M is the maximum value at the border between the zones *II* and *III* and depends on both channel width and channel depth.

2.2.1 Zone *I*

Let considers the Poisson equation in gate region, only for the majority carriers and ions concentrations:

$$\frac{d^2\psi_i}{dx^2} = \frac{q}{\varepsilon}\left(N_{aG}^{-} - n_i e^{\frac{\phi_{pF}-\psi_i}{V_T}} \right)$$

where Φ_{pF} and Ψ_i are the hole quasi-Fermi and the electrostatic potential, respectively; integrating in $[-\infty, -X_{CH}/2]$, one obtains:

$$E^2\Big|_{-\frac{X_{CH}}{2}^-} = \frac{2qV_T N_{aG}^{-}}{\varepsilon}\left(e^{-\frac{V_I}{V_T}} - 1 + \frac{V_I}{V_T} \right) \qquad (2.4)$$

being V_I is measured respect to $V_I(-\infty)=0$. Analogously, if the Poisson equation is integrated in the region *II* assuming $E(0)=0$ for symmetry, the electric field at $x=-X_{CH}/2$ can be written as follows:

$$E^2\Big|_{-\frac{X_{CH}}{2}^+} = \frac{2qV_T p_{SP}}{\varepsilon}\left(e^{\frac{V_{II}}{V_T}} - 1 \right) \qquad (2.5)$$

Therefore, by expressing the total voltage V_I+V_{II} in terms of the apparent bandgap narrowing, ΔV_{aG}, namely:

$$V_I + V_{II} = V_T \ln\left(\frac{N_{aG}^{-}}{p_{SP}} \right) - \frac{\Delta V_{aG}}{2} \qquad (2.6)$$

and by imposing the equality of (2.4) and (2.5), one obtains:

$$\frac{V_I}{V_T} + e^{-\frac{V_I}{V_T}}\left(1 - e^{-\frac{\Delta V_{aG}}{2V_T}} \right) = 1 - \frac{p_{SP}}{N_{aG}^{-}} \qquad (2.7)$$

which can be numerically solved to obtain V_I for an arbitrary p_{SP}.

It is clearly from (2.7) that V_I is at most even to V_T, justifying the assumption *a)* in the previous section.

2.2.2 Zone *II*

For the assumption *b)* it is convenient to refer to a sufficiently small channel X_{CH} in order to vanish the zone *III* and the thickness W of the zone *II* coinciding with $X_{CH}/2$. In this case, by neglecting the doping and electrons in Poisson equation, this latter can be written along the x-direction as follows:

$$\frac{d^2\psi_i}{dx^2} = -\frac{q}{\varepsilon} n_i e^{\frac{\psi_F - \psi_i}{V_T}} \tag{2.8}$$

where Ψ_F and Ψ_i are the Fermi and the electrostatic potential in the channel, respectively. By integrating (2.8) in the interval $[-X_{CH}/2,0]$ and using as boundary condition the symmetry of the potential distribution along the channel,

$$\left.\frac{d\psi_i}{dx}\right|_{x=0} = 0$$

the electric field can be written as:

$$E(x) = -\frac{d\psi_i}{dx} = -\sqrt{\frac{2qV_T p_{SP}}{\varepsilon}\left(e^{\frac{\psi_i(0)-\psi_i(x)}{V_T}} - 1\right)}$$

which, further integrated, yields:

$$X_{CH} = \sqrt{\frac{8\varepsilon V_T}{q p_{SP}}} \tan^{-1}\left(\sqrt{\frac{p_J}{p_{SP}} - 1}\right) \tag{2.9}$$

This last can be iteratively solved to obtain for a given X_{CH} the carrier density p_{SP} and the voltage drop across the zone *II*:

$$V_{II} = V_T \ln\left(\frac{p_J}{p_{SP}}\right) \tag{2.10}$$

as long as $p_{SP} \geq N^*$. It is evident that, when X_{CH} is wide enough to make $p_{SP} < N^*$, i.e. $X_{CH} > 2W^*$, (2.9) gives the maximum extension of the zone *II*, namely:

$$W^* = \sqrt{\frac{2\varepsilon V_T}{qN^*}} \tan^{-1}\left(\sqrt{\frac{p_J}{N^*} - 1}\right) \tag{2.11}$$

and the voltage component V_{II} is even to:

$$V_{II} = V_T \ln\left(\frac{p_J}{N^*}\right) \tag{2.12}$$

2.2.3 Zone *III*

By considering the x-component hole current density negligible and by using the electric field (2.3), one obtains:

$$\frac{dp}{p} = \frac{|E_M| 2x}{V_T\left(X_{CH} - 2W^*\right)} dx$$

which, integrated in the interval $[-(X_{CH}/2 - W^*), 0]$ with N^* as boundary condition, yields the hole carrier concentration at the saddle point:

$$p_{SP} = N^* e^{-\frac{|E_M|}{4V_T}\left(X_{CH} - 2W^*\right)} \tag{2.13}$$

and the voltage drop can be evaluated as:

$$V_{III} = \frac{|E_M|}{4}\left(X_{CH} - 2W^*\right) \tag{2.14}$$

By recalling that (2.3) has been derived assuming one-dimensional the electric field along the symmetry axis of gates, that is certainly true for gates infinitely deep (Y_G=∞) and distant from the source (Y_R=∞), it obvious that the maximum electric field E_M must be adequately written to incorporate the effects of finite Y_G and Y_R, whose reduction leads the electric field internally to the channel to be more influenced from that of gate corners and n^+-n junction, respectively. Therefore, the maximum electric field is determined from the sum of a one-dimensional electric field and of the cylindrical contribution from the gate corners:

$$E_M = E^{1-D} + E^{CYL} \tag{2.15}$$

In Fig.2.2 the E_X distribution, evaluated from the model along the x-axis and $y=0$, is compared with the numerical simulation results for X_{CH}−$1\mu m$, Y_R−$1\mu m$ and different Y_G structures in thermal equilibrium conditions. It is clear that the distribution is linear according to (2.3) and, as expected, by reducing the junction depth the maximum at the border between the zone *III* and *II* increases due to a major interaction among the electric fields at the gate corners.

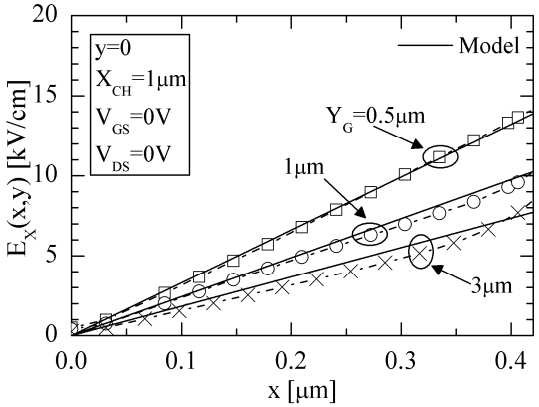

Fig.2.2 Comparisons between model and simulation of E_X along the x-axis at $y=0$ in thermal equilibrium condition for X_{CH}-$1\mu m$, Y_R-$1\mu m$ and different Y_G structures.

2.2.3.1 1-D term of E_M

To properly account for the X_{CH} effect on the JFETs conduction, as it will be shown in Chapter 3, it is necessary consider both fixed and mobile charges in Poisson equation along the x-axis; in fact, as X_{CH} increases, the electron density at the channel centre increases towards its neutral value, becoming inadequate the assumption of fully depletion. By integrating the Poisson equation with the condition $E(x)|_{x=0}=0$, one obtains:

$$E^{1-D}=\sqrt{\frac{2qV_TN_{EPI}}{\varepsilon}\left[\frac{V_{III}}{V_t}+\frac{n_{SP}}{N_{EPI}}\left(e^{-\frac{V_{III}}{V_T}}-1\right)+\frac{p_{SP}}{N_{EPI}}\left(e^{\frac{V_{III}}{V_T}}-1\right)\right]}$$

For the pursuit of simplicity, the contribution of hole carriers can be neglected since it become relevant for $X_{CH}\approx 2W^*$, hence, it is accounted for by V_{II}, indeed, the contribution of the electron carriers is relevant for $V_{III}>>V_T$, so that, the first term in (2.3) can be rewritten as:

$$E^{1-D}=\sqrt{\frac{2qN_{EPI}V_{III}}{\varepsilon}} \tag{2.16}$$

2.2.3.2 Cylindrical term of E_M

- ***V_{DS}=0V***

Since E_M in (2.14) represents the maximum field at the extremity of zone *III,* namely at $(-X_{CH}/2+W^*)$, as shown in Fig.2.3, a convenient way to account for the field effects of the corners lies in assimilating the gate geometry to a cylindrical shape with radius $r_J=\sqrt{L_d^2+Y_G^2}$, where the Debye length $L_d=\sqrt{2\varepsilon V_T q^{-1}N_{EPI}^{-1}}$ has been introduced to take into account the zone *II* when Y_G becomes infinitesimal. Therefore, assuming that the cylindrical shape extends at the same way of the parallel-plane behavior of the horizontal gate sides, it can be written as follows:

$$E^{CYL}(r_j) = \frac{qN}{2\varepsilon}\frac{\left(W_{SC}^{V_G}\right)^2 - r_j^2}{2r_j} \tag{2.15}$$

where $W_{SCR}^{V_G} = \sqrt{2\varepsilon q^{-1} N_{EPI}^{-1}\left(V_{bi} - V_{GS}\right)}$ is the p^+-n Space Charge Region dependent on Gate-Source voltage, the further factor of two added to denominator arises from the symmetry of electric field due to the double gates [57] and N represents an equivalent channel doping dependent on Y_R. In fact, by noting that the abrupt change of the n-n^+ junction doping modifies the electric field at the gate corners according to an equivalent charge variation $\Delta N = N_{EPI}\exp\left(-Y_R/L_d\right)$ [58], by using in the former equation $N=N_{EPI}+\Delta N$ the maximum electric field, E_M, can be expressed as:

$$E^{CYL} = \frac{qN_{EPI}}{4\varepsilon}\frac{\left(W_{SC}{}^{V_G}\right)^2}{\sqrt{L_d^2 + Y_G^2}}\left(1 + e^{-\frac{Y_R}{L_d}}\right) \tag{2.16}$$

where the term r_J has been neglected with respect to $W_{SCR}^{V_G}$ [34].

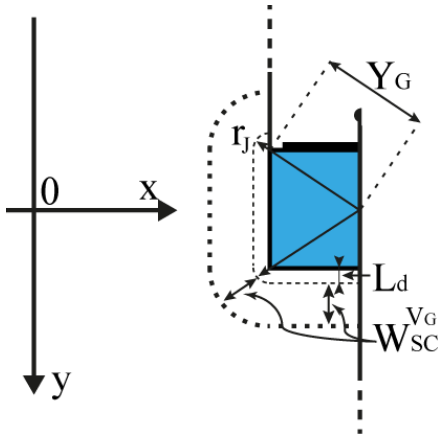

Fig.2.3 Shape of a space charge region of gate, showing the cylindrical and planar component of the electric field.

- ***V_{DS}≠0V***

In presence of V_{DS}, the bottom side of the horizontal gate region is reversely biased by $(V_{DS}-V_{GS})$, obtaining a depletion width $W_{SC}^{V_D}=\sqrt{2\varepsilon\left(V_{bi}-V_{GS}+V_{DS}\right)q^{-1}N_{EPI}^{-1}}$, while the upper gate side remains biased by V_{GS} only because of the shielding effect exhibited from the holes pile-up in the channel. This means that the electric field inside the channel cannot be assumed symmetric with respect to $y=0$, as it has been done previously, since the higher electric field of the bottom gate side pushes the hole density of channel towards the surface moving the position of the saddle point, Δy, where the electric field is practically zero.

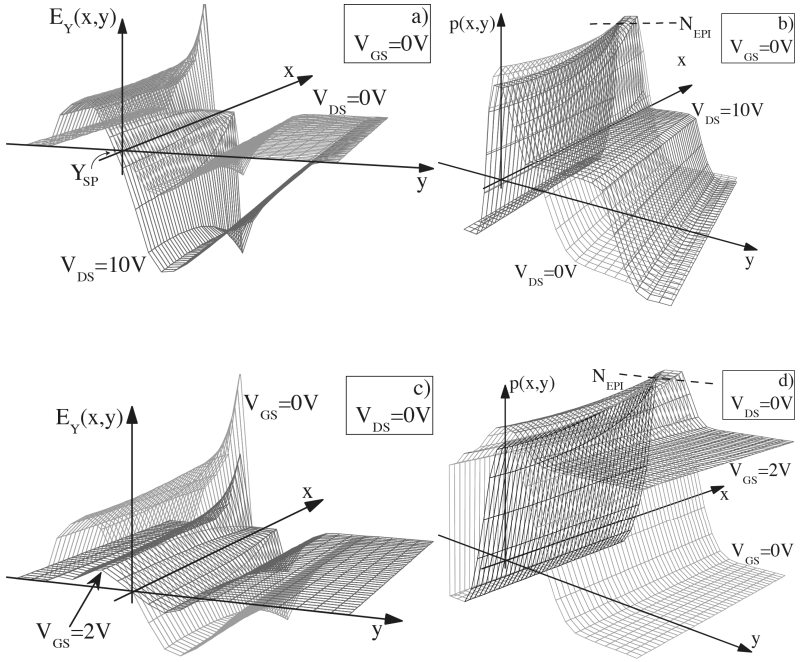

Fig.2.4. Simulated *3D* charts showing, for the half-cell of Fig.2.1, the variation of the electric field *y*-component and hole density, with respect to their equilibrium values, when a,b) $V_{DS}=10V$ and $V_{GS}=0V$ and c,d) $V_{GS}=2V$ and $V_{DS}=0V$.

In Fig. 2.4 3D-charts shows the variation induced from V_{DS} and V_{GS} separately on the distributions of the electric field *y*-component, $E_Y(x,y)$, and carrier density, $p(x,y)$, with respect to the equilibrium conditions. By applying V_{DS} (see Fig. 2.4a and 2.4b), the electric field is unvaried in the upper portion and tends to extend towards the substrate due to the shielding effect of holes; in this way, the saddle point, Y_{SP}, located at the ordinate where $E_Y = 0$, slightly shifts towards the surface, p_{SP} decreases and the symmetry of E_Y fails. Conversely, according to the curves in Fig. 2.4c and 2.4d, both E_Y and $p(x,y)$ vary significantly with V_{GS}, however not changing Y_{SP}. Therefore, if the epilayer is enough tick to allow the vertical extension of the electric field along the channel without reaching the n^+ region of source and substrate, the complexity of the two-dimensional behaviour of the channel can be overcome assuming that the electric field matches at the two channel extremities the same values imposed by the bias conditions at each gate side. As shown in Fig 2.5, which highlights the modification of the electric field when V_{DS} is applied, what said means that, in order to account for the x-axis variation of the electric field internally to the channel, the two channel extremities must be taken $\pm X_{CH}/2$ far from the gate extremities, located at $y=\pm Y_G/2$. Therefore, describing the maximum electric fields at upper and bottom gate sides, respectively, as follows:

$$\left|E_{MAX}^{V_G}\right| = \left| q\frac{N_{EPI}}{\varepsilon}\left(W_{SC}^{V_G} - \frac{X_{CH}}{2}\right)\right| \tag{2.17.a}$$

$$\left|E_{MAX}^{V_D}\right| = \left| -q\frac{N_{EPI}}{\varepsilon}\left(W_{SC}^{V_D} - \frac{X_{CH}}{2}\right)\right| \tag{2.17.b}$$

and using the linear electric field along the y-axis given by:

$$E(y)=\left|E_{MAX}^{V_G}\right|-\left|\Delta E\right|\left(y+\frac{Y_G+X_{CH}}{2}\right)= \\ =\left|E_{MAX}^{V_G}\right|-\frac{\left|E_{MAX}^{V_G}\right|+\left|E_{MAX}^{V_D}\right|}{Y_G+X_{CH}}\left(y+\frac{Y_G+X_{CH}}{2}\right) \tag{2.18}$$

the displacement of the ordinate of the saddle point is determinates as follows:

$$Y_{SP}=-\frac{\left(Y_G+X_{CH}\right)}{2}\frac{W_{SC}^{V_{DS}}-W_{SC}^{V_{GS}}}{W_{SC}^{V_{DS}}+W_{SC}^{V_{GS}}-X_{CH}} \tag{2.19}$$

Using in (2.16) the half value of (2.19) for the presence of double gate [57], the former can be rewritten a:

$$E^{CYL}\frac{1}{2}\frac{qN_{EPI}\left(1+e^{-Y_R/L_d}\right)}{2\varepsilon}\frac{\left(W_{SC}^{V_G}\right)^2}{\sqrt{L_d^2+\left(Y_G+Y_{SP}/2\right)^2}} \tag{2.20}$$

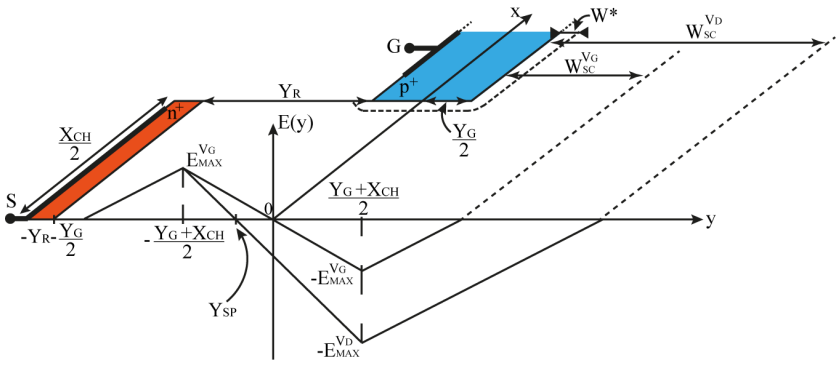

Fig.2.5 Cutaway view of the y-component of electric field at *x=0*.

2.2.4 Gate-Channel potential barrier

In order to complete the set of equations that permits to evaluate $V_{G/CH}$, it is important to note that (2.14) holds until the space charge

regions overlaps or, equivalently, until $V_{G/CH}<V_{bi}-V_{GS}$, while, for gate regions sufficiently spaced, $V_{G/CH}$ and p_{SP} coincide with V_{bi} and n_i^2/N_{EPI}, respectively. By using (2.12) and (2.14) in (2.1) set to $V_{bi}-V_{GS}$ and by neglecting L_d in (2.20), one obtains:

$$X_{CH}^{\lim}=\left(a_1-\sqrt{a_1^2-a_2}\right) \tag{2.21}$$

which is the maximum channel width for which the channel is not in neutrality condition. The terms in (2.21) are:

$$a_1=\frac{1}{2}\frac{4(b_1c_1+c_3\overline{V_{III}})+b_2c_2\overline{V_{III}}^{1/2}}{4b_1+b_2c_3\overline{V_{III}}^{1/2}} \tag{2.22.a}$$

$$a_2=\frac{4c_2\overline{V_{III}}}{4b_1+b_2c_3\overline{V_{III}}^{1/2}} \tag{2.22.b}$$

$$b_1=\frac{V_{bi}-V_{GS}}{2}\left(1+e^{-\frac{Y_R}{L_d}}\right) \tag{2.22.c}$$

$$b_2=\sqrt{\frac{2qN_{EPI}}{\varepsilon}} \tag{2.22.d}$$

$$c_1=W_{SC}^{V_{DS}}+W_{SC}^{V_{GS}} \tag{2.22.e}$$

$$c_2=Y_G\left(3W_{SC}^{V_{DS}}+5W_{SC}^{V_{GS}}\right) \tag{2.22.f}$$

$$c_3=W_{SC}^{V_{DS}}-W_{SC}^{V_{GS}}+4Y_G \tag{2.22.g}$$

and

$$\overline{V_{III}}=V_{bi}-V_{GS}-V_I-V_{II}$$

In conclusion, using the previous quantities, $V_{G/CH}$ for a generic channel geometry and bias conditions can be calculated as follows:

$$\begin{cases} V_{G/CH} = V_T \ln\left(\dfrac{N_{aG,eff}}{p_{SP}}\right) \\ \qquad\qquad if \quad X_{CH} \le 2W^* & (2.23.a) \\ V_{G/CH} = V_T \ln\left(\dfrac{N_{aG,eff}}{N^*}\right) + \dfrac{E_M}{4}\left(X_{CH} - 2W^*\right) \\ \qquad\qquad if \quad 2W^* \le X_{CH} \le X_{CH}^{\lim} & (2.23.b) \\ V_{G/CH} = V_T \ln\left(\dfrac{N_{aG,eff}}{N^*}\right) + \dfrac{E_M^{\lim}}{4}\left(X_{CH}^{\lim} - 2W^*\right) \\ \qquad\qquad if \quad X_{CH} \ge X_{CH}^{\lim} & (2.23.c) \end{cases}$$

where W^* is given from (2.11), while $V_{S/CH}$ is from (2.2) and the carrier densities at the saddle point result:

$$p_{SP} = N_{aG,eff}\, e^{-\frac{V_{G/CH}}{V_T}} \tag{2.24}$$

2.3 Model Validation

In order to validate the model, direct comparisons with numerical simulation results evaluated by using ATLAS Silvaco [32] are reported in this section. The physical models for 4H-SiC simulation are reported in APPENDIX A, indeed, for Si the fully activation and band-gap narrowing described by Slootbom [59] have been considered. The geometry of the structure both for 4H-SiC and for Si are in Table 2.1 and the use of different parameters values will be explicitly cited in the text.

REGIONS	DEVICE PARAMETERS		*4H-SiC*	*Si*
EPILAYER	N_{EPI}	$[cm^{-3}]$	10^{15}	
	Y_R	$[\mu m]$	1	
	Y_{EPI}	$[\mu m]$	9.3	
GATE	N_{aG}	$[cm^{-3}]$	$6 \cdot 10^{19}$	
	N^{-}_{aG}	$[cm^{-3}]$	$5.5 \cdot 10^{17}$	$6 \cdot 10^{19}$
	$N_{eff,aG}$	$[cm^{-3}]$	$3.3 \cdot 10^{17}$	$6.3 \cdot 10^{18}$
	Y_G	$[\mu m]$	1	
	X_G	$[\mu m]$	0.5	
SOURCE/DRAIN	$N_{dS/dD}$	$[cm^{-3}]$	$5 \cdot 10^{19}$	
	$N^{+}_{dS/dD}$	$[cm^{-3}]$	$4.9 \cdot 10^{18}$	$5 \cdot 10^{19}$
	$N_{eff,dS/dD}$	$[cm^{-3}]$	10^{18}	$5.6 \cdot 10^{18}$
	$Y_{S/D}$	$[\mu m]$	0.7/30	
	$\tau_{0n,0p}$	$[\mu s]$	0.15	1
	Z	$[\mu m]$	1	1

Table 2.1. Main physical and geometrical parameters of the structures.

Using the data of Table 2.1, the values of $V_{G/CH}$ and $V_{S/CH}$ components calculated for various channel widths, X_{CH}, of the reference structure are compared with the numerical simulations in Fig.2.6a and 2.6b assuming the thermal equilibrium conditions and $V_{GS}=2V$, respectively. Note that, as further proof of the validity of the voltage partition operated by this model (see (2.2)), in both figures the sum of the $V_{G/CH}$ and $V_{S/CH}$ components is also compared with simulations.

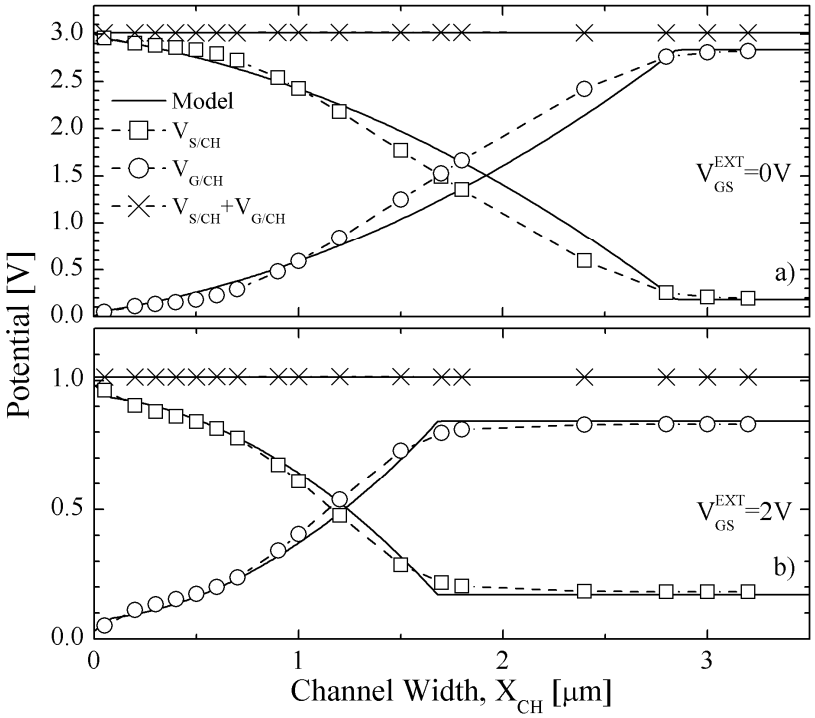

Fig.2.6 Comparisons between numerical simulations and model of $V_{S/CH}$, $V_{G/CH}$ and $V_{S/CH}+V_{G/CH}$ as function of X_{CH} for the 4H-SiC structure in Table 2.1 at a) $V_{GS}=0V$ and b) $V_{GS}=2V$.

The accuracy of this model, in determining both the voltage barrier $V_{S/CH}$ and the hole density p_{SP} under equilibrium conditions and for different channel width, X_{CH}, and various Y_G and Y_R combinations, is shown by the comparisons with numerical simulations in Fig.2.7. By observing the curves, $V_{S/CH}$ remains higher than $2V$ for X_{CH} lower than $1\mu m$ even for a surface topology $(Y_R=0)$, while it tends to increase with Y_G for a fixed channel width; indeed, once X_{CH} has become greater than $2W^*=86nm$, $V_{S/CH}$ fast decreases and tends asymptotically to V_{n+n}. In this case, as shown from Fig.2.6a, $V_{G/CH}$ tends to coincide with V_{bi}.

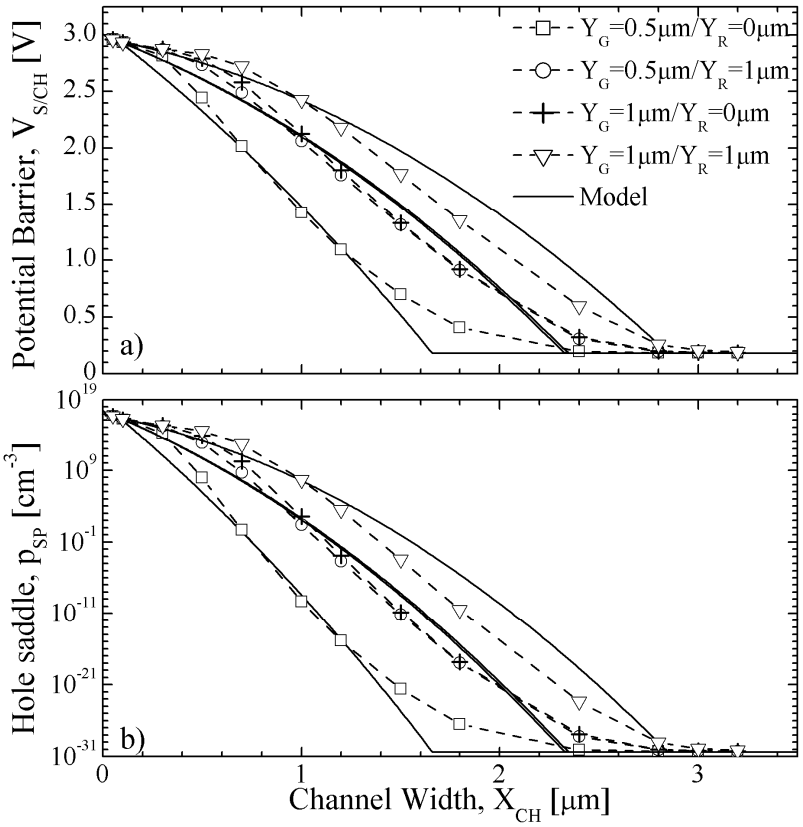

Fig.2.7 Comparisons between model and numerical simulations a) $V_{S/CH}$ and b) p_{SP} as function of X_{CH} for the 4H-SiC structure in Table 2.1 for different values of Y_G and Y_R under equilibrium conditions.

The combined effect of the channel doping, N_{EPI}, and gate depth, Y_G, on $V_{S/CH}$, is analyzed in Fig.2.8 for a structure designed with $Y_R=0.5\mu m$. Note that the greater slope of curves with higher N_{EPI} and reduced Y_G confirms the impossibility to obtain reproducible BSIT devices when high channel doping are used.

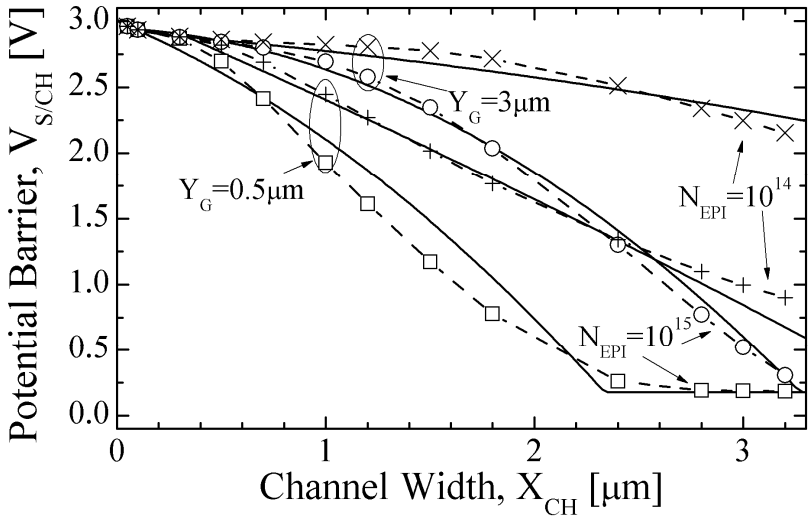

Fig.2.8 Comparisons between model and numerical simulations $V_{S/CH}$ as function of X_{CH} for the *4H-SiC JFET* in Table 2.1 with $Y_R=0.5\mu m$ for different values of Y_G and N_{EPI} under equilibrium conditions.

The above behavior is better explained in Fig.2.9, where both $V_{S/CH}$ and p_{SP} are plotted as function of N_{EPI} for three different Y_G values and a fixed $X_{CH}=1\mu m$ and $Y_R=0\mu m$. Besides the accuracy of the model, it is interesting to observe that the barrier height becomes practically N_{EPI}–independent provided that the gate is deeper than $3\mu m$, as it is required in the BMFET structures (see Chapter 1) where the low channel doping is needed to push the device operation in the conductivity modulation regime.

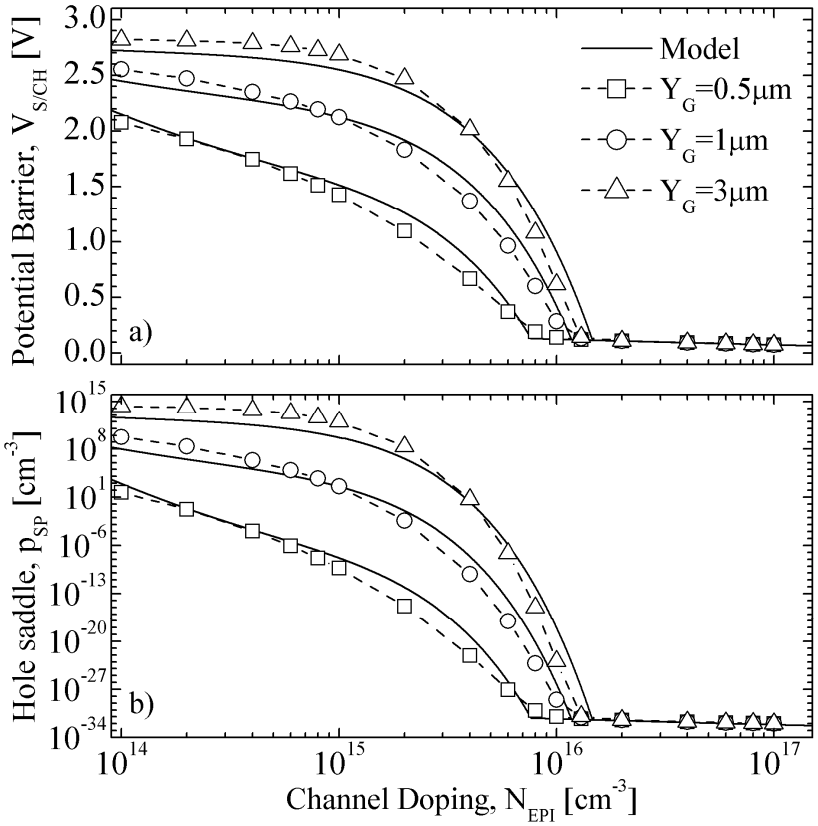

Fig.2.9 Comparisons between model and numerical simulations a) $V_{S/CH}$ and b) p_{SP} as function of N_{EPI} for the 4H-SiC structure in Table 2.1 for $X_{CH}=1\mu m$, $Y_R=0\mu m$ and different values of Y_G under equilibrium conditions.

The barrier voltage $V_{S/CH}$ (2.2) and the holes density p_{SP} (2.13) calculated at $V_{GS}=0V$ using different V_{DS} is shown in Fig.2.10 as function of X_{CH}. It is interesting noting that, for channel thinner than $1\mu m$, the barrier varies only of few hundreds of millivolts for drain voltages as high as $40V$, that justifies of several orders of magnitude of variation for the hole density p_{SP} in Fig.2.10b. It is worth noting that, for the channel doping $N_{EPI}=10^{15}cm^{-3}$ used in this case (see Table 2.1), the barrier $V_{S/CH}$ at $V_{DS}=0V$ tends to vanish as X_{CH} approaches $2.8\mu m$ and this values reduces to $2\mu m$ and $\sim 1.85\mu m$ by increasing V_{DS}, as expected.

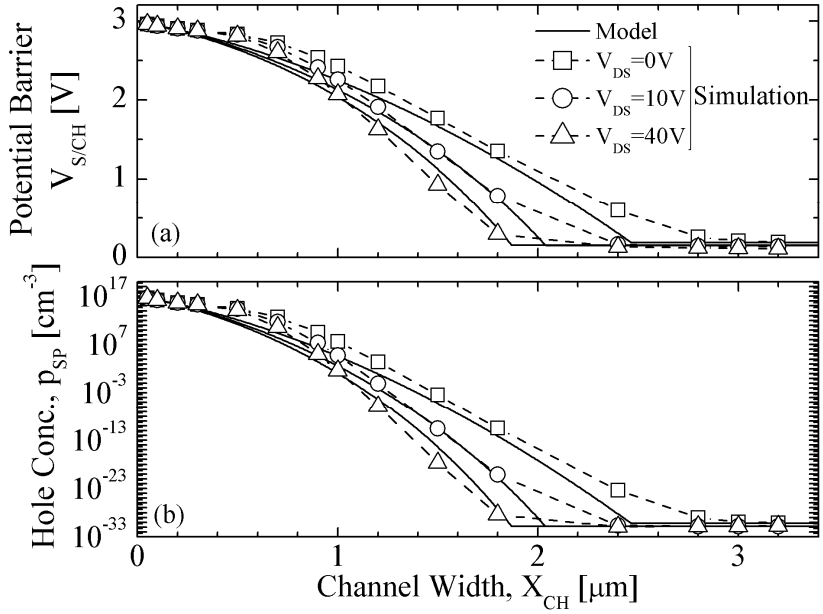

Fig. 2.10. Model and numerical simulations comparisons of (a) $V_{S/CH}$ and (b) p_{SP} as function of X_{CH} for the 4H-SiC structure in Table 2.1, using different V_{DS} with $V_{GS}=0V$.

Fig.2.11 describes the effect of Y_G on the barrier for two different Y_R values at the constant voltage $V_{DS}=10V$. Besides the expected increase of $V_{S/CH}$ with Y_G for a fixed Y_R, it is evident that the reduction of $V_{S/CH}$ with Y_R, which is practically negligible for $3\mu m$-deep gates, is remarkable at lowest Y_G to require X_{CH} much thinner than $1\mu m$ in the case of planar channels ($Y_R=0\mu m$) with $0.5\mu m$ deep gates.

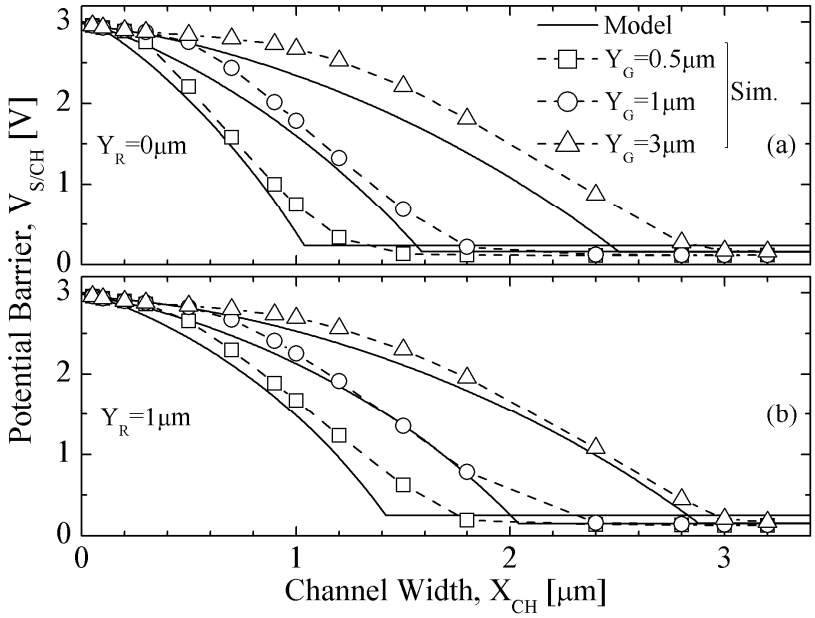

Fig. 2.11. Model and numerical simulations comparisons of $V_{S/CH}$, at $V_{DS}=10V$, as function of X_{CH} for different Y_G of the 4H-SiC device in Table 2.1, by using (a) $Y_R=0\mu m$ and (b) $Y_R=1\mu m$.

The validity of the barrier model for doping range interesting the BSIT application is confirmed from the results of Fig.2.12, showing the variation of $V_{S/CH}$ with N_{EPI} and V_{DS} for a given channel geometry ($X_{CH}=Y_G=1\mu m$). It is evident that a device with a channel width $X_{CH}=1\mu m$ becomes practically open for $N_{EPI}\cong 10^{16}cm^{-3}$, which delimits the normally-on device behaviour. In this case, a normally-off behaviour can be achieved either by increasing Y_G as shown also in Fig.2.11 or by reversely biasing the gate, as shown from the further curve reported in Fig.2.12 using $V_{GS}=-2V$, which demonstrates the usefulness of this model even for the analysis of SIT structures [35], [60].

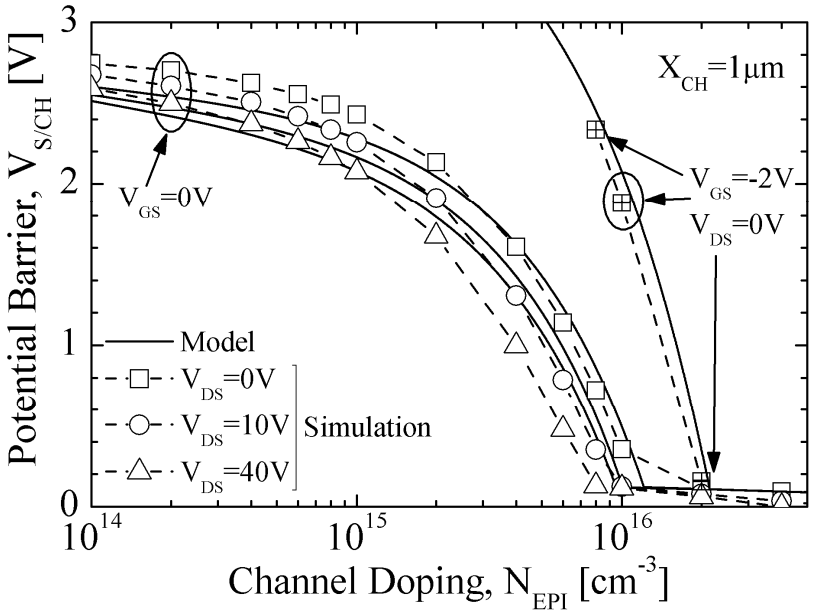

Fig. 2.12. Model and numerical simulations comparisons of $V_{S/CH}$ as function of N_{EPI} for the 4H-SiC structure in Table 2.1, using $X_{CH}=1\mu m$ and different V_{DS}.

In order to justify the model also for other semiconductors, its validity is extended for silicon BSIT devices as shown from the curves of Fig.2.13, in which V_{DS} and Y_G are changed. Comparing these curves with those of 4H-SiC in Fig.2.10, it is evident the capability of this latter semiconductor to realize higher barriers with the same geometry, that can be translated in an higher blocking voltage for the normally-off 4H-SiC devices.

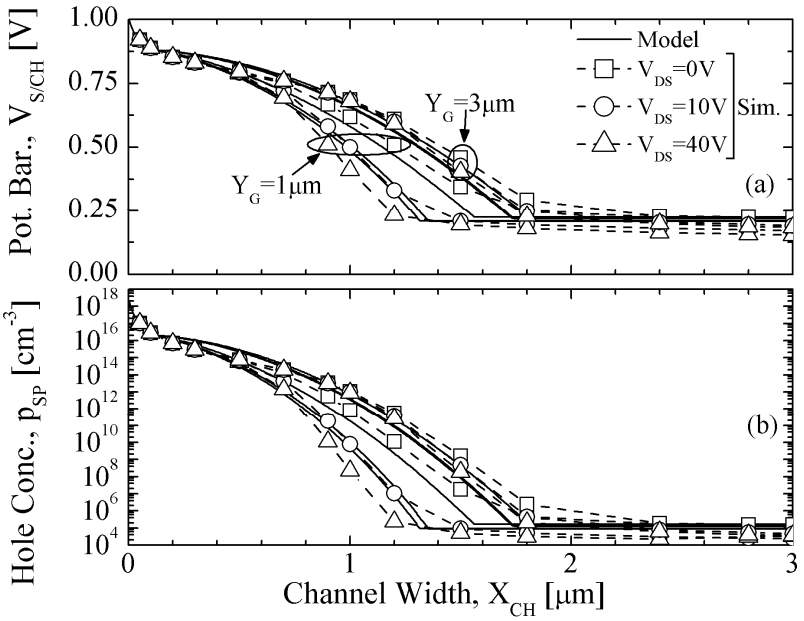

Fig. 2.13. Model and numerical simulations comparisons of (a) $V_{S/CH}$ and (b) p_{SP} as function of X_{CH} using different V_{DS} and Y_G for the Si structure in Table 2.1.

Finally, in order to confirm the validity of the model, it has been used to justify the numerical results published by other authors in the past years. One of the most representative for BSIT devices have been reported by [60]. Using the same data representation, $V_{S/CH}$ values normalized to V_{bi} for various N_{EPI} and X_{CH} are compared in Fig. 2.14a and Fig. 2.14b with the curves taken from Fig. 6b and Fig. 7 of [60], respectively. Since the data in it have been obtained by neglecting the minority carriers in the Poisson equation for an infinitely deep gate, the voltage V_{II} has been consequently neglected in (2.1) and Y_G has been assumed infinite in (2.20). The relevant accuracy shown from the curves is a clear proof of the capability of this model to predict the barrier voltage for various combinations of the channel parameters.

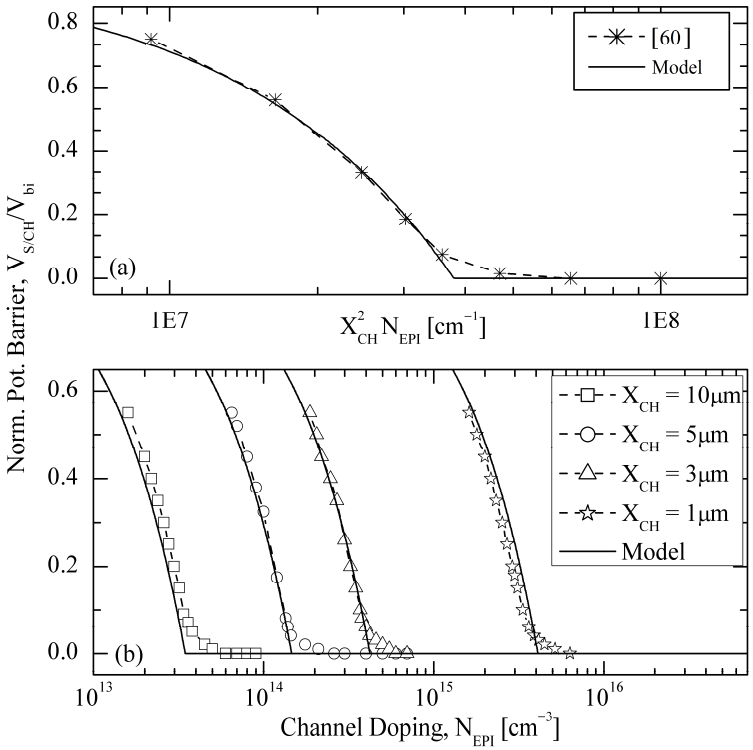

Fig. 2.14. Comparison between model and data [60] of the normalized potential barrier, $V_{S/CH}/V_{bi}$, as a function (a) of $N_{EPI}X_{CH}^2$ product and (b) of the channel doping, N_{EPI}.

Chapter 3

Sub-threshold Drain Current Model

Drain current model under sub-threshold and unipolar conditions has been developed from the previous model of the potential barrier height and is shown in this chapter.

3.1 Motivation

A model of the transfer characteristics of bipolar JFET-like structures [38], [40]-[42], [46] has been pursued since the first proposed exemplary of this class of devices, BSIT [36], has been proposed. It is well known that their normally-off behaviour is achieved surrounding the n^+ source by deepest p^+ gate regions in order to overlap the depletion regions, which introduce a potential barrier underneath the source opposing to the electron injection from the source to the drain. However, for the difficulty to evaluate the potential barrier in the two-dimensional channel without neglecting the voltage-dependent free carriers in Poisson equation, the transfer characteristics have been described so far only numerically, thus, leaving to the few existing models [47], [53]-[54] the mere role of qualitative analysis. As shown from numerical analysis of [45], the behaviour of these devices in the sub-threshold region is particularly complex, since the drain current, I_D, depends exponentially on the gate-source voltage, V_{GS}, and the slope of the curves depends on the channel geometry and on the amount of drain voltage, V_{DS}. Therefore, it is evident that an accurate modelling of the potential barrier and of its relations with the I_D-V_{GS} curves can contribute to better understand the physical operation of this class of devices.

3.2 Drain Current Model: Theory

Let considers that the hole current is negligible along the y-axis in order to write the y-component electric field as follows:

$$E_Y(x,y) = V_T \frac{1}{p(x,y)} \frac{\partial p(x,y)}{\partial y} \tag{3.1}$$

and, by using (3.1) in the electron current density, one obtains:

$$J_{nY}(x,y) = q\mu_n n(x,y) E_Y(x,y) + qD_n \frac{\partial n(x,y)}{\partial y} = \\ = \frac{qD_n}{p(x,y)} \frac{\partial\left(p(x,y)n(x,y)\right)}{\partial y} \tag{3.2}$$

where D_n is the electron diffusion coefficient. Integrating (3.2) in the interval $[-X_{CH}/2, X_{CH}/2]$ by taking the pn product constant along the x−axis, the current becomes:

$$I(y) = qD_n Z \frac{\partial(pn)}{\partial y} 2\int_0^{X_{CH}/2} \frac{1}{p(x,y)} dx \tag{3.3}$$

which integrated again along the y-axis from the n^+-n interface, located at $-(Y_R+Y_G/2)$, to the saddle point (SP) at Y_{SP}, for the constancy of the electron current, results:

$$I\int_{-(Y_R+Y_G/2)}^{Y_{SP}} \frac{dy}{2\int_0^{X_{CH}/2} \frac{1}{p(x,y)} dx} = qD_n Z\left(n_i^2 e^{\frac{V_{GS}}{Vt}} - p_{SP}n_{SP}\right) \tag{3.4}$$

where Z is the length of the device.

The distribution of holes around the saddle point $(0, Y_{SP})$ can be described by expanding in series the potential $V(x,y)$ truncated to the squared terms: $V(x,y) \simeq V(0,Y_{SP}) + \Delta V(x,Y_{SP}) + \Delta V(0,y)$, where the

latter two terms can be described by integrating, respectively, along *[0,x]* the linear electric field $E_X(x,y) \simeq \left(2E_M / X_{CH}^*\right)x$, which is obtained from (2.3), being $X_{CH}^* = X_{CH} - 2W^*$, and along *[y,Y_{SP}]* the expression (2.18). This latter quantity results:

$$\Delta V(0,y) = V(0,y) - V(0,Y_{SP}) = -\left[-\int_y^{Y_{SP}} E(y)dy\right] =$$
$$= \left|E_{MAX}^{V_G}\right|\left(Y_{SP} - y\right) + \frac{\Delta E}{2}\left[\left(y + \frac{Y_G + X_{CH}}{2}\right)^2 - \left(Y_{SP} + \frac{Y_G + X_{CH}}{2}\right)^2\right]$$

where $\Delta E = qN_D\varepsilon^{-1}\left(W_{SC}^{V_D} + W_{SC}^{V_G} - X_{CH}\right)/\left(Y_G + X_{CH}\right)$. In this way, the hole density

$$p(x,y) = n_i e^{\frac{\phi_P - V(x,y)}{V_T}}$$

can be expressed as:

$$p\left(x,y\right) = p_{SP}Ke^{\frac{E_M x^2}{V_T X_{CH}^*}} e^{-\frac{\Delta E}{2V_T}\left(y + \frac{Y_G + X_{CH}}{2} - \frac{E_M^{V_G}}{\Delta E}\right)^2} \tag{3.5}$$

where p_{SP} is given from (2.13) and

$$K = e^{\frac{1}{V_T}\left[-E_M^{V_G}Y_{SP} + \frac{\Delta E}{2}\left(\frac{Y_G + X_{CH}}{2} + Y_{SP}\right)^2 + \frac{E_M^{V_G}}{2}\left(\frac{E_M^{V_G}}{\Delta E} - Y_G - X_{CH}\right)\right]}$$

Note that (3.5) reduces to p_{SP} when is evaluated at $y=Y_{SP}$.

In order to evaluate n_{SP}, one has to consider that in sub-threshold regime the channel of a normally-off device is pinched-off from the depleted lateral gates. It is clear that, if the electron current exists, it must be necessarily filamentary around the saddle point with an area of ZL_d [55], indeed, when the cumulative effects of positive gate and

drain voltages are enough large to annul the barrier, namely $V_{S/CH}=V_{n+n}$ or, equivalently, $V_{G/CH}=V_{bi}-V_{GS}$, the drift current interests only the neutral region of the channel, namely $Z\Delta X_{Drift}$, which is wide:

$$\Delta X_{Drift} = X_{CH} - \left(a_1 - \sqrt{a_1^2 - a_2}\right) \tag{3.6}$$

where a_1 and a_2 are reported in (2.22.a) and (2.22.b), respectively. Therefore, since the electrons crossing the barrier are extracted by the electric field V_{DS}/X_{EPI}, the filamentary current can be written as follows:

$$I = qZv_n n_{SP}\left(\Delta X_{Drift} + L_d\right) \tag{3.7}$$

where the electron velocity

$$v_n = \frac{v_{SAT}}{1+\frac{v_{SAT}Y_{EPI}}{\mu_n V_{DS}}}$$

is written to coincide asymptotically with the saturation velocity v_{SAT} or $\mu_n V_{DS}/Y_{EPI}$ at high and low fields, respectively, by using (3.5) and (3.7) in (3.4), the total drain current can be expressed as:

$$I_D = \frac{1}{\frac{1}{2qD_nZ\frac{X^0}{Y^0}\frac{n_i^2 e^{\frac{V_{GS}}{V_T}}}{p_{SP}}} + \frac{1}{qZv_n\left(\Delta X_{Drift}+L_d\right)\frac{n_i^2 e^{\frac{V_{GS}}{V_T}}}{p_{SP}}}} = \frac{1}{\frac{1}{I_{Diff}}+\frac{1}{I_{Drift}}} \tag{3.8}$$

where the two terms describe the diffusive and ohmic amount of drain current, respectively, and

$$X^{\circ} = \sqrt{\frac{V_T X_{CH}^{*}}{E_M}} erf\left(\sqrt{\frac{E_M X_{CH}^{*}}{4V_T}}\right) \tag{3.9.a}$$

$$Y^{\circ} = K\sqrt{\frac{2V_T}{\Delta E}}\left\{erf\left(\frac{E_M^{V_G}}{\sqrt{2V_T\Delta E}}\right) + erf\left[\sqrt{\frac{\Delta E}{2V_T}}\left(\frac{X_{CH}+Y_G}{2}+Y_{SP}-\frac{E_M^{V_G}}{\Delta E}\right)\right]\right\} \tag{3.9.b}$$

It is worth to note that, once the barrier voltage is vanished, the channel becomes neutral, i.e. $n_i^2 \exp(V_{GS}/V_T)\, p_{SP}^{-1} = n_{SP} = N_{EPI}$, and the ohmic contribution begins to dominate, so that it can be written as:

$$I_{Drift} = qZv_n N_{EPI}\left(\Delta X_{Drift} + L_d\right)$$

3.3 Model Validation

The main parameters of the Si and 4H-SiC structures used as reference are reported in Table 2.1, including the active and the effective doping calculated by taking into account, for SiC, the partial ionization and the bandgap narrowing reported in APPENDIX A and assuming, for Si, the full activation of doping and the same bandgap narrowing model [59] for p^+ and n^+ regions. The use of different parameters values will be explicitly cited in the text.

3.3.1 Numerical simulation results

Fig.3.1a and 3.1b show the effect of Y_G and X_{CH}, respectively, on the I_D-V_{GS} curves obtained at two different V_{DS}. For a given V_{GS}, the dependence of drain current on V_{DS} tends to disappear as the aspect ratio X_{CH}/Y_G of the channel decreases. The discrepancy of the model for $X_{CH}=2\mu m$ in Fig.3.1b originates from the neglected electron density in $E^{1\text{-}D}$, as shown in previous chapter, which becomes relevant with the X_{CH} increase and leads to a lower carrier density p_{SP} value in (3.9.b) than that expected. This conclusion is also justified by

observing the discrepancy of few hundreds of *mV* of the model in Fig.2.8 for $X_{CH}=2\mu m$ and $Y_R=1\mu m$, which describes the limit geometry for the presence of $V_{S/CH}$ barrier when Y_G is set $1\mu m$ as in Fig.3.1b.

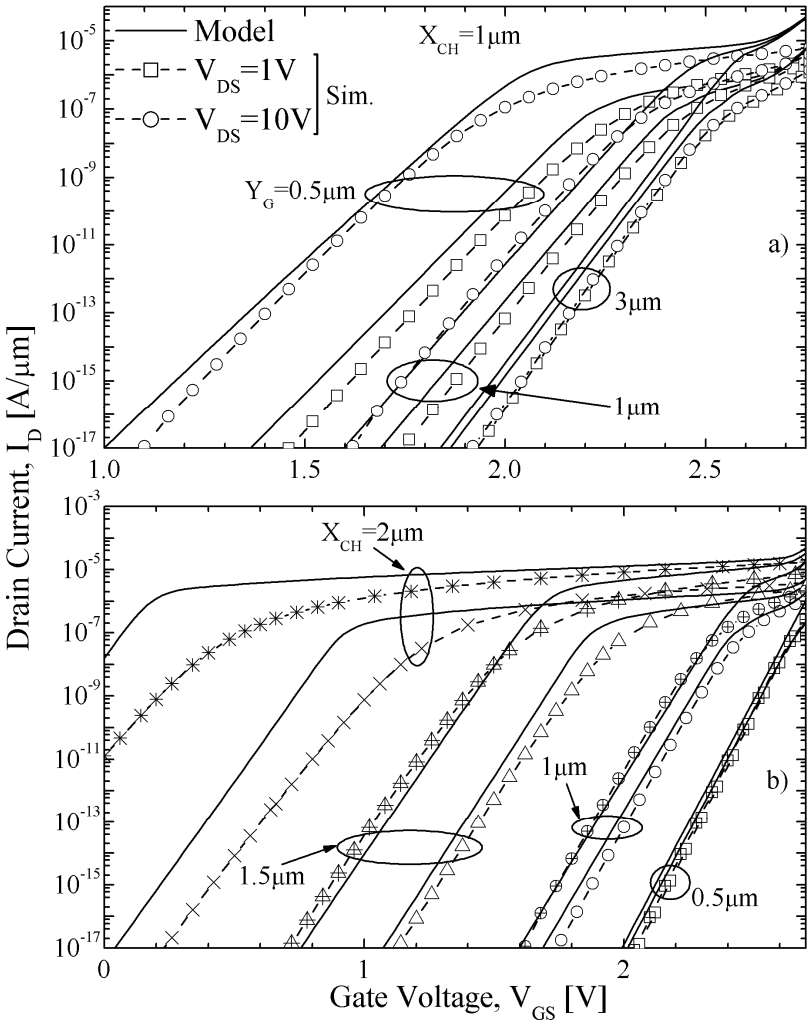

Fig.3.1. Model and numerical simulations comparisons of the I_D-V_{GS} curves for the 4H-SiC structure in Table 2.1 using (a) $X_{CH}=1\mu m$ with different Y_G and V_{DS} and (b) different X_{CH} at $V_{DS}=1V$ (symbol) and $V_{DS}=10V$ (symbol+cross).

Fig.3.2 shows the effect of Y_R on the I_D-V_{GS} curves for two X_{CH} values and a fixed Y_G. The need of recessed gates to guarantee the normally-off behaviour of device is evident by comparing the curves at $V_{GS}=2V$ and observing that the drain current increases as much as ten orders of magnitude when X_{CH} doubles from *0.5 to 1μm*. Finally, it must be observed that the modification of the slope of I_D-V_{GS} curves with the change of channel parameters and with V_{DS} is always well predicted by the model for all the cases examined so far.

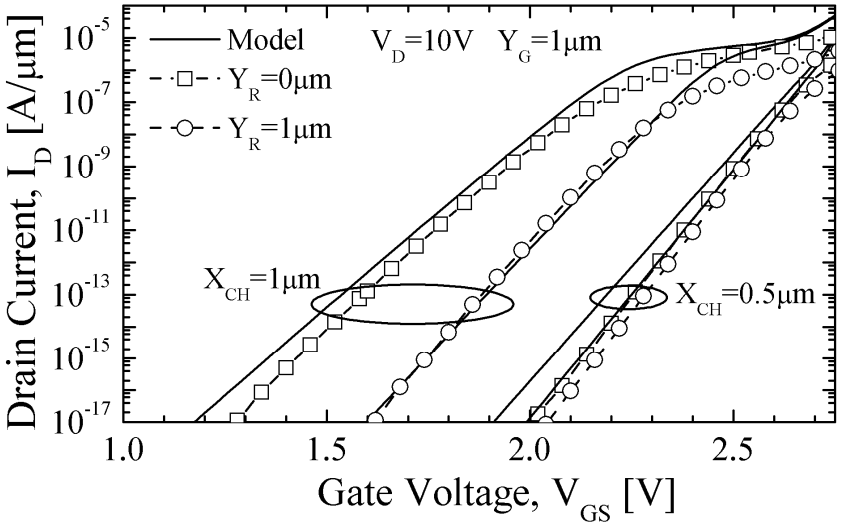

Fig.3.2. Model and numerical simulations comparisons of the I_D-V_{GS} curves, at $V_{DS}=10V$, using different X_{CH} and Y_R for the 4H-SiC structure in Table 2.1.

Besides the validity observed of the barrier model for SIT operation in Fig.2.10, the results of Fig.3.3a and 3.3b demonstrate its application on silicon BSITs structures [35], [60] by showing, respectively, the X_{CH}-dependence of the curves at two different V_{DS} voltages and the Y_G effect for a given geometry. The limitation of V_{DS} to *5V* in this case is due to the lower voltage for punching-trough the Si epilayer with respect to 4H-SiC, whose occurrence invalidates the present model.

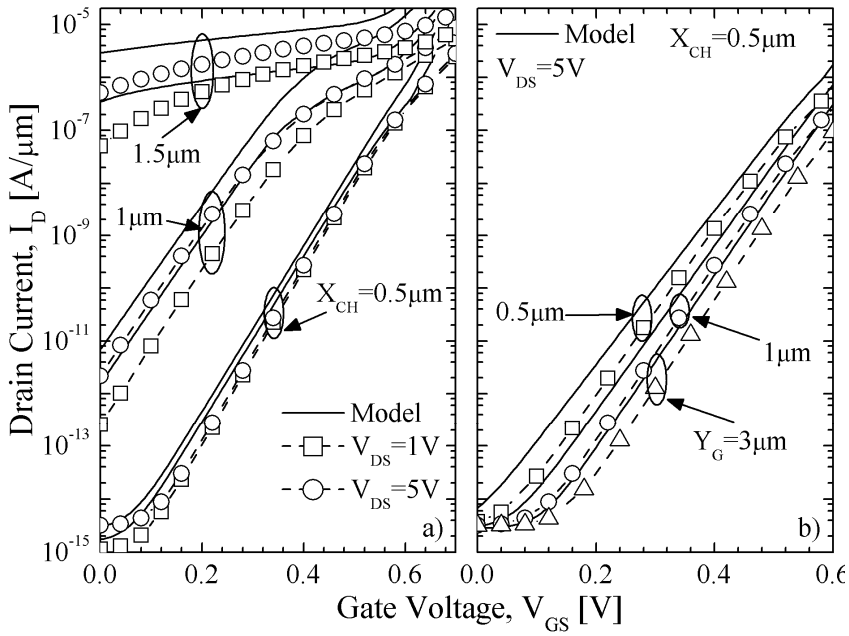

Fig. 3.3. Model and numerical simulations of I_D-V_{GS} curves for the Si structure in Table 2.1, obtained using (a) different X_{CH} and V_{DS} and (b) X_{CH}=*0.5μm*, V_{DS}=*5V* and different Y_G.

3.3.2 Experimental comparisons

In Fig.3.4 the model has been used to justify the I_D-V_{GS} characteristics measured on commercial 4H-SiC Vertical JFETs SJEP170R550 [9] with a blocking voltage of *1700V* and *8A* of nominal current. To overcome the lack of data in this case, the values of the channel parameters were taken from the results of reverse analysis made on this device in [61] (X_{CH}=*0.71μm*,Y_G=*2μm*,Y_R=*0μm*), the active area has been put equal to $8.6 \cdot 10^{-3} cm^2$ as in [62] and the resistance value of *550mΩ* given in [9] has been added as ohmic drop to the gate bias V_{GS}. Finally, since the channel of SJEP170R550 makes use of a bilayer, as shown in Fig.1.2, with the bottom layer $6 \cdot 10^{15} cm^{-3}$ doped, N_{EPI} value used in the model, which corresponds to the doping in the channel region of Fig.3.5, has been chosen $10^{16} cm^{-3}$ according to the higher doping of the top layer [62]. It is worth noting that both the slope of the measured curves, corresponding to an ideality factor of *1.2*, and their V_{DS} dependence is well predicted from the model, while the slight discrepancy observed in the vicinity of their curvature depends on the use of a constant resistance, with which it is ignored the higher ohmic drop of the bottom layer before that the conductivity modulation occurs.

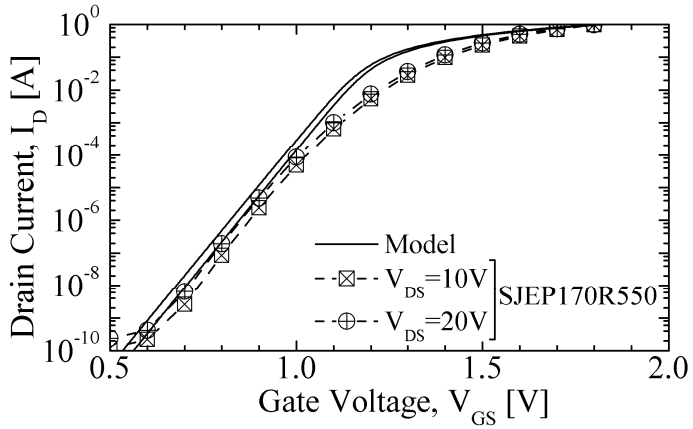

Fig. 3.4. Model and measurement comparisons of SemiSouth Laboratory Inc. SJEP170R550 I_D-V_{GS} characteristics at V_{DS}=*10V* and *20V*.

Chapter 4

Modeling of Reverse Recovery of 4H-SiC *p-i-n* Diode

4H-SiC *p-i-n* diode is a promising power device in addition to being the core structure of many bipolar transistors as well as BMFET. In the chapter a novel dynamic model of the *p-i-n* diode switching-off is shown and correlates the physical parameters, like lifetime and mobility which depends on the fabrication processes, with the electrical quantities, resulting a good instrument of investigation and design.

4.1 Motivation

4H-SiC *p-i-n* diodes and BJT are still under investigation in the attempt of improving the material properties [33], [63], [64], which are determinant in the bipolar operation. Among the various obstacles, one can find the low activated doping of terminal regions, which limit the injection capability of the junction, the scarce quality of SiO_2/SiC interface [65] required for surface passivation, the stacking faults effect [66] and the electron-hole scattering mechanism [67], which are a probable cause of the forward voltage increasing of *p-i-n* diodes at highest current. In this scenery with many questions still open, the use of *black-box* numerical simulators cannot be considered exhaustive since, differently than analytical models, they do not allow to separate the effects of physical parameters intervening on the electrical performances required at different operation conditions of diode. With the purpose to analyze the fundamental SiC parameters for bipolar

applications, such as apparent bandgap narrowing, carrier lifetime and partial doping ionization, models for the switching behavior of SiC diodes are absent in the literature [68] since the existing ones either merely give the voltage and current decays by using a lumped [69] and dynamic [70] charge model or are limited by strong assumptions concerning the heavily doped regions and the carrier distribution in the base [71] or, further, are unable to derive closed-form expressions of transient [72], [73]. Moreover, models proposed for the switching operation of silicon diodes [74] are unlikely to be extended to SiC since the recombination effects of the terminal regions are normally neglected due to the thicker base of silicon diodes. It must be finally remarked that only few models [75], [76] has been verified by comparisons with numerical simulations.

The proposed model is capable to describe the whole transient of the current and voltage for a wide range of physical parameters of SiC or other semiconductor materials and of forward-to-reverse current ratios. In more, the originality of the model is to obtain the spatial-temporal profiles of carriers, current components and electric field in the whole device, including the widening of the space charge region during the turn-off, with comparable accuracy of numerical simulations. Finally, it allows to highlight the influence of the boundary conditions represented by the p^+-n and n-n^+ junctions on the switching behaviour of diode, including the effect of the partial doping activation of terminal regions.

4.2 Switching-off Model

The one-dimensional p^+-n-n^+ structure used in our analysis is shown in Fig. 4.1 with a sketch of the minority carriers profile along the base and the main parts of the simulated measurement set-up. The diode transient is described by two consecutive phases, which are the storage, t_S, and *turn-off* intervals. During the storage interval, a constant reverse current flows through the diode whit the whole base remaining neutral and the electron-hole plasma stored therein tends to vanish due to both the electron-hole recombination and the carrier extraction from the electric field of the p^+-n and n-n^+ junctions; indeed, during the *turn-off* interval, the diode current, J_{Diode}, tends to

the saturation level and the depletion region significantly extends into the base, because the diode gets reversely biased. By defining in this model the storage time t_S as the time it takes for the hole density at the right border of the p^+-n junction to reduce to the doping level, namely until $p(0^+,t)=N_B$, it is clear that for $t>t_S$ the temporal variation of the electron and hole densities cannot be taken anymore equal at the right border of the junction, where the donor charge, qN_B, starts to prevail coherently with the space charge region extension, as schematized in Fig. 4.1a.

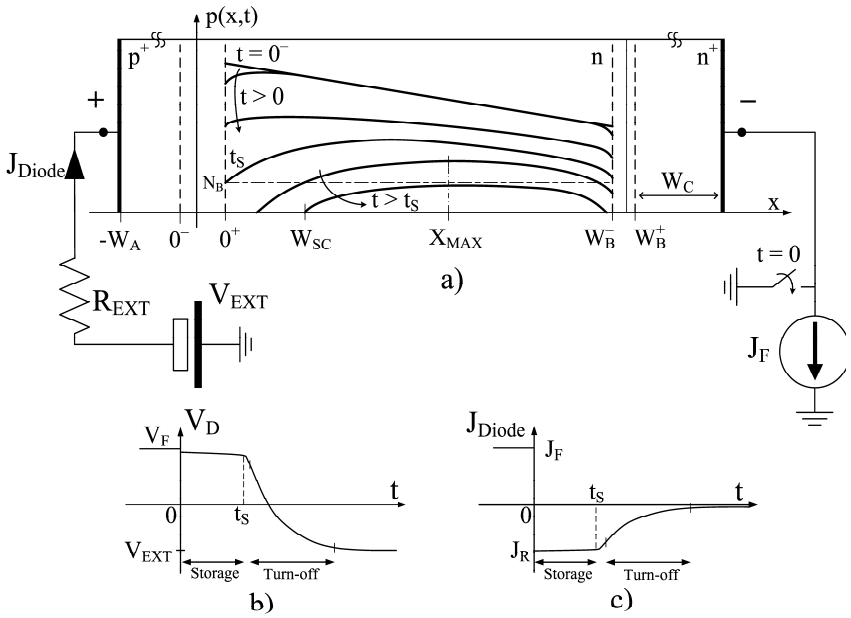

Fig.4.1 a) Basic circuit used for numerical simulations and schematization of temporal-spatial hole profiles during the switching-off. Typical shape of the voltage b) and current c) transients.

In order to evaluate the current and voltage transients conjunctly with the spatial-temporal distributions of carriers, electric field and current components in the device volume, at a generic instant, the fundamental equations of semiconductors are adequately treated. In

particular, by assuming the equality of the recombination rates, $U_p=U_n=U$, in the base and by manipulating the current density and continuity equations, one obtains the following equation:

$$\frac{p}{D_n}\frac{\partial n}{\partial t}+\frac{n}{D_p}\frac{\partial p}{\partial t}=n\frac{\partial^2 p}{\partial x^2}+p\frac{\partial^2 n}{\partial x^2}+\frac{E}{V_T}\left(p\frac{\partial n}{\partial x}-n\frac{\partial p}{\partial x}\right)-U\left(\frac{n}{D_p}+\frac{p}{D_n}\right) \tag{4.1}$$

The necessity to have (4.1) valid at a generic instant of the whole transient implies to write the electron density as:

$$n(x,t)=p(x,t)+N_B-N_B\cdot H\left(t-t_S\right)\cdot F\left(\Delta x\right) \tag{4.2}$$

because describes the coexistence of the donor charge appearance, occurring in a generic Δx space interval when $t>t_S$, with the presence of neutrality condition in the remaining part of the base. $F\left(\Delta\xi\right)=H\left(\xi\right)-H\left(\xi-\Delta\xi\right)$ is the boxcar function defined in terms of the Heaviside step function $H(\xi)$. Therefore, by substituting (4.2) in (4.1), one obtains:

$$\begin{aligned}\frac{\partial p(x,t)}{\partial t}-D_a\frac{\partial^2 p(x,t)}{\partial x^2}+\frac{p}{\tau_a}=\frac{E}{V_T}\frac{D_pD_n\left(p-n\right)}{D_pp+D_nn}\frac{\partial p(x,t)}{\partial x}-\\ -\frac{E}{V_T}\frac{D_pD_n}{D_pp+D_nn}N_Bp\left[\delta\left(x\right)-\delta\left(x-\Delta x\right)\right]H\left(t-t_S\right)+\\ +\frac{pD_nN_B}{D_pp+D_nn}F\left(\Delta x\right)\delta\left(t-t_S\right)\end{aligned} \tag{4.3}$$

where $\delta(\xi)$ is the Dirac delta function, representative of $H(\xi)$ derivative. The mathematical complexity due to the unknown electric field in (4.3) can be overcome by observing that, if the electric field is expressed from the sum of the current density equations in terms of J_{Diode}, namely:

$$E(x,t)=V_T\frac{\frac{J_{Diode}}{q}-(D_n-D_p)\frac{\partial p}{\partial x}-D_nN_B\delta(x-\Delta x)H(t-t_S)}{D_nn+D_pp} \qquad (4.4)$$

while substituting it in hole or electron current density, one obtains:

$$J_{p(n)}=\mp qD_a\frac{\partial p}{\partial x}+\lambda_{p(n)}J_{Diode}-q\lambda_{p(n)}D_nN_BH(t-t_S)\left[\delta(x)-\delta(x-\Delta x)\right] \qquad (4.5)$$

where V_T is the thermal voltage, $D_a=D_n\frac{p+n}{D_nD_p^{-1}n+p}$ the ambipolar diffusion coefficient in the base at arbitrary injection level and, finally, $\lambda_{p(n)}$ is the injection-dependent coefficient expressed as $\lambda_p=\frac{p}{D_nD_p^{-1}n+p}$ $\left(\lambda_n=\frac{D_nn}{D_pp}\lambda_p\right)$. By using (4.5) in (4.3) and by assuming the spatial derivatives of D_a and λ_p are neglected, the partial differential equation used in this model is as follows:

$$\frac{\partial p(x,t)}{\partial t}-D_a\frac{\partial^2 p(x,t)}{\partial x^2}+U=$$
$$=-\frac{\lambda_p}{q}\frac{\partial J_{Diode}(x,t)}{\partial x}-\frac{D_pD_nN_B}{D_nn+D_pp}\frac{\partial p}{\partial x}H(t-t_S)\left[\delta(x)-\delta(x-\Delta x)\right] \qquad (4.6)$$

which gives a more suitable expression for the r.h.s term of (4.3). Note that, writing $U=p/\tau_a$ accordingly to the Shockley-Hall-Read model, being $\tau_a=\tau_p+\tau_np/(p+N_B)$ the ambipolar carrier lifetime [77], depending on the carrier density values, D_a changes from $2D_nD_p/(D_n+D_p)$ to D_p, τ_a varies from $\tau_p+\tau_n$ to τ_p and, finally, λ_p assumes values between $D_p/(D_n+D_p)$ and zero, coherently with the irrelevant role of the electric field at low injections. As it will be

shown ahead, using the analytical model of the steady-state condition reported in APPENDIX C to describe the initial conditions of diode before switching, (4.6) can be easily solved to obtain closed form expressions of the spatial-temporal distribution of carriers valid from the stationary conditions up to the end of the transient. It is worth noting that, since the static model is based on the stationary solution of (4.6), the present model realizes along with it, a self-consistent tool for the analysis of SiC diodes under arbitrary operation conditions. In the following, the physical parameters will be denoted by the apex "*0*" to indicate their values under stationary conditions.

4.2.1 Storage

At $t=0^+$, J_{Diode} suddenly switches from a forward, J_F, to reverse value, J_R, and the forcing signal in the r.h.s. of (4.6) can be modeled as:

$$\frac{\partial J_{Diode}}{\partial x} = -\left[\left|J_R(t)\right| + J_F\right]\left[\delta(x) - \delta(x - W_B)\right]$$

while the temporal impulsive term on the r.h.s. of (4.6) must be put equal to zero. The main complexity to obtain from (4.6) the spatial–temporal carrier profile along the base, changing from a flat to concave shape as shown in Fig. 4.1a, originates from the need of accounting for the spatial–temporal variation of the physical parameters D_a and τ_a, which are the main causes of non-linearity of the differential equation. An easy way to account for the injection dependence of those parameters consists of assuming these parameters to be spatially constant along the base with their value taken at the peak, p_{MAX}, of the carrier profile. Therefore, assuming the constancy of J_{Diode} along the base, the solution of (4.6) results:

$$p(x,t) = p_S(x,t) + p_{F0}(x,t) + p_{FW}(x,t) \qquad (4.7)$$

where

$$p_S(x,t) = (A_0 + A_1 x)e^{-\frac{t}{\tau_a}} + \\ + \sum_{i=1}^{\infty}\left[B_i \cos\left(\frac{k_i}{\sqrt{D_a}}x\right) + C_i \sin\left(\frac{k_i}{\sqrt{D_a}}x\right)\right]e^{-\frac{t}{\tau_a}(1+k_i^2\tau_a)} \quad (4.8)$$

represents the homogenous solution of (4.6) and the resolution is reported in APPENDIX D. For the linearity of (4.6), $p_{F0}(x,t)$ ($p_{FW}(x,t)$) represents the solutions obtained by Laplace method when the pulse $\delta(x)$ ($\delta(x-W_B)$) is singly applied by imposing the initial condition $p_{F0}(x,0^+)=0$ ($p_{FW}(x,0^+)=0$) along the base and the Neumann condition describing the electron (hole) current leaving the base at $x=0^+$ $\left(x=W_B^-\right)$. The Neumann conditions are individuated observing that, since the minority currents injected into the cathode and anode cannot vary instantaneously and at $t=0^+$ they remain equal to the stationary values J_{pC}^0 and J_{nA}^0 given by (C-4) and (C-5), the sudden variation of the total current $\Delta J_{Diode} = \left(J_R - J_F\right)$ at the above abscissas can be justified only through the abrupt variation of majority hole and electron currents at $x=0^-$ and $x=W_B^+$, respectively. Since these majority currents move with saturated velocity across the space regions of the p^+-n and n-n^+ junctions and, hence, are the same at the two junction extremities due to the reduced space charge widths, the previous current balances, at $t=0^+$, can be extended to the low-doped side of the junctions, namely at $x=0^+$ and $x=W_B^-$, so that, using (4.5), one can write:

$$\begin{cases} \left.\dfrac{\partial p(x,t)}{\partial x}\right|_{\substack{x=0^+ \\ t=0^+}} = -\dfrac{\lambda_n^0 J_R - J_{nA}^0}{qD_a^0} \\ \left.\dfrac{\partial p(x,t)}{\partial x}\right|_{\substack{x=W_B^- \\ t=0^+}} = \dfrac{\lambda_p^0 J_R - J_{pC}^0}{qD_a^0} \end{cases} \quad (4.9)$$

or, by using (4.7):

$$\begin{cases} \left.\dfrac{\partial p_{F0}}{\partial x}\right|_{\substack{x=0^+\\ t=0^+}} = -\dfrac{\lambda_n^0 J_R - J_{nA}^0 + qD_a^0 \left.\dfrac{\partial p_S}{\partial x}\right|_{\substack{x=0^+\\ t=0^+}}}{qD_a^0} \\ \left.\dfrac{\partial p_{FW}}{\partial x}\right|_{\substack{x=W_B^-\\ t=0^+}} = \dfrac{\lambda_p^0 J_R - J_{pC}^0 - qD_a^0 \left.\dfrac{\partial p_S}{\partial x}\right|_{\substack{x=W_B\\ t=0^+}}}{qD_a^0} \end{cases} \tag{4.10}$$

Furthermore, observing that, for the assumed constancy of currents across the junctions, the continuity equations indicate that the carrier density at the low-doped sides varies exponentially as $\exp(-t/\tau_a)$ due to the neutrality condition, (4.10) can be extended from $t=0^+$ up to the end of transient and used as Neumann boundary conditions in the following manner:

$$\begin{cases} \left.\dfrac{\partial p_{F0}(x,t)}{\partial x}\right|_{x=0^+} = -\dfrac{J_{F0}}{qD_a^0} e^{-\frac{t}{\tau_a}} \\ \left.\dfrac{\partial p_{FW}(x,t)}{\partial x}\right|_{x=W_B^-} = \dfrac{J_{FW}}{qD_a^0} e^{-\frac{t}{\tau_a}} \end{cases} \tag{4.11}$$

where J_{F0} and J_{FW} represent the numerators of (4.10). Using the Laplace method, solutions $p_{F0}(x,t)$ and $p_{FW}(x,t)$ can be written as:

$$p_{F0(FW)}(x,t)=\frac{J_{F0(FW)}\sqrt{D_a}e^{-\frac{t}{\tau_a}}}{qD_a^0\sqrt{\pi}}\left[2\sqrt{t}e^{-\frac{(mW_B-x)^2}{4D_at}}-\right.$$
$$\left.-\sqrt{\frac{\pi(mW_B-x)^2}{D_a}}erfc\left(\sqrt{\frac{(mW_B-x)^2}{4D_at}}\right)\right] \tag{4.12}$$

where *m=0* (*m=1*)when (12) is referred to $p_{F0}(x,t)$ ($p_{FW}(x,t)$).

Once the hole distribution has been obtained from (4.7), the transient of the diode voltage $V_D(t)$ can be calculated from the same expression used for the stationary conditions in APPENDIX C and rewritten here to evidence the time-dependent quantities:

$$V_D(t)=V_T\ln\left(\frac{p(0^+,t)N_B}{n_i^2}\right)+\frac{D_n-D_p}{D_n+D_p}V_T\ln\left(\frac{p(0^+,t)+\frac{D_nN_B}{D_n+D_p}}{p(W_B,t)+\frac{D_nN_B}{D_n+D_p}}\right)$$
$$+V_T\ln\left(1+\frac{p(W_B,t)}{N_B}\right)+J_{Diode}\left(R_C+R_A+R_B(t)+R_S\right) \tag{4.13}$$

where $p(0^+,t)$ and $p(W_B,t)$ are calculated from (4.7) while, to account for the time-dependent conductivity of base, differently than the stationary model, the specific resistance of base has been simply written as: $R_B=\left[q\left(\mu_nN_B+(\mu_n+\mu_p)p_{MAX}(t)\right)\right]^{-1}W_B$. According to the circuit of Fig.4.1a, the total current density is written as follows:

$$J_{Diode}(t)=\frac{V_{EXT}-V_D(t)}{R_{EXT}} \tag{4.14}$$

being V_{EXT} the power supply and R_{EXT} the external resistance expressed by $[\Omega cm^2]$, indeed the electric field and the current distribution along the base are evaluated from (4.4) and (4.5).

4.2.2 Turn-off

To better clarify the modeling of the various physical and electrical parameters intervening in the turn-off interval, their derivation has been divided into different paragraphs.

4.2.2.1 Carrier distribution

As observed before, at the end of the storage time, namely when the condition $p(0^+,t_S)=N_B$ is reached, the right border of p^+-n junction enters the low-injection regime and, because of the hole removal operated by the electric field, the neutrality condition fails in vicinity of the junction thus allowing the widening of the space charge width, W_{SCR}. Analogously, depending on the reflecting properties of the n-n^+ junction, the carrier density at the n-n^+ junction tends to recombine because of the lower lifetime of substrate and the concave shape resulting in the carrier profile ensures the holes escape from the base extremities during turn-off. It is evident from the above observations that, firstly, the validity of V_{pn} in (4.13) fails since it must be rewritten to include the reverse voltage manifesting across the junction; secondly, the contribution of the impulsive term in the r.h.s. of (4.6) cannot be ignored in this case. In continuity with the storage analysis, by interpreting (4.7) as the homogeneous solution of (4.6) in the turn−off interval, the carrier distribution can be obtained by adding to (4.7) a fourth term, $p_{T0}(x,t)$, determined by imposing the boundary condition $p_{T0}(x,t_S)=0$ and the Neumann condition occurring at $t=t_S$, as made in (4.11). This condition can be written by observing that, since the electron density injected in the anode, at $x=0^-$, has become negligible, the total current (4.14) is composed solely by holes, so that using (4.7) in (4.5), this latter can be written as:

$$0 = J_{Diode}(t_S) + qD_a^{t_S} \left.\frac{\partial}{\partial x}\right|_{\substack{x=0^+ \\ t=t_S}} \left(p_s(t) + p_{F0}(t) + p_{FW}(t) + p_{T0}(t) \right) \quad (4.15)$$

which, similarly to (4.12), can be used as Neumann boundary condition

$$\left.\frac{\partial p_{T0}(x,t)}{\partial x}\right|_{x=0^+} = -\frac{J_{T0}}{qD_a^{t_S}} e^{-\frac{t-t_S}{\tau_a}} \quad (4.16)$$

where $D_a^{t_S}$ indicates the diffusion coefficient value at $t=t_S$. Therefore, by using (4.16) in conjunction with a null initial condition, one obtains:

$$p_{T0}(x,t) = \frac{\sqrt{D_a} J_{T0} e^{-\frac{t-t_S}{\tau_a}}}{qD_a^{t_S}\sqrt{\pi}} \left[2\sqrt{t} e^{-\frac{x^2}{4D_a(t-t_S)}} - \sqrt{\frac{\pi x^2}{D_a}} erfc\left(\sqrt{\frac{x^2}{4D_a(t-t_s)}} \right) \right] \quad (4.17)$$

which allows the calculation of the carrier distribution at $t \geq t_S$, as follows:

$$p(x,t) = p_S(x,t) + p_{F0}(x,t) + p_{FW}(x,t) + p_{TO}(t) \quad (4.18)$$

4.2.2.2 **Transients of current and voltage**

As said before, because of the prominent enlargement of the p^+-n junction depletion occurring while the current is still high, the voltage term representing V_{DIF} in (4.13) can be neglected and voltage component V_{pn} must be considered dependent on the junction width $W_{SC}(t)$ [78] as follows:

$$V_{pn} = V_{bi} - 2V_T - \frac{qN_B}{2\varepsilon} W_{SC}^2(t) \quad (4.19)$$

By observing that the charge variation determined by junction capacitance:

$$qN_B dW_{SC} = -J_{Diode}(t)dt \tag{4.20}$$

must be concomitant with the reduction of the hole charge density $qp_{MAX}(t)\left(W_B - W_{SC}(t)\right)$ accumulated in the neutral base, which can be written as:

$$qp_{MAX}(t_S)e^{-\frac{t-t_S}{\tau_a}}\frac{dW_{SC}}{dt} = -J_p(W_{SC},t) - J_{pC}(t) \tag{4.21}$$

where $J_p\left(W_{SC},t\right)$ and $J_{pC}\left(t\right)$ represent the hole flows leaving the neutral base, determined from the carrier gradient at $x=W_{SC}$ and the hole injection in the cathode, respectively, and we assumed that the peak value decreases exponentially with time. By using the equivalent transit time defined in [77] $\tau_{p,EQ} = \dfrac{\cosh\left(\dfrac{x_{MAX}(t)-W_{SC}(t)}{L_p}\right)-1}{\cosh\left(\dfrac{x_{MAX}(t)-W_{SC}(t)}{L_p}\right)}$ for describing the hole flow in the base portion $\left(x_{MAX}(t)-W_{SC}(t)\right)$, being $L_p = \sqrt{D_p\tau_p}$ the hole carrier diffusion length due to the low injection regime existing there, the former current in the r.h.s. of (4.21) results:

$$J_p\left(W_{SC},t\right) = qD_p\frac{p\left(x_{MAX}(t_S),t_S\right) - p(W_{SC},t_S)}{x_{MAX}(t_S)-W_{SC}(t_S)}e^{-\frac{t-t_S}{\tau_{p,EQ}}} \tag{4.22}$$

while the hole flow towards the substrate can be approximated with the cathode current related to the peak value as APPENDIX C:

$$J_{pC}(t) \cong qS_C p_{MAX}(t)\left(1+\frac{p_{MAX}(t)}{N_B}\right) \tag{4.23}$$

Note that $\tau_{p,EQ}$ reduces to τ_a or to the transit-time $\left(x_{MAX}(t)-W_{SC}(t)\right)^2 \Big/ \left(2D_p\right)$ when $\left(x_{MAX}(t)-W_{SC}(t)\right)$ is much greater or lower than L_p, respectively. Therefore, by using (4.22) and (4.23), (4.21) can be rewritten, as follows:

$$q\left(N_B + p_{MAX}(t_S)e^{-\frac{t-t_S}{\tau_a}}\right)\frac{dW_{SC}(t)}{dt} = -J_{Diode}(t) - J_p(W_{SC},t) - J_{pC}(t) \tag{4.24}$$

and, by expressing J_{Diode} as:

$$J_{Diode}(t) = \frac{V_{EXT} - V_{pn}}{R_{EXT} + \left(R_C + R_A + R_B(t) + R_S\right)} \tag{4.25}$$

with V_{pn} given from (4.19) and the specific injection-dependent resistance of base written as follows:

$$R_B(t) \cong \left[q\left(\mu_n N_B + (\mu_n + \mu_p)\, p_{MAX}\left(t_S\right)e^{-\frac{t-t_S}{\tau_a}}\right)\right]^{-1} W_B$$

can be numerically integrated to obtain $W_{SC}(t)$ at $t \geq t_S$ and calculate the total voltage $V_D(t)$ from (4.13). Otherwise, if the diffusive terms $J_p(W_{SC},t)$ and $J_{pC}(t)$ can be neglected, like for thin diodes, (4.24) reduces to the following:

$$\frac{dW_{SC}}{|h_1|W_{SC}^2-1}=\frac{h_2\left(h_3e^{-\frac{t}{\tau_a}}+1\right)}{\left(h_4e^{-\frac{t}{\tau_a}}+1\right)\left(h_5e^{-\frac{t}{\tau_a}}+1\right)}dt \tag{4.26}$$

which can be solved analytically to obtain the following closed-form:

$$W_{SC}(t)=\frac{1}{\sqrt{|h_1|}}\frac{1+\mathrm{H}(t)}{1-\mathrm{H}(t)} \tag{4.27}$$

where *H(t)* is reported in APPENDIX E.

4.3 Model Validation

The model is validated by direct comparisons among numerical simulation and experimental results of 4H-SiC *p-i-n* diodes, whose structure and physical characteristics are summarized in the Table 4.1 and the temperature is set to *298°K*.

REGIONS	DEVICE PARAMETERS	THEORETICAL					EXP.
		D1#	D2#	D3#	D4#	D5#	D6#
BASE	τ_{0np}/τ_{0n} [ns]	15/15	1E3/1E3	15/15	60/600	1E3/1E3	15/15
	W_B [μm]	5				15	5
	N_B [cm^{-3}]	3E15					3E15
	μ_p/μ_n [$cm^2V^{-1}s^{-1}$]	121/929					121/929
ANODE	τ_{0n} [ns]	15	1E3	15	600	1E3	15
	W_A [μm]	1.3					~1.3
	N_A (N_{aA}) ($N_{eff,aA}$) [cm^{-3}]	6E19 (5.4E17)(2.04E17)					6E19 (5.4E17) (2.04E17)
	μ_{pA}/μ_{nA} [$cm^2V^{-1}s^{-1}$]	60/52					60/52
CATHODE	τ_{0p} [ns]	15	15	1.5E-1	60	1E3	15
	W_C [μm]	100					300
	N_C (N_{dC}) ($N_{eff,dC}$) [cm^{-3}]	5E19 (4.9E18)(2.2E17)					5E19 (4.9E18) (2.2E17)
	μ_{pC}/μ_{nC} [$cm^2V^{-1}s^{-1}$]	62/54					62/54

Table 4.1 Geometrical and physical parameters for *p-i-n* diodes used in the comparisons among model, numerical simulation and experimental results at the room temperature.

4.3.1 Numerical simulation comparisons

To verify the accuracy of the injection-dependent ambipolar lifetime used in (4.6) even if a pronounced difference between the hole and electron lifetime exists, τ_{0n} and τ_{0p} coefficients have been put equal for the couples of devices (D1#, D3#) and (D2#, D5#), while with a ratio of ten in D4#; whereas, in order to evidence the model sensitivity to the substrate properties and epilayer thickness, D3# and D5# have been designed with the lowest substrate lifetime and the thickest epilayer, respectively.

From the stationary characteristics shown in Fig. 4.2, all the devices show a noteworthy ohmic drop for voltage and current higher than *2.8V* and *100A/cm*^{2}, respectively, mainly because of lower values of mobility and ionized acceptors of SiC, which reduce the hole injection capability of the anode in the epilayer. It is interesting noting that the effect of the lower epilayer lifetime in D1# and D3# is more evident at the lowest currents where the recombination current in the space charge region (C.2) dominates for all devices and that their curves remain always overlapped despite of the two-orders of magnitude lower lifetime of the substrate of D3#, suggesting the prevalence of the anode current J_{nA}^{0} (C.5) at the highest currents.

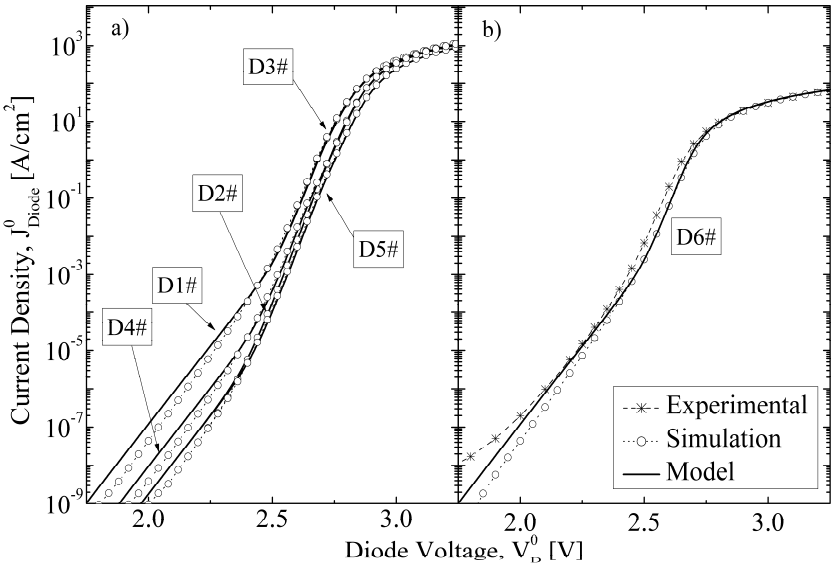

Fig.4.2 Steady-state characteristics of all devices used in the analysis.

This is also confirmed by the perfect coincidence at this regime of the D2# and D4# curves, despite of their slight τ_{0n} difference, while device D5# shows the largest ohmic voltage drop due to the thicker base. The effect of the lower substrate lifetime of D3# become more evident by comparing the transient behaviors of D1#, D2#, D3# in Fig.4.3, all switched from $J_F = 208A/cm^2$, corresponding to an injection level $p^0(0^+)/N_B$ of 8, 20 and 7.5, respectively, using $V_{EXT}=-3V$ and $R_{EXT}=0.1\Omega cm^2$.

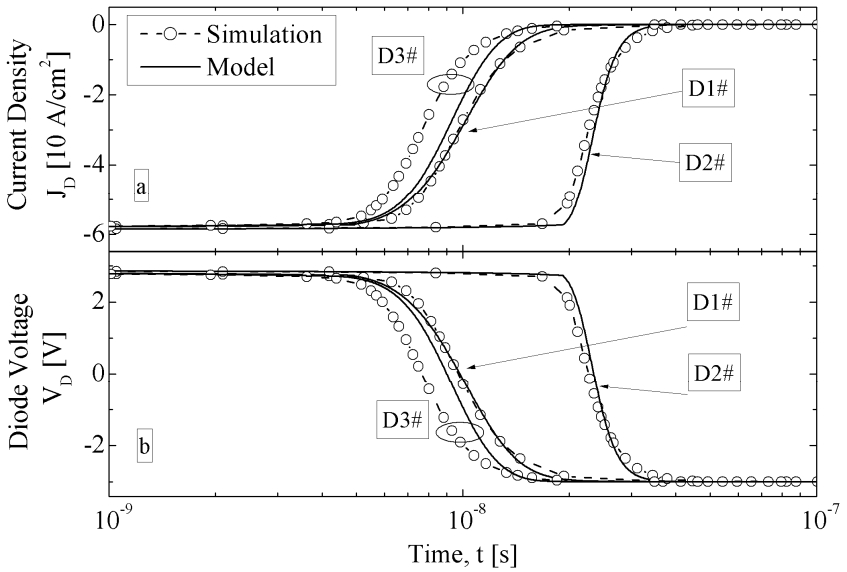

Fig.4.3 Current (a) and voltage (b) waveforms for diodes D1#, D2#, and D3# in Table 4.1, switched from $J_F = 208A/cm^2$ with $V_{EXT}=-3V$ and $R_{EXT}=0.1\Omega cm^2$.

The lower dV_D/dt shown by the model for the structure D3# at the beginning of turn-off depends from the inadequate expression used for $J_{pC}(t)$ in (4.23); in fact, because of the very low substrate lifetime of D3#, the carrier density at $x = W_B^-$ is much lower than p_{MAX} and that overestimates $J_{pC}(t)$, which ends to slow down the initial $W_{SCR}(t)$ variation in (4.23). The vanishing of the carrier accumulated at the epilayer-substrate interface of D1# at the end of the storage time is indirectly confirmed by the similarity of the turn-off behavior simulated for D1# and D3#.

The effects of different reverse voltages on the transient behavior of D5# when, biased at the same forward $J_F = 64A/cm^2$, it is switched by $V_{EXT}=-5V,-10V,-15V$ with a fixed load $R_{EXT}=0.1m\Omega cm^2$ are shown in Fig. 4.4, while the curves in Fig. 4.5 show the transient behavior of D4# when it is forward biased with $J_F = 1kA/cm^2$, which corresponds to the injection level $p^0(0^+)/N_B$ of 48, and then switched with the same $V_{EXT}=-10V$ but different R_{EXT} values equal to $13.5m\Omega cm^2$ (curve A) and ten times lower (curve B). To better evidence the effect of the extreme reverse currents, reaching the limit value of $J_{Diode} = -8kA/cm^2$ in the curve B, the external voltage V_{EXT} has been ramped to $-10V$ in $10psec$ and the carrier density $p(0^+)$ and $p(W_B)$ have been assumed in the model to remain equal to their stationary values.

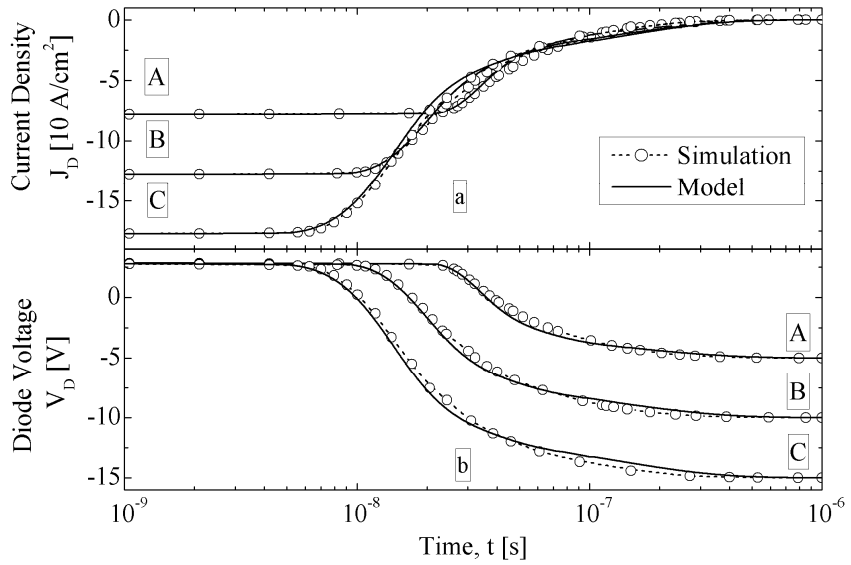

Fig.4.4 Current (a) and voltage (b) waveforms for diode D5# using different reverse voltages $V_{EXT}=-5V,-10V\ -15V$ and fixed $J_F=64A/cm^2$ and $R_{EXT}=0.1m\Omega cm^2$.

The voltage variation manifesting in the curve B with the V_{EXT} reduction must be attributed to the ohmic drop determined in (4.13) from the large current variation $(|J_R|+J_F)$, which is high enough to push the diode voltage below the stationary value, expected, in principle, equal in the two curves for the same value imposed to J_F.

Note that, despite of the different storage and shape of the two curves, in both cases the transients seem extinguishing in *10ns,* which is a clear proof for the recombination tail introduced by $J_{pC}(t)$ in (4.24). This is better evidenced from the results in Fig. 4.4a where, by recalling that the diode D5# has been designed with the highest lifetime, both the soft behavior and the curves coincidence at longer times arise from the significant hole density remaining accumulated in the base portion $W_B - x_{MAX}$ during turn-off. In other words, since p_{MAX} value is slightly modified from the increase of the reverse current from 1 to 3 in Fig. 4.4a, and, besides, $J_{pC}(W_{SCR},t)$ tends quickly to zero due to the reduced $\tau_{p,EQ}$ value, when the decreasing J_{Diode} becomes comparable with $J_{pC}(t)$, this latter intervenes to reduce $W_{SCR}(t)$ variation according to (4.24).

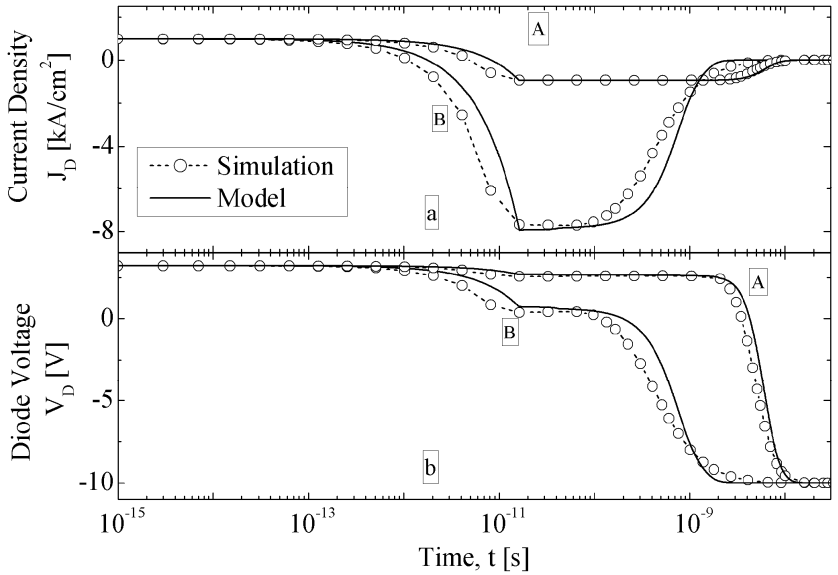

Fig.4.5. Current (a) and voltage (b) waveforms for diode D4# using different R_{EXT} and fixed J_F=*1kA/cm*^{2} and V_{EXT}=*-10V*. R_{EXT} value has been put equal *13.5mΩcm*^{2} for curve A and *1.35mΩcm*^{2} for curve B.

In Fig.4.6, the current and voltage transient of D1# are compared for different V_{EXT} and R_{EXT} values and by applying a $J_F = 208A/cm^2$ in order to show the accuracy of (4.24) and (4.27) in determining the transient of $W_{SCR}(t)$.

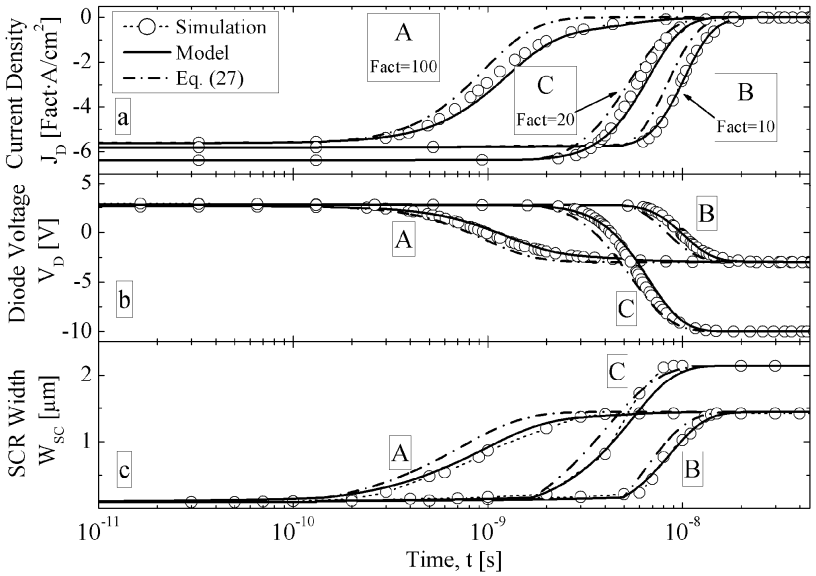

Fig.4.6. Current (a) and voltage (b) waveforms and temporal variation of the space charge width (c) for diode D1# using different reverse current and fixed $J_F = 208A/cm^2$.CurveA:$V_{EXT}=-3V, R_{EXT}=10m\Omega cm^2$;Curve B:$V_{EXT}=-3V$, $R_{EXT}=0.1\Omega cm^2$; Case C:$V_{EXT}=-10V$, $R_{EXT}=0.1\Omega cm^2$.

The accuracy shown from (4.27) in Fig. 4.6 does not follow from the low carrier lifetime used in D1#, as it can be seen in Fig. 4.7 where the voltage transients examined in Fig. 4.3-4.5, including those for the higher lifetime structures D2# and D5#, are recalculated with the $W_{SCR}(t)$ values given by (4.27) and compared with simulations. Note that the accuracy of (4.27) is relevant for D2# but fails dramatically for the thickest diode D5#, whose larger $W_B - x_{MAX}$ value is responsible both for the pronounced tail at longer times through $J_{pC}(t)$ and the slower slope at the first turnoff instants through the higher value of $\tau_{p,EQ}$ in $J_p(W_{SCR},t)$.

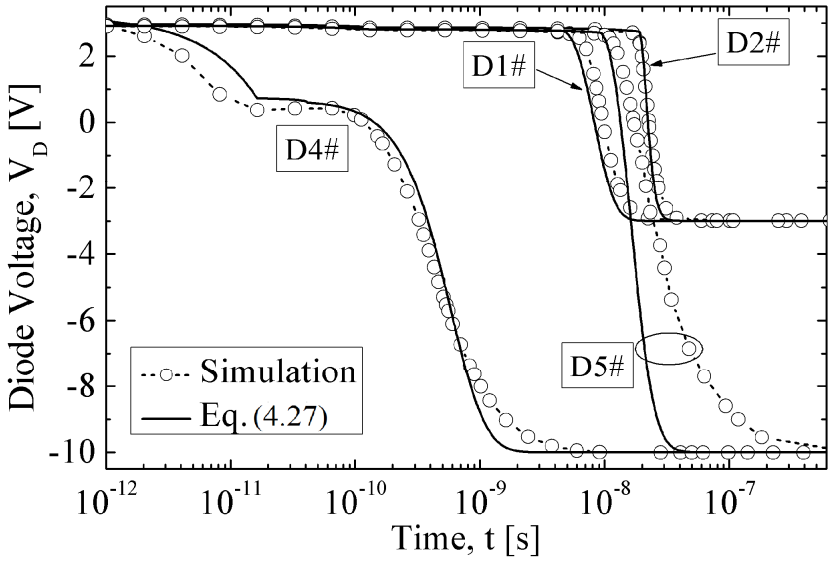

Fig.4.7. Comparisons of simulated voltage transients of D2# (Fig.4.3b), D5# (curve B in Fig.4.4b), D1# (Fig.4.3b) and D4# (curve B in Fig.4.5b) with the model using (4-27) for $W_{SCR}(t)$ calculation.

The accuracy of the model in determining the temporal-spatial distribution of the hole carrier density, hole current components and electric field is shown in Fig.4.8, where, for the same switching conditions used for D1# in Fig.4.3, the hole carrier profile given by (4.7) and (4.18), the electric field (4.4) and the hole current (4.5) are plotted at the various instants shown in the inset. By recalling t_S definition used in this paper, it is interesting noting from Fig.4.8a how, once the condition $p(0^+,t_S)=N_B$ is reached, the space charge widening of junction starts to appear, as it emerges also from the curve of the electric field in Fig.4.8c, and the hole current at the junction border becomes equal to the reverse current of $58A/cm^2$ imposed from the circuit, thus, confirming the negligible value of the electron injected in the cathode at $t=t_S$. In more, the movement of the abscissa x_{MAX} of carrier peak towards the substrate is well described by the model.

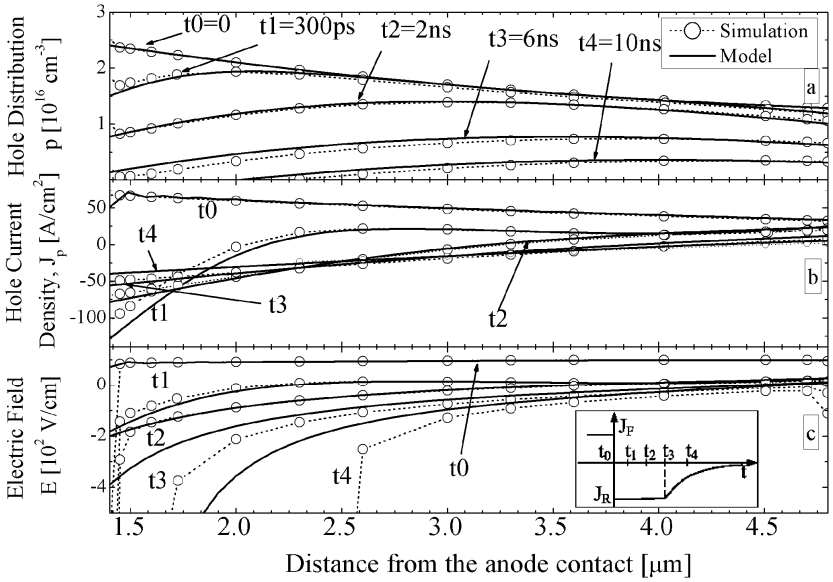

Fig.4.8. Transients of hole distribution (a), hole current density (b) and electric field (c) for diode D1# using J_F=*208A/cm*^{2}, R_{EXT}=*0.1Ωcm*^{2} and V_{EXT}=*-3V*.

4.3.2 Experimental comparisons

To compare the model with experimental data, the structure D6# in Table 4.1 is used. The static curves are compared in Fig.4.2b with the numerical simulations and the model obtained using a parasitic resistance of R_S=*5mΩcm*^{2} in (C-9).

In Fig. 4.9 the measured transients for J_F *(J_R)* value of *59A/cm*^{2} *(700/cm*^{2}*)* are compared with the model and simulations. The reverse voltage is *-40V* applied to the D6# structure and is the maximum voltage value before the punch-trough happens invalidating the model. Unfortunately, although the model accurately describes the diode transient, as proved by comparison with a simulation performed with a step voltage switching, Fig.4.9 show a strong mismatch between model and experimental, due to the substantial equivalence between the fall-time of the pulse generator and the diode lifetime, both equal to *15ns*, that causes the termination of the entire storage interval

during the voltage pulse switching. This is also confirmed by the comparison of experimental and a simulation performed with the same transient time of the pulse generator in Fig. 4.9.

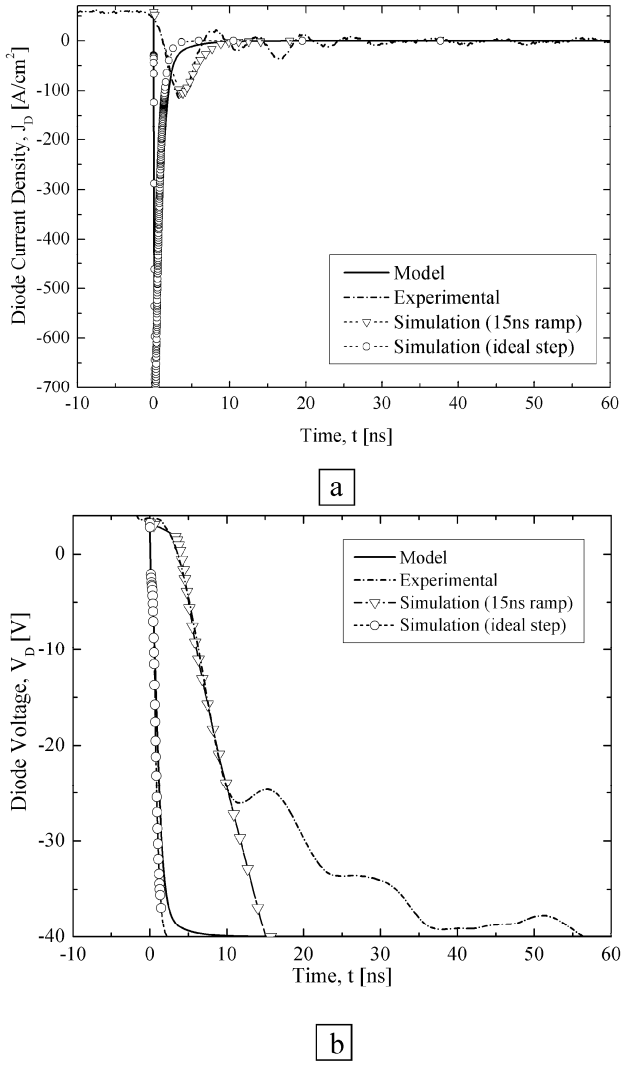

Fig.4.9. Comparisons of (a) current and (b) voltage waveforms for diode D6#. Switching conditions: J_F=59A/cm^2, R_{EXT}=57mΩcm^2, V_{EXT}=−40V.

In Fig.4.10 the effects of a non-ideal voltage pulse are reduced by applying to D6# two much smaller diode reverse voltages, namely V_{EXT}=*-1V* and V_{EXT}=*-0.5V*, in correspondence of J_F (J_R) values equal to *13.5A/cm²* (*18.9A/cm²*) (Curve A) and *8.8A/cm²* (*13.3A/cm²*) (Curve B), respectively. Although these voltage values are inappropriate for the diode under test, they allow to appreciate the good correspondence of the model with simulations and measurements during the whole switching interval.

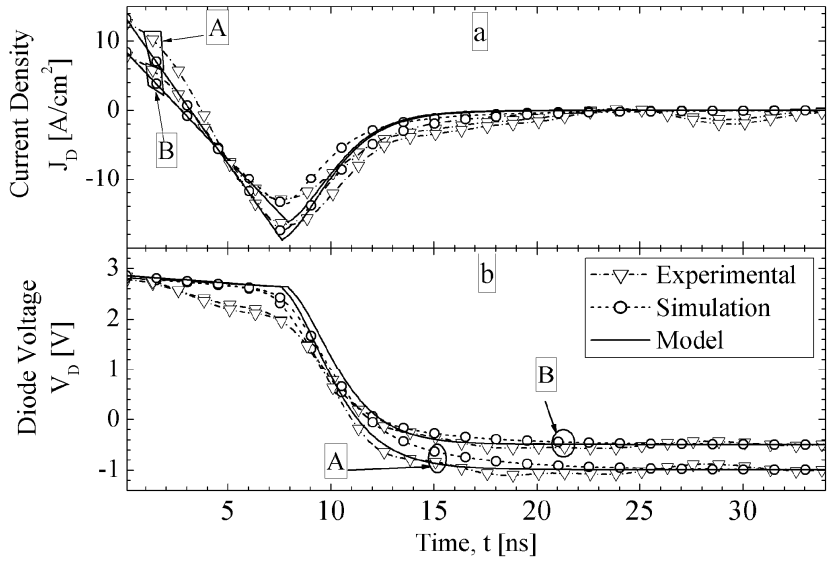

Fig.4.10. Comparisons of current (a) and voltage (b) waveforms for diode D6# . Switching conditions: CurveA: J_F=*13.5A/cm²*, R_{EXT}=*200Ωcm²*, V_{EXT}=*-1V*. Curve B: J_F=*8.8A/cm²*,R_{EXT}=*200Ωcm²*,V_{EXT}=*-0.5V*.

4.4 Circuit Representation of the Model

Equivalent electrical circuit of the static and dynamic *p-i-n* models are reported in Fig.4.11. For the stationary model, i.e. S_W is on *S*, $p^0(0^+)$ is defined by applying a V_{pn}^0, which defines the total diode voltage at low injection regimes. Indeed, once the switching-off is started, i.e. S_W is on *D*, the dynamic model, which is expressed by (4.14) and (4.21),

is reported in the right side of the circuit. In the storage interval, the switch, S_{W2}, is closed and the diode voltage coincides with (4.13) until V_{pn} has reached $V_{RIF} = 2V_T \ln\left(N_B/n_i\right)$. For $t \geq t_S$, the switch opens and the transient is governed by the charge of the capacitance $C_j^* = \frac{\varepsilon}{W_{SC}}\left[1+\frac{p_{MAX}\left(t_S\right)e^{-\frac{t-t_S}{\tau_a}}}{N_B}\right]$ with a net current determined by the difference between $J_{Diode}\,(t)$ and $J_p(W_{SCR},t)+J_{pC}(t)$.

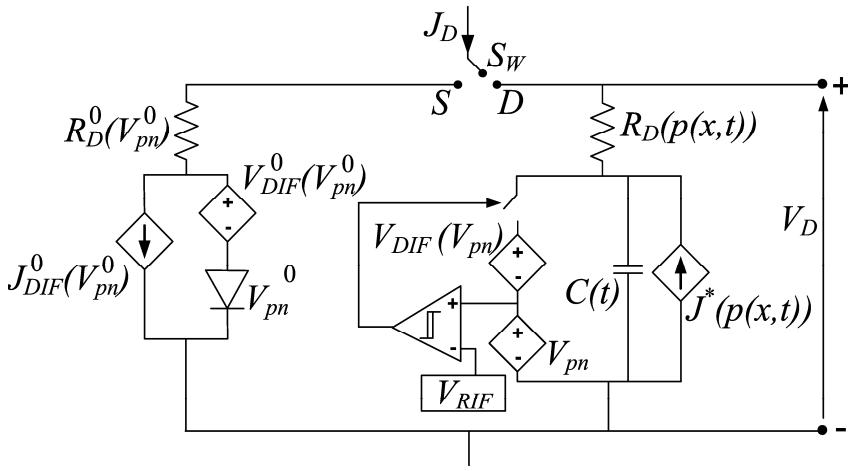

Fig.4.11. Circuit schematic of both static and dynamic models.

Chapter 5

Hole Injection Efficiency of Implanted p^+ Anode Regions

Basically, the BMFET principle of the conductivity modulation depends on the capability to inject hole carriers from the Gate regions to the Channel in order to have a lower on−state resistance than that of unipolar counterpart. In this chapter the hole injection efficiency is studied by considering two phenomena: incomplete ionization and band−gap narrowing. From the analysis of the heavy doping effects by using numerical simulations of a 4H−SiC $p-i-n$ diode, the ionized acceptor concentration value, that maximizes the hole injection and the forward current, has been found in the range of $5\times10^{18}cm^{-3}$ and $5\times10^{19}cm^{-3}$ which correspond to the Al^+ implanted concentration of about $2\times10^{20}cm^{-3}$ with a post implantation annealing temperature as high as *1950°C*.

5.1 Motivations

p^+-n junctions are fundamental parts of micro−electronic devices and in 4H−SiC technology they are manufactured both by multilayer epitaxial growth and by selective area ion implantation. Because the epitaxial growth is only feasible for a planar surface, it does not permit to obtain a generic device topology, limiting the development of novel concept devices. In order to overcome that, ion implantation is the unique solution to process selective area, but has to be joined to a very high temperature post implantation annealing, because the damage produced by the ions in the implanted crystal has to be

recovered and the implanted doping species have to be electrically activated. In fact, for equivalent doping values and nominal blocking voltage, the most of the implanted bipolar diode have shown higher forward voltage drops and lower blocking voltages than epitaxial junctions [80]. As a consequence ion implantation process has been generally used for constructing junction terminal extensions [81] or for increasing doping densities in the areas of ohmic contacts.

Another important aspect regards the incomplete ionization of Aluminum (Al), which is the more common p−type dopant of SiC. Its ionization energy is about *190meV* and for obtaining a p−type conductivity with a hole concentration higher than $5\times10^{18}cm^{-3}$ at room temperature a much more higher concentration of doping atoms in substitutional position is necessary. The maximum Al incorporation in epitaxial 4H−SiC has been as high as $3\times10^{20}cm^{-3}$ for growing temperature as low as *1300°C* [82], claiming a sheet resistance of about $10^{-2}\Omega cm$ without showing carrier density. Indeed, for epitaxial growth temperature of *1500°C* and an Al incorporation of $5.5\times10^{19}cm^{-3}$, an hole density of about $4\times10^{18}cm^{-3}$ at room temperature has been obtained in [83]. Concerning the doping by Al^+ ion implantation, an elevated p−type conductivity has been obtained by increasing the implanted Al concentration per unit volume up to the low $10^{21}cm^{-3}$ [84] and by increasing the post implantation annealing temperature up to *1800°C* [85]. Very recently a minimum p−type 4H−SiC material resistivity in the low $10^{-2}\Omega cm$ range with an hole density above $10^{19}cm^{-3}$ at room temperature have been obtained for an implanted Al concentration of $8\times10^{20}cm^{-3}$ and a post implantation annealing temperature upper to *2000 °C* obtained by a microwave induced heating [86]. Subsequently a very similar result has been obtained for a post implantation annealing temperature of *1950°C* obtained by a conventional inductively heated system [87].

In this chapter simulations of hole injection into the base and forward current−voltage characteristics of 4H−SiC $p-i-n$ diodes have been performed with the aim to emphasize the high doping effects and the incomplete ionization phenomena in the Al^+ anode region. It is shown that a high hole injection level and an elevated forward diode current density are obtained for thinner base and by increasing the ionized acceptor doping up to $5\times10^{18}cm^{-3}$. In more, for any other

value above $5\times10^{18}cm^{-3}$, the hole injection and forward current tend to saturate because of the effective hole density in p−type anode, which is limited by the bandgap narrowing effect.

5.2 Simulation of $p^{+}-n$ Junction: Hole Carrier Distribution and Forward $J-V$ Curves

Numerical simulation has been used to obtain the hole depth profiles and the forward current−voltage characteristics of vertical 4H−SiC $p-i-n$ diodes with Al^{+} ion implanted anodes. Simulation assumes an acceptor depth profile flat over $0.3\mu m$ next to the sample surface followed by a decreasing concentration towards the base where the metallurgical junction is formed at $1.3\mu m$ depth. Hole density values, N_{aA}^{-}, of 5×10^{17}, 5×10^{18} and $5\times10^{19}cm^{-3}$ in the acceptor plateau region has been considered in the simulation, while a fixed n^{-} doping of $3\times10^{15}cm^{-3}$ and carriers lifetimes of $15ns$ [88] have been assumed in the base region. In order to focus on the hole injection efficiency and its effects, two $p-i-n$ structures are considered: the first is a $25\mu m$−thick epilayer ($\rho_{EPI}Y_{EPI}=5.3m\Omega cm^2$) with an anode contact resistance of $0.4m\Omega cm^2$, neglecting that at the cathode, the second is a $5\mu m$−thick epilayer ($\rho_{EPI}Y_{EPI}=0.8m\Omega cm^2$) without any contact resistance. The physical models are reported in the APPENDIX A.

The hole carriers concentration profiles are reported in Fig.5.1(a) and it is clear that at the same forward voltage the hole carrier injection is higher for the thinner base. The reason of this difference is due to the less intense recombination in this structure, if one considers the same injection at the anode−base interface and the same recombination rate but with different volumes of the base. Indeed, in both the epilayer thicknesses the increasing of the injected hole level saturates when the ionized atoms concentration reaches $5\times10^{18}cm^{-3}$. In order to understand this phenomena it is necessary considering Fig.5.1(b) in which it is shown the saturation trend of the effective majority carrier concentration, $N_{aA,eff}=N_{aA}^{-}e^{-\frac{\Delta E_A}{kT}}$, in the anode region, where k is the Boltzmann constant and T is the absolute temperature; due to the shrinking of the band−gap, ΔE_A, as heavy doping effect

[89], for a real hole density between $5\times10^{18}cm^{-3}$ and $5\times10^{19}cm^{-3}$, the effective hole concentration varies of a few unit in the decade $10^{18}cm^{-3}$, while it increases of an order of magnitude by changing from $5\times10^{17}cm^{-3}$ to $5\times10^{18}cm^{-3}$.

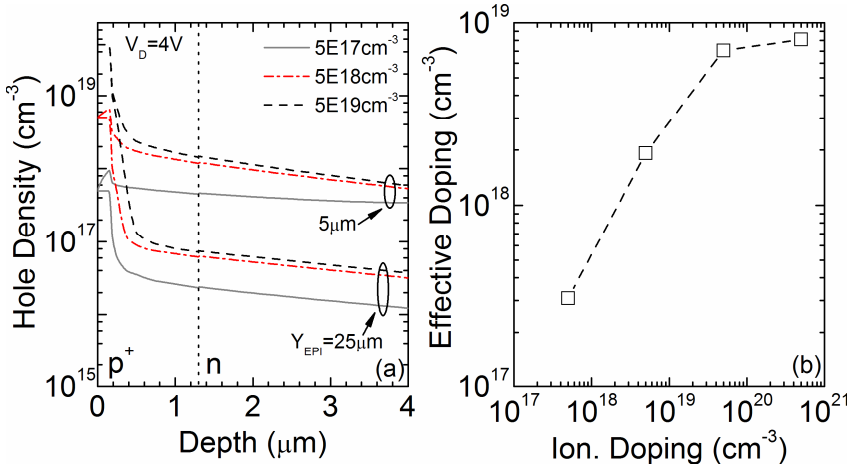

Fig.5.1 (a) Hole depth profile for different Y_{EPI} and ionized acceptor concentration values of the Al^+ implanted anode at a forward voltage of $4V$. The vertical dashed line represents the metallurgical junction. (b) Effective doping concentration in the anode as function of ionized acceptor density (Ion. Doping).

About the forward diode current density, the numerical results are reported in Fig.5.2 for the same diode structures of Fig 5.1.a. The trend of maximum forward current values is linked to that of minority carriers injection into the anode, J_{nA}, thus very similar to that shown in Fig.5.1 for hole injection in the base. In particular, maximum forward current is larger in the thinner base, for which the series resistance is less of two order than that unipolar due to the conductivity modulation, and increases by increasing of the majority carriers concentration in the anode up to 5×10^{18} cm^{-3}, for any further increasing a weak increase of maximum forward current density is found for the same epilayer base thickness.

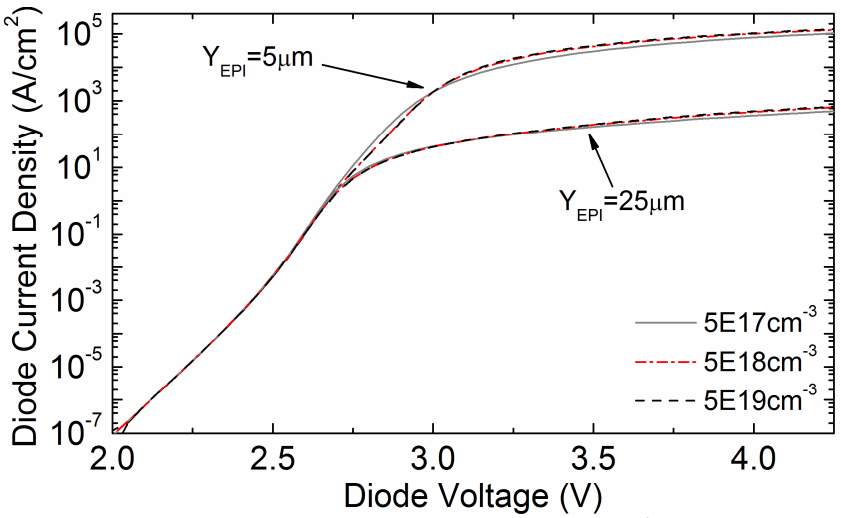

Fig.5.2. Simulated forward current-voltage characteristics of Al^+ implanted 4H-SiC p-i-n diodes for different values of the activated acceptor concentration and of the n-type base thicknesses.

The model shown in APPENDIX C can help the reader to explain the influence of J_{nA} on the total diode current, J_D; it consists to separate J_D in four components, as follows:

$$J_D = J_{EPI} + J_{SCR} + J_{pC} + J_{nA} \quad (1)$$

where J_{SCR} and J_{EPI} are the recombination current densities in p^+-n Space Charge Region and in neutral base, respectively, and J_{pC} is the minority diffusion current density into the cathode region. In Fig. 5.3 the comparison of the forward current–voltage characteristic obtained from numerical simulation and model results is reported for a diode base thickness of $25\mu m$ and a majority carrier concentration into the anode region of $5\times10^{17}cm^{-3}$ and with a series contact resistance of $0.4m\Omega cm^2$. Observing the curves, if at low diode voltage ($V_D<2.7V$) the recombination currents dominate, for higher diode voltage J_{nA} defines the total diode current.

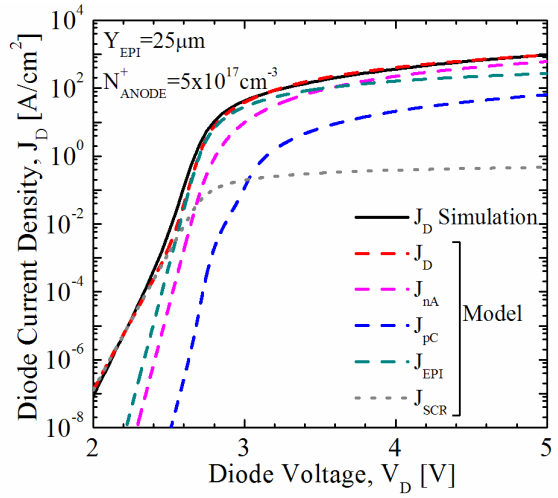

Fig.5.3. Comparison between model and numerical simulation results of the forward current-voltage characteristic for $Y_{EPI}=25\mu m$ and $N_{aA}^{-}=5\times10^{19}cm^{-3}$.

Furthermore, being J_{nA} expressible in terms of anode physical parameters, as follows:

$$J_{nA}=q\frac{D_{nA}N_B}{L_{nA}N_{eff,aA}}\coth\left(\frac{W_A}{L_{nA}}\right)p\left(0^+\right)\left(1+\frac{p\left(0^+\right)}{N_B}\right) \tag{5.2}$$

where q is the elementary charge, D_{nA} and L_{nA} are the electron diffusion and coefficient in the anode region, respectively, W_A is the anode depth, N_B is the base doping concentration and $p(0^+)$ is the hole concentration injection level into the base, the weak increasing of the current densities shown in Fig.5.2 is mainly attributable to saturation of the effective doping concentration and of the hole injection level. Taking into account the very high ionization energy of Al in 4H–SiC, which is about *190meV*, and the possible presence of compensating defects in the material due to the lattice damage during the ion implantation process, the acceptor concentration of Al substitutional atoms in the 4H–SiC lattice has to be much more elevated of the desiderate majority carrier concentration. In conclusion, from all these aspects an optimal value for ionized acceptor at room temperature in

the anode of a 4H−SiC $p-i-n$ diode could be in the range of $5\times10^{18}cm^{-3}$ and $5\times10^{19}cm^{-3}$ in order to have the maximum advantages in terms of diode electrical performance and of technology issue.

5.3 Hole Densities in Al^+ Implanted Regions

In this section results of experiments concerning the electrical activation in Al^+ implanted 4H−SiC are shown and discussed to suggest the better processing condition for obtaining a desired hole density value in the anode region of an Al^+ implanted 4H−SiC $p-i-n$ diode.

In order to obtaining a batter isolation of the implanted layer during electrical characterization, a High−Purity Semi−Insulating (HPSI) 4H−SiC wafers Si−face 8° miss−cut from the <0001> axis has been used for studying the post implantation annealing of Al^+ implanted layers. Al depth profiles with a plateau of about $0.3\mu m$ width and various heights between $5\times10^{19}\ cm^{-3}$ and $8\times10^{20}\ cm^{-3}$ have been performed with runs of multiple energies and doses by heating the sample at *573−673K*. The correspondence between as implanted and desired Al profiles has been verified by Secondary Ion Mass Spectroscopy (SIMS) measurements [86]. Once completed the ion implantation process, the post implantation annealing has been performed in a modified JIPELEC inductively heated furnace, where sample holder is a glassy carbon coated graphite crucible, and the characteristics of the thermal cycle were the heating rate of *40K/s* and the exponential cool down ramp with a characteristic time of about *3minutes*. The process has been performed in a high purity Argon ambient at *1atm* with an annealing temperature and time of *2220°C* and *5minutes*.

At *2220°C* the SiC sample surface must be protected to prevent a step bunching phenomenon by coating the implanted samples with a pyrolysed resist film (C−cap) layer, which can resist up to *2370°C* for *30seconds* [86]. A detailed receipt for manufacturing this C−cap is published in [90]. After the very high temperature annealing this C−cap has been removed by a dry thermal oxidation at *1120°C* for *10minutes* and root mean square surface roughness obtained by atomic force microscopy (AFM) shows values in the range of $0.5\pm0.1nm$ and

7.8±1.2nm with increasing roughness for the increasing of the implanted Al concentration.

Hall carrier density and sheet resistance have been obtained from electrical characterizations at room temperature and with a magnetic field of *1T* and a Hall scattering factor of *0.77* [91]. The devices were $5\times5mm^2$–square Van der Pauw structures with Ti/Al ohmic contacts on the corners [92]. Fig. 5.4 shows the comparison between the measured hole densities in the samples of this study and that obtained in the Al^+ implanted anode of 4H–SiC $p-i-n$ diodes previously fabricated with a post implantation annealing of *1870°C/20minutes*. It is evident the better electrical activation of the implanted Al^+ by increasing the post implantation annealing temperature from *1870°C* to *2220°C*. From the comparison between experimental data and reference line of $5\times10^{18}cm^{-3}$, it is shown that an Al concentration of at least $2\times10^{20}cm^{-3}$ has to be implanted for obtaining the desired majority carrier concentration in the anode of $p-i-n$ diode.

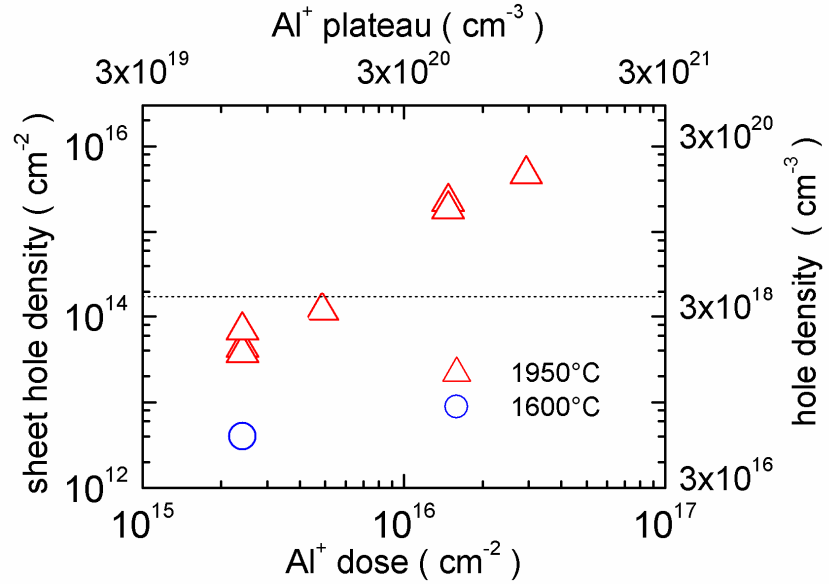

Fig. 5.4. Hole density in the Al^+ implanted layers in terms of the Al implanted atoms for *1600°C/20min* and *1950°C/5min*. The horizontal dashed line corresponds to the majority concentration of $5\times10^{18}cm^{-3}$.

In more, a much higher hole concentration is reported and, as shown in Fig.5.5, it corresponds a very low resistivity of around *30mΩcm*. Although the possible improvements of a high hole concentration are counteracted by the heavy doping effects in terms of hole injection level and forward current density for the same epilayer base thickness as shown previously, a high activated doping concentration is useful to fabricate ohmic contacts and p−type regions with very low ohmic drops and with reduced effects due to the parasitic resistances.

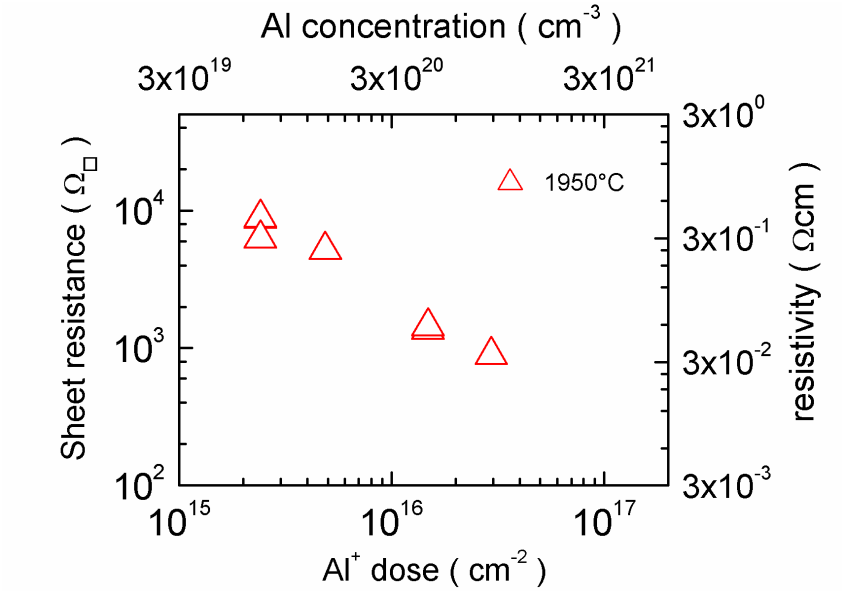

Fig.5.5. Sheet resistance of the Al^+ implanted layers after a *1950°C/5min* annealing. Sheet resistance has been converted in the material resistivity by taking into account the thickness of the implanted layers (*0.3μm*).

Chapter 6

BMFET Mask Design

In this chapter the BMFET mask layout are shown with the main process steps to fabricate the transistors.

6.1 Process Steps

The fabrication process is mainly summarized in 27 steps as reported in Tab.6.1. In Fig.6.1 the six mask layouts are reported, indeed, in Fig.6.2 the superposition of the first five mask levels is shown where the main regions of the transistor are highlighted. The substrate is a 4H-SiC n-type <0001> Si-face 4°off-axis (*ρ=20mΩcm*) wafer on which a n-type 10µm-thick epitaxial layer was grown with a doping of $10^{15}cm^{-3}$.

Process	***Description***
Cleaning	- Boiling trichloroethylene for 5 minutes. - Boiling acetone for 5 minutes. - Boiling isopropyl alcohol for 5 minutes. - Piranha for 5 minutes. - HF:$H_2$0-1:10 for 30 seconds.
Ion Implantation	At the top of wafer, Phosphorous ion implantation at 400°C for the Source region formation: flat profile with 0.7um depth and $5x10^{19}cm^{-3}$ doping peak.
Deposition	- Chemical Vapor Deposition (CVD) densification on the top of sample of an oxide layer. - At the top of wafer, sputter deposition of Aluminum layer (with 1% of Si).
Photolithography-Gate	- Photoresist modeling to transfer the implantation mask on the

	surface of the Al-layer (MASK 1). - UV radiation.
Wet-Etching	- Etching of the Al layer by Alu Etch (composed of acetic acid, ortophosphor acid and nitric acid) for define the implantation mask. Definition of the Source region with 4µm width. - Photoresist cleaning.
Implantation	At the top of wafer, Aluminum ion implantation at 400°C for the Gate regions formation: flat profile with 0.5um depth and $6x10^{19}cm^{-3}$ doping peak.
Dry-Etching	Removal of implanted superficial p-type layer from the top of samples by RIE.
Cleaning	- Elimination of mask layer of Aluminum by Alu Etch. - Elimination of oxide layer by HF:H_20-1:5 for 15 minutes. - Piranha for 5 minutes. - HF:H_20-1:10 for 30 seconds. - RCA cleaning for preparing the surface at heat treatment.
Annealing	At 1600°C for 30 minutes, with 40°C/s ramp, in Ar environment.
Deposition	Chemical Vapor Deposition (CVD) on the top of the sample of an oxide layer.
Photolithography-Active Area	- Photoresist modeling to transfer the mask layer (MASK 2). - UV radiation.
Etching	- Etching the n-type region and definition of the device active area. - Photoresist cleaning.
Cleaning	- Elimination of oxide layer by HF:H_20-1:5 for 15 minutes. - Piranha for 5 minutes. - HF:H_20-1:10 for 30 seconds.
Photolithography-Metal 1	- Photoresist modeling for the transfer of the mask layer (MASK 3). - UV radiation.
Deposition Titanium	Sputter deposition of Titanium-layer with 0.08um thick on the top of the samples.
Lift-off	Definition of the Gate contacts by lift-off.
Photolithography-Metal 2	- Photoresist modeling for the transfer of the mask layer (MASK 4). - UV radiation.
Deposition Nickel	Electron beam deposition of a 0.3um-layer of Nickel.
Lift-off	Definition of the Source contacts by lift-off.
Deposition Nickel	Electron beam deposition of a 0.3um-layer of Nickel on the back surface.
Annealing	Samples annealing at 1000°C in vacuum, for 2 minutes.

Deposition Nickel	Chemical Vapor Deposition (CVD) on the top of sample of an oxide layer.
Photolithography-Opening contacts	- Photoresist modeling for the transfer of the mask layer (MASK 5). - UV radiation.
Etching	- Etching of the oxide and opening of the metal via to the Source and Gate metals. - Photoresist cleaning.
Deposition Aluminum	Sputter deposition of Aluminum-layer with 1um thick on the top of the sample
Photolithography-Pads	- Photoresist modeling for the transfer of the mask layer (MASK 6). - UV radiation.
Etching	- Etching of the Aluminum metal to define the pads. - Photoresist cleaning.

Table 6.1 Main steps of the BMFET process fabrication.

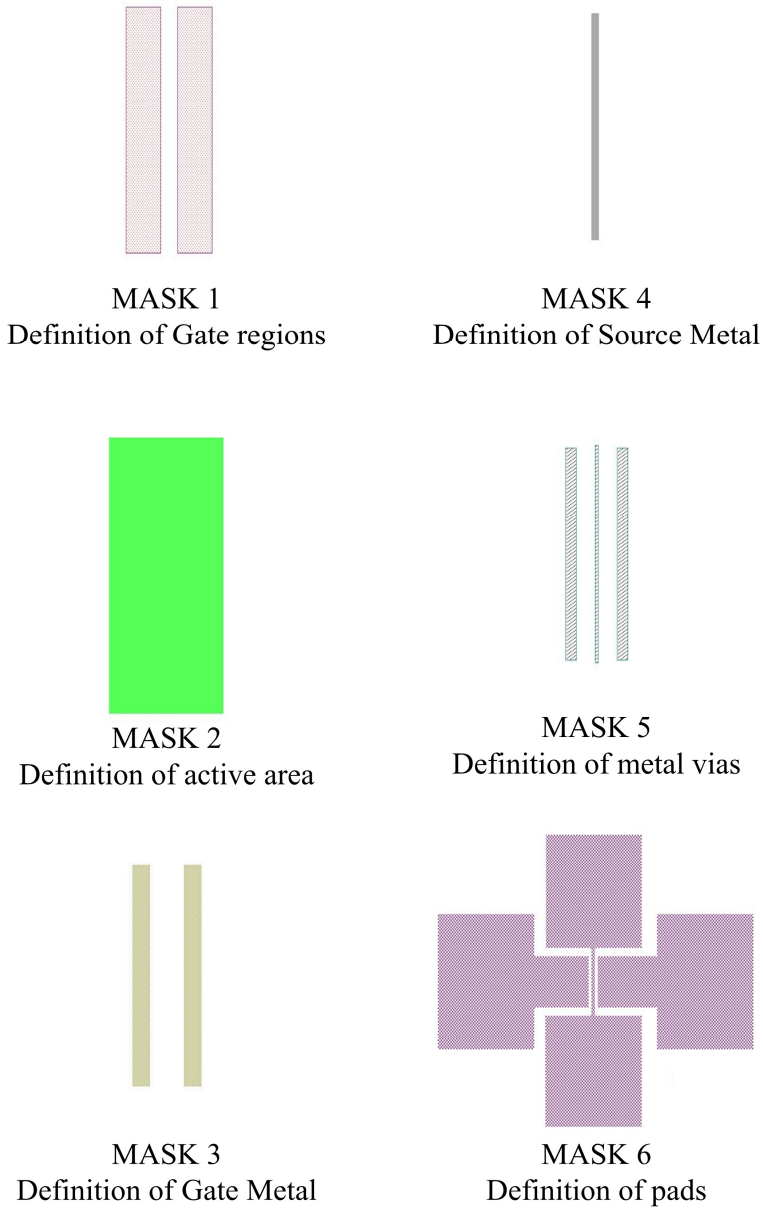

Fig.6.1 The six mask layouts for the lithography process steps.

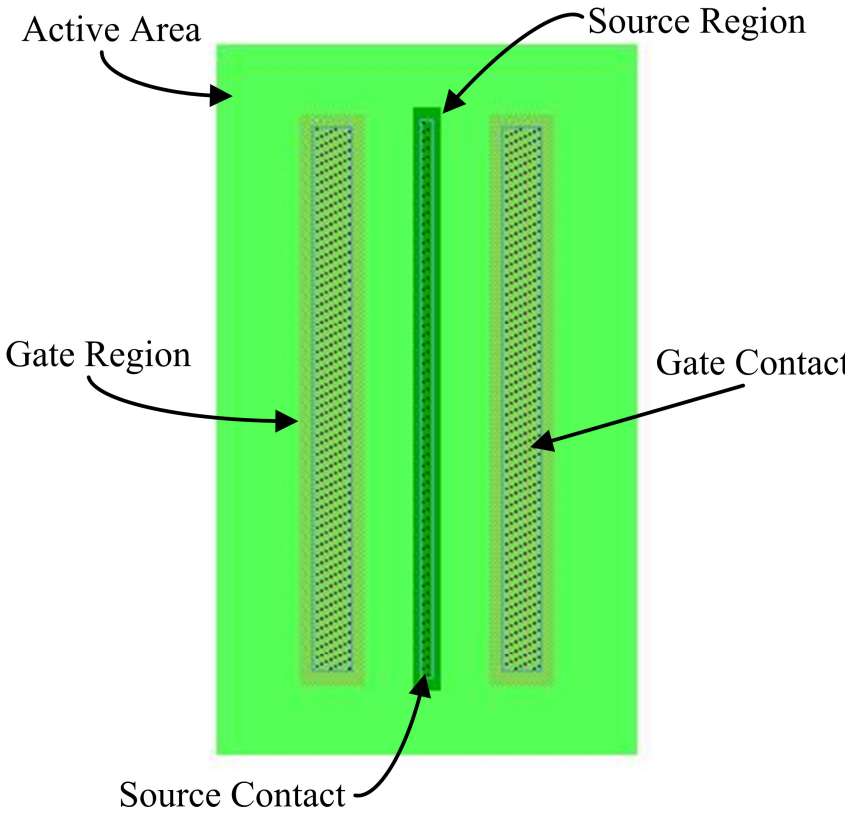

Fig.6.2. Superposition of the first five mask layouts.

Chapter 7

V_2O_5 as Anode of a 4H-SiC Schottky Diode

The first realization of a 4H-SiC Schottky diode, which has a thin layer of V_2O_5 as anode contact, is reported in this chapter. Once the realization process has been shown, the results of *JV* and *CV* measurements are reported and illustrate the typical behavior of a Schottky Barrier Junction (SJB).

7.1 Motivation

4H polytype of Silicon Carbide (4H-SiC) material is very attractive for all those applications where needs to have high power density with low switching power losses and/or to be resistant in harsh environments, i.e. ambient temperature higher than $470°K$, highly ionized radiations, high pressure [93]-[95]. This capability depends on its superior physical properties respect to Silicon as the wide bandgap ($3.2eV$), the high values of thermal conductivity ($3.7 Wcm^{-1}°K^{-1}$), saturation drift velocity ($2 \cdot 10^7 cm/s$) and critical electrical field ($2.2MV/cm$). The availability of very good substrates allowed the development of Schottky Barrier Junction (SBJ) devices as high voltage power diodes [96]-[97], low leakage current rectifier for long life-low power level generators [98] or gas sensors [99], while the blindness to visible and infrared radiations and the robustness of the material suggest the employ of such devices as low noise photodetectors of x-rays and UV radiations without aging effects [100]-[101]. Nevertheless, it is still working a lot on the improvement

of the anode region in terms both of material and of fabrication process. Until now, conventional metals, among which Platinum [102], Gold [103], Nickel [104] and Titanium [105], have been intensively studied obtaining interesting electrical performances compared to Silicon counterpart, but they suffer of some aspects related to the fabrication processes; for example, Au and Pt films interdiffuse into 4H-SiC substrate at temperature around *723°K* making a thermally instable interface [106]-[107] or, in order to have Ni and Ti SBJ diodes with good performance, high temperature annealing (*973÷1173°K*) [108] and accurate surface preparations [109] are needed. Although 4H-SiC technology is compatible with Silicon one, their different chemistry justifies the research of new materials as anode contact of SBJ and, for example, oxides of Iridium or Ruthenium [110], refractory metal borides [111] or transition metals [112] have been proposed, but can require oxidation processes or high temperature annealing, which can affect or be not compatible with the fabrication process of the device or the overall integrated circuit.

In this context, the present work proposes the use of the Transition Metal Oxide (TMO) Divanadium Pentoxide (V_2O_5) as thin interlayer between 4H-SiC and Aluminum (Al) metal contact in order to have a SBJ at the interface with the semiconductor. V_2O_5 and, in general, TMO materials have been proposed in organic electronic device [113]-[115] to form a good ohmic contact, but we are not aware of a their application in 4H-SiC structure. As first realization, the proposed structure is not optimized for a particular application, because our aim is to analyze the transport mechanism underlying its operation by using forward and reverse characteristics at various temperatures as such as capacitance-voltage curves.

7.2 Device Fabrication

A simplified cross-section view of the device structure is in Fig.7.1, where Al and Ni are, respectively, the anode and the cathode contacts of the diode. The substrate is a 4H-SiC n-type <0001> Si-face 4° off-axis ($\rho=0.021\Omega cm$) wafer on which a n-type $5\mu m$-thick epitaxial layer was grown with a doping (N_D) of *8.8*

x10^{15}*±2.2x10*^{15}*cm*$^{-3}$ (CREE, Inc.). The wafer are sequentially cleaned with Acetone and, then, Isopropyl alcohol at *353°K* for *5minutes* and, finally, a bath in HF:H_2O (1:10) for *3minutes* is done. After each cleaning processes, the wafer is rinsed with DI water for *3minutes*. First, V_2O_5 (99.99% powred Sigma-Aldrich) and, then, Al have been deposited by thermal evaporation in an ultra high vacuum chamber without heating the sample. The base vacuum pressure and growth rate of V_2O_5 deposition were *~2x10*$^{-7}$*mbar* and *<0.1nm/s*, respectively. After the depositions, the samples are annealed at *723°K* in a Nitrogen ambient for *10minutes*. The process is completed with the thermal deposition of a Ni film onto the back face of the substrate for the ohmic contact. Al contacts are circular with diameters of *0.5mm* and are concentric with *2mm*-V_2O_5 dots.

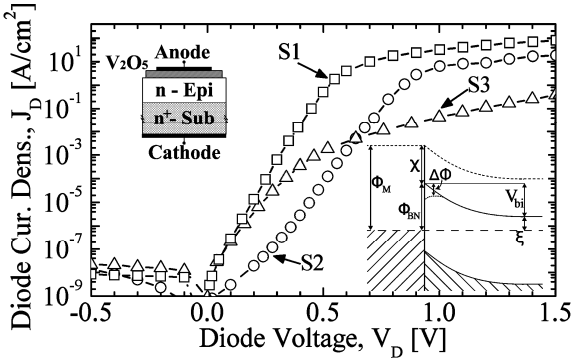

Fig. 7.1. Comparisons of J_D–V_D curves of finite samples (S1), without HF-etch with annealing (S2) as-deposited sample with HF-etch (S3) at *T=298K*. The cross-section of the structure is reported in the insert.

7.3 Results and Discussion

In Fig. 7.1 J_D-V_D curve shows an exponential behavior for over six decades only for *S1* sample, which has been realized from the previous process, while *S2* and *S3* samples evidence separately the beneficial effects of the HF–etch and annealing processes. If the HF–bath is avoided (see *S2*), the current is significantly lower than *S1* and the exponential behavior occurs with two lower different slopes, which confirms the occurrence of defects at the interface according to

[105]. Although it is well known that the wet etch reduces the thickness of the native SiO_2 and, hence, the chance of barrier unevenness [109], the thermal annealing (see *S3*) is absolutely necessary since it favors the intimate contact between 4H-SiC and V_2O_5 with a significant reduction of series resistance, as shown from comparison of *S2* and *S3* curves. By recalling that the annealing temperature was around *700K*, this value is much lower than that used for Ni/4H-SiC in [106], normally occurring in the range *973÷1173K*.

Since the Schottky barriers has been intensively used for the analysis of fundamental properties of semiconductor, numerous models are available to describe their current transport mechanism. By considering the low doping of epilayer, the most frequently used model is described from the following empirical expression [116]:

$$I_D = SR^{**}T^2 e^{-\frac{\Phi_{BN}}{V_T}} \left(e^{\frac{V_D}{V_T n}} - 1 \right) \tag{7.1}$$

where $R^{**}=146Acm^{-2}K^{-2}$ is 4H-SiC effective Richardson constant [103] and n is the ideality factor, while, with the help of the energy band in the insert of Fig. 7.1, $\Phi_{BN} = \Phi_M - \chi - \Delta\Phi$ is the Schottky Barrier Height (SBH), Φ_M and χ are V_2O_5 work function and 4H-SiC electronic affinity, respectively, and $\Delta\Phi$ accounts for the barrier lowering due to the combined effects of the image-force and the static-dipole layer as in [117]:

$$\Delta\Phi = \sqrt{\frac{qE_M}{4\pi\varepsilon_{SiC}}} + \alpha E_M \tag{7.2}$$

In this last $E_M = \sqrt{2qN_D\left(\Phi_{BN} - \xi - V_D - V_T\right)/\varepsilon_{SiC}}$ is the maximum electric field at the interface, α is a constant [117], having dimension of a length, and $\xi = V_T \ln\left(N_C/N_D\right)$ is the distance of Fermi level from the conduction band.

Observing that J_D-V_D curves measured on all the samples have stably the typical behaviour in Fig. 7.2a and 7.2b, Tab. 7.1

summarizes the range of n and Φ_{BN} parameters, extracted from the slope of $ln(J_D)$-V_D and the intercept with the $ln(J_D)$-axis, respectively; in particular, n assumes values between *1.025* and *1.06* and SBH is in the range of *0.78÷0.85eV*. R_{ON} values, which are in the range of $8.6m\Omega cm^2$ and $9.27m\Omega cm^2$ as reported in Tab. 7.1, represent the series resistance of diodes extracted from the insert of Fig. 7.2.a, as follows:

$$R_{ON}\Big|_{J_D=100\,A/cm^2} = \frac{V_{D2} - V_{D1} - nV_T \ln\left(\frac{J_{D2}}{J_{D1}}\right)}{J_{D2} - J_{D1}}$$

where J_{D1} (V_{D1}) and J_{D2} (V_{D2}) are the two current (voltage) values measured around $100A/cm^2$.

	PARAMETERS		VALUES
J_DV_D	Φ_{BN}	*[eV]*	*0.78÷0.85*
	n		*1.025÷1.06*
	$R_{ON@100A/cm2}$	$[m\Omega cm^2]$	*8.6÷9.27*
	α	*[nm]*	*0.96÷1.1*
C_DV_D	$\Phi_{BN}\|_{1kHz}$	*[eV]*	*0.87*
	$N_D\|_{1kHz}$	$[10^{16}cm^{-3}]$	*1.107*
	$\Phi_{BN}\|_{10kHz}$	*[eV]*	*0.9*
	$N_D\|_{10kHz}$	$[10^{16}cm^{-3}]$	*1.104*
	$\Phi_{BN}\|_{100kHz}$	*[eV]*	*0.91*
	$N_D\|_{100kHz}$	$[10^{16}cm^{-3}]$	*1.096*
	$\Phi_{BN}\|_{1MHz}$	*[eV]*	*0.91*
	$N_D\|_{1MHz}$	$[10^{16}cm^{-3}]$	*1.096*
	Φ_{BN}	*[eV]*	*0.89*
	N_D	$[10^{16}cm^{-3}]$	*1.101*

Table 7.1 Parameter values extracted from J_D-V_D and C_D-V_D measurements

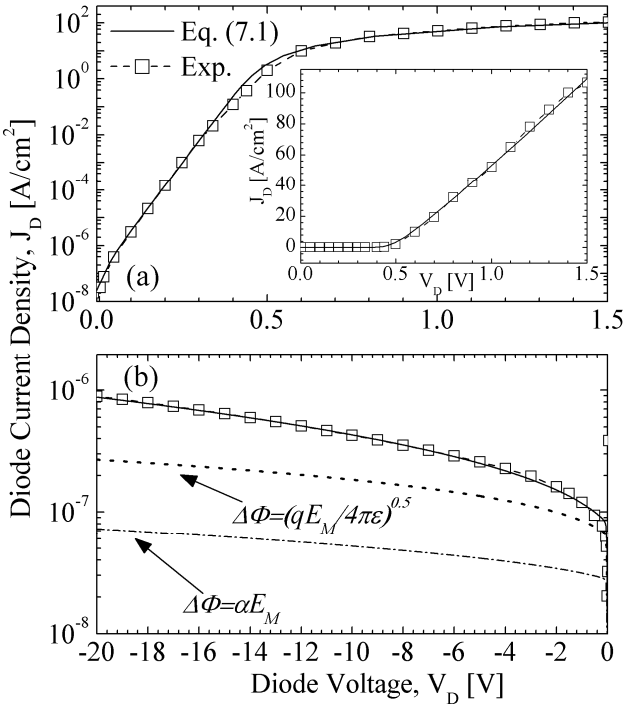

Fig. 7.2. Model and measurements comparison of the forward (a) and reverse (b) J_D–V_D at *T=298K*. The insert in (a) shows the forward J_D-V_D curve using a linear scale.

Whilst barrier lowering mechanisms effects (7.2) used in (7.1) are negligible on the forward curves, they becomes stronger at reverse bias avoiding the expected saturation of reveres current. This is clearly shown in Fig. 7.2b, where, expressing the reverse current as $|J_S| = R^* T^2 \exp(-\Phi_{BN}/V_T)$, the experimental curves are compared with the theoretical curves calculated using separately the two mechanisms in (7.2) and assuming the quantity α in (7.1) as fitting parameter. Though the force-image effect dominates at low voltage, namely for V_D higher than $-6V$, the combination of the two effects is needed to fit the whole characteristic of all the samples, obtaining α values in the range $0.96 \div 1.1nm$. This value does not differ

significantly on that found in [117] for silicide SBJs on Silicon, which have an α between *1.5nm* and *3.5nm* depending on the anode material.

The capacitance $1/C_D^2$ for unit area measured at various reverse voltage and signal frequencies is plotted in Fig. 7.3, since it allows to determine the effective barrier height $\Phi_{BN}-\Delta\Phi$ from the intercept with the V_D-axis and the doping density from the slope, as indicated from the following equation:

$$C_D^{-2} = \frac{2}{qN_D\varepsilon}\left(V_{bi} - V_D\right) \tag{7.4}$$

where $V_{bi} = \left(\Phi_{BN} - \Delta\Phi - \xi - V_T\right)$ is the built-in voltage. Using the lower portion of graphs where $1/C_D^2$ varies linearly with V_D, N_D results $1.1x10^{16}cm^{-3}$, which is in the range of the nominal tolerance given by the manufacture, while from the intercept with the V_D-axis the quantity V_{bi} slightly increases from *0.65eV* at *1kHz* to *0.69eV* at *1MHz*, and using ξ=*190meV*, one obtains a mean Φ_{BN} value of *0.89eV*, which is higher than *90meV* by the average extracted from the forward J_D-V_D curves. By observing all the curves at higher reverse voltages, the slight deviation from the linear behavior can be a consequence of $\Delta\Phi$–dependence on the voltage or of the increase itself of the reverse current with V_D, that makes unreliable the capacitance extraction. In fact, by modeling the reverse current with a voltage-controlled shunt resistance R_S, it is evident that the decrease of R_S with V_D is equivalent to an increase of the effective capacitance $C_{EFF} = C_D + \left(R_S^2\omega^2 C_D\right)^{-1}$. This latter equation explains also $1/C^2_D - V_D$–dependency on the frequency in Fig. 7.3, since they tend to the linear behavior in all V_D range only at the highest frequencies.

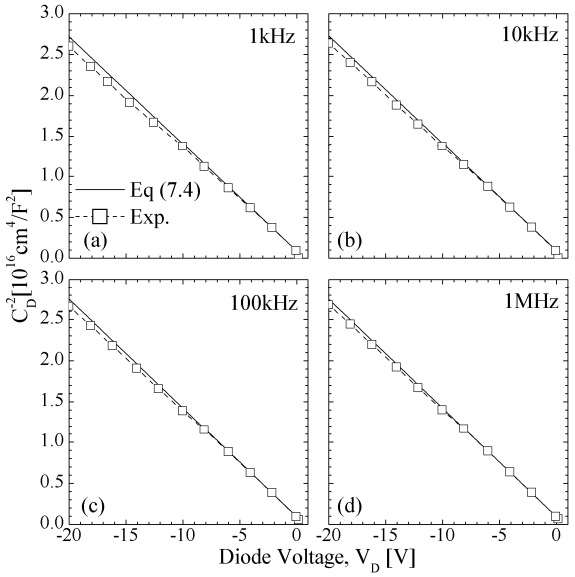

Fig. 7.3. Comparisons between measurements and model results of $C_D^{-2}-V_D$ curves for a signal frequency of (a) *1kHz*, (b) *10kHz*, (c) *100kHz* and (d) *1MHz*. The signal amplitude is *100mV* and *T=298K*.

By considering that $V_2O_5-\Phi_M$ is in the range of *4.7÷5.3eV* [115], [118] and χ is *3.7eV* [16], the expected SBH is between *1eV* and *1.6eV*, which are much higher than our values. Possible explanations of this mismatch could be: *i)* the greater thickness and the longer air-exposition of our V_2O_5 films, since in [115] Φ_M has been found to decrease from *7eV* to *5.2eV* after one hour of air-exposition; *ii)* the no−ideal behavior, since the ideality factor is higher than *1* suggesting the eventual formation of an inhomogeneous barrier [119]. Being inhomogeneities imperfections at the interface among two materials, they induce a SBH spatial fluctuation making no-uniform barrier on the overall surface; therefore, the current flow will have a preferential path through the regions with the lowest SBH, called patches. Such phenomena is characteristic for a real Schottky barrier and has been also used to justify the barrier lowering effect described in (7.2) [120]. Moreover, although it has been discovered before on Si junction, wide band gap or heterojunction Schottky Barrier also manifest it

[121]−[123]. About 4H−SiC, inhomogeneous SBHs have been found for different kind of anode metals, as Ni [121], Ti [124] or Pt [125], and in all cases unexpected Richardson constant and SBH values are extracted.

Recalling Tung's model [119]-[120], SBH fluctuates from the high average value Φ_{BO} of the ideally behaving contact area to lower barrier value $\Phi_{BO}-\Delta$ of surrounding areas and the total current can be seen as a sum of currents through different areas provided the "effective" values of barrier, Φ_{BN}^{EFF}, and contact area, S_{EFF}. In order to quantify Φ_{BO} and Φ_{BN}^{EFF}, a methodological approach has been proposed in [121] and has been used in this analysis. According to it, once evaluated Φ_{BN} and n at different temperatures and plotted $\Phi_{BN}-n$ curve, Φ_{BO} is represented from the asymptotical value of Φ_{BN} as n approaches the unitary value, while Φ_{BN}^{EFF} coincides with the slope of the Arrhenius plot of $ln(I_D/T^2)-1/T$. For our case $\Phi_{BN}-n$ curve is reported in Fig 7.5 for which has been used I_D-V_D curves of Figure 7.4 measured in the range of $100K \div 425K$. Both curves, as well as the abrupt variation of the ideality factor around at $T=150K$, are similar to those observed in [121], where Φ_{BN} increase and n decrease with temperature are used as an indirect proof of the presence of barrier inhomogeneities. As shown in the insert of Figure 7.5, from the asymptotic value [122] at $n\sim1.01$ one obtains $\Phi_{B0}=0.83eV$, while the Φ_{BN}^{EFF} value resulting from the Arrhenius plot of Figure 7.6a is $0.68eV$. It is worth to note that the intercept with the vertical axis gives the constant $R^{**}S$ equal to $1.43x10^{-2}AK^{-2}$, from which R^{**} is $7.28Acm^{-2}K^{-2}$ as is expected. As a further confirmation of the truth of this analysis, by determining the Arrhenius plot from the reverse curves of Figure 7.4b measured at the various temperature for two different voltages, as shown in Figure 7.6b, the resulting values of Φ_{BN}^{EFF} and $R^{**}S$ do not differ from the previous ones.

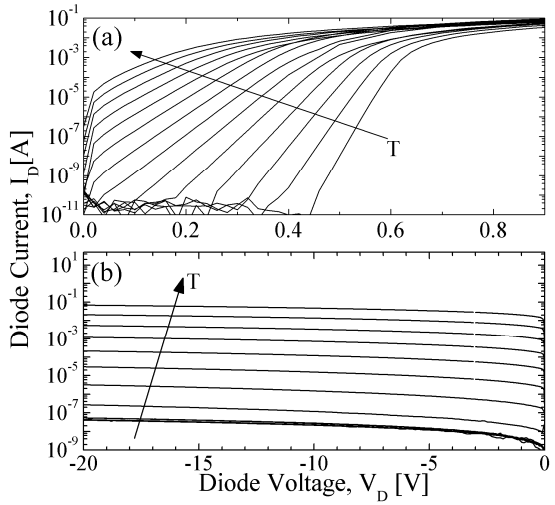

Fig. 7.4. Forward (a) and reverse (b) I_D–V_D curves from *T=100K* to *T=425K*. The step is *25K*.

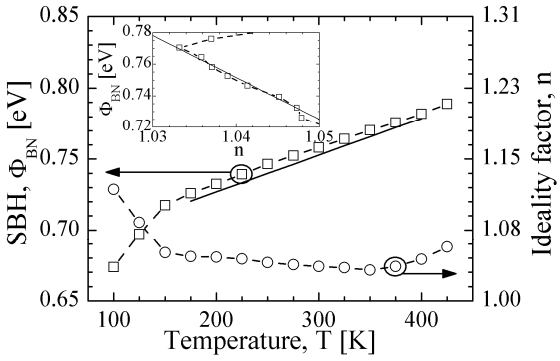

Fig. 7.5. The barrier height (Φ_{BN}) and ideality factor *n* vs. *T*. In the insert Φ_{BN} vs. *n* is plotted.

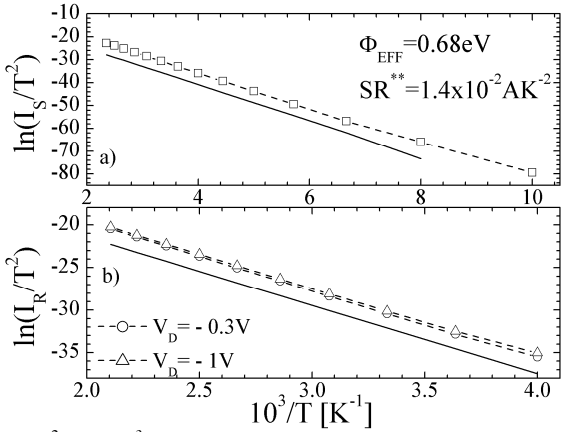

Fig. 7.6. (a) $ln(I_S/T^2)$ vs. $10^3/T$ plot evaluated from the intercept of the forward diode characteristics of Fig. 7.4. (b) $ln(I_R/T^2)$ vs. $10^3/T$ plot evaluated from the diode reverse currents for V_D=$-0.3V$ and $-1V$.

By assuming the contact surface covered by N_{PT} patches, the total diode current is expressed as follows [121]:

$$I_D = N_{PT} S_{EFF} R^{**} T^2 e^{-\frac{\Phi_{BN}}{V_T}} \left(e^{\frac{V_D}{V_T}} - 1 \right) \tag{7.5}$$

where N_{PT} represents the total number of low barrier patches with the effective area S_{EFF}:

$$S_{EFF} = \frac{4\pi\varepsilon}{9kN_D T} \frac{\Phi_{B0} - \Phi_{BN}^{EFF}}{V_{bi}} \tag{7.6}$$

Using Φ_{B0}=$0.83eV$ and Φ_{BN}^{EFF} =$0.68eV$ in (7.6), this gives at room temperature S_{EFF}=$4.13x10^{-12}cm^2$ and, using (7.5) for fitting the curves in Fig. 7. 4, one obtains N_{PT}=$2.6x10^7$, which corresponds to patch area $N_{PT}S_{EFF}$ equal approximately to five percents of the total area. Note that, being S_{EFF} inversely proportional to the temperature, the lower is the temperature, larger is the patch area and, hence, the ideality factor. Contrarily with the low R^{**} value of $7.28Acm^{-2}K^{-2}$ previously

claimed, reporting $ln(I_D/N_{PT}/S_{EFF}/T^2)-1/T$ curve in the Arrhenius plot, Richardson's constant results $145.9Acm^{-2}K^{-2}$, which is very close to the theoretical one.

Despite the reduced contact area invested from conduction, its percentage is higher than $1\div2\%$ value observed on Ni_2Si/4H−SiC [121] or than 3% of Ge/4H-SiC [123] Schottky diodes, indicating a more uniform barrier. Taking in account that the necessarily lower Φ_{BN} value given from $1/C_D^2$ measurements because of low inhomogeneous barriers [119], the reduced difference of Φ_{B0} ($0.83eV$) from Φ_{BN}^{CV} ($0.89eV$) is a further proof of the greater uniformity of our samples, compared to the difference of $140meV$ found in [123].

Finally, a comparison of Schottky diodes realized with different anode metals [112] is reported in Figure 7.7. The quality of V_2O_5 junctions is comparable with that achieved by Ni contacts, for which high temperatures annealing processes are needed, and IrO_2 contacts, having this latter a R_{ON} twice higher. Although Ni and IrO_2 SBH values of $1.63eV$ and $1.64eV$, respectively, correspond to a very low reverse leakage current, predicting a good behavior at high temperatures, they cause too high conduction power losses, which are prohibitive at low switching frequency; in fact, ideal values between $1eV$ and $1.3eV$ have been calculated in order to compensate those effects [126].

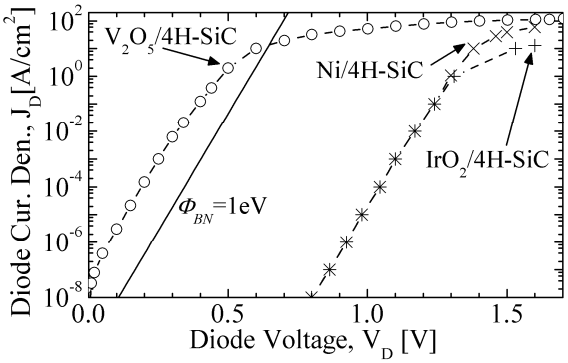

Fig. 7.7. Comparisons of J_D-V_D curves among V_2O_5/4H-SiC, IrO_2/4H-SiC, Ni/4H-SiC and ideal ($\Phi_{BN}=1eV$) SBJs.

Conclusions

The research activity concerns the design and modelling of 4H-SiC normally-off Bipolar Mode Field Effect Transistor. The device structure is a vertical trench to whose base *p*-type regions are realized by ion-implantation. Space charge regions of gate-channel *p-n* junctions overlap inducing a potential barrier which opposes to the electron flow from source to drain during the off-state, while by forward biasing gate-source junctions the potential barrier height decreases, up to disappear, and the hole injection from gate to channel effects a channel conductivity modulation. From the analysis of the static and dynamic electrical characteristics, three main physic mechanisms are highlighted and regard the dependency of the potential barrier on the physical and geometric parameters, the extraction of the hole during the switching-off and the hole injection efficiency of the *p*-type regions; each phenomena is deeply treated in each Chapter.

In the first chapters an original analytical model of the potential barrier is proposed and has been obtained by solving Poisson's equation considering both the minority carriers and the electric fields to the corners and to source. Comparisons with numerical simulations reveal the accuracy of the model to describe the potential barrier height for any value of the physic and geometrical parameters, as channel doping and width, and any gate and drain bias conditions. Analyzing these results, a doping-independent potential barrier is achievable for channel doping lower than $10^{15} cm^{-3}$, for a fixed channel width and depth. Moreover, it has been shown that a lower potential barrier height is formed when gate and source regions are very close due to the electric field of the high-low junction at source.

By starting from this model, J_D dependency on V_{GS} has been modelled and comparisons with experimental measurements as well as

device simulation are reported. Two regions are typically defined: the former is at low gate voltage and an exponential behaviour of J_D is shown due to the presence of the potential barrier; the second starts once the barrier disappears and ohmic behaviour is due to the electron current which flows through the neutral portion of the channel. The proposed model expresses in an original and compact form these two behaviours and is able to describe, for example, the slope of J_D, which has a complex dependence on the channel parameters and on the electric bias conditions, and, further, to evaluate the threshold voltage, which defines the beginning of the unipolar region. In this way, since physical and geometric channel parameters are correlated to the electrical quantities, the model can be an useful instrument to properly design the channel of devices as BMFET or with similar structure as VJFET and SIT.

As all bipolar devices, the turning-off of BMFET is mainly dominates by the extraction of the hole carriers from channel through gates and in Chapter 4, from the analysis of the input diode, an original model of the switching-off behaviour of a *p-i-n* diode is developed. In addition to current and voltage transients, it is able to describe the temporal-spatial distributions of the electric fields, of the hole carriers and of the current densities in the intrinsic region. Moreover, being relevant for 4H-SiC the partial doping and the band−gap narrowing effects, the asymmetric high-low junctions at the extremities of the base region are separately introduced as boundary conditions. Numerical simulation and experimental measurements show the accuracy of the model both for 4H-SiC and for Si also by changing physical and geometrical parameters, as carrier life-time and low-doped region width. Together with a static model, it is an useful instrument able to design and to understand which process-dependent physical quantities influences device performances.

Chapter 5 reports the effects of the incomplete ionization and of the band-gap narrowing on the gate doping levels, which is relevant in terms of input resistance, current gain and blocking voltage. Different implanted doses and thermal annealing procedures have been considered and the extracted Aluminium concentrations have been used to evaluate the hole injection in the base region of a *p-i-n* diode. It is shown that for a fixed device structure the ionized acceptor

concentration value, that maximizes the hole injection and the forward current, has been found in the range of $5 \cdot 10^{18} cm^{-3}$ and $5 \cdot 10^{19} cm^{-3}$ corresponding to the implanted concentration of about $2 \cdot 10^{20} cm^{-3}$ with a post implantation annealing temperature as high as *1950°C*.

Finally, in Chapter 6 the main process steps and mask layouts are described and in Chapter 7 an original Schottky diode is proposed whose aim is to be integrated as a free-wheeling diode. V_2O_5 thin layers have been deposited on 4H-SiC epilayer by thermal deposition and covered with Al metal contact. In order to realize a Schottky diode, both HF−surface cleaning before the deposition and thermal annealing at *723K* are needed. From the analysis of J_D-V_D and C_D-V_D characteristics, a barrier height between *0.77* and *0.85eV*, an ideality factor between *1.025* and *1.06* and a series resistance of $9 m\Omega cm^2$ have been extracted and the diode shows a stable behaviour up to *425K*. Moreover, as all Schottky barrier junction, inhomogeneity appear which are due to spatial fluctuations of the potential barrier height. By using Tung's model, the extracted parameters are the homogeneous potential barrier equal to *0.83eV* and the effective area equal to $10^{-4} cm^2$, whose percentage respect to the total area (*5%*) is one of the higher found in literature among the numerous materials used as anode contact for 4H-SiC Schottky diode.

APPENDIX A

In the following the main physical models and the related carrier transport parameters of 4H-SiC are reported.

A.1 Carrier Statistics

The band gap amplitude varies with the following quadratic law, in the temperature range 0÷800°K [1], [127]:

$$E_g(T) = 3.265 - 6.45\times10^{-4}\times\frac{T^2}{T+1300}$$

and, for $T>T_0=300°K$, it can be approximated to:

$$E_g(T) = E_G^{300°K} - E_G^{\alpha}\times(T-T_0) \tag{A.1}$$

The intrinsic concentration is evaluated as follows:

$$n_i(T) = \sqrt{N_C(T)N_V(T)}\; e^{-\frac{E_g(T)}{2kT}} \tag{A.2}$$

where

$$\begin{aligned} N_C(T) &= 2M_c\left(\frac{2\pi m_e^* kT}{h^2}\right)^{\frac{3}{2}} = N_C(T_O)\left(\frac{T}{T_O}\right)^{\frac{3}{2}} \\ N_V(T) &= 2\left(\frac{2\pi m_h^* kT}{h^2}\right)^{\frac{3}{2}} = N_V(T_O)\left(\frac{T}{T_O}\right)^{\frac{3}{2}} \end{aligned} \tag{A.3}$$

are the effective density of states in conduction and valence bands, respectively, $m_e^* = 0.77m_0$ [128] and $m_h^* = 1.2m_0$ [129] are the electron and hole effective masses (where m_o is the electron rest mass) and M_C=3 represents the equivalent valleys in conduction band for 4H-SiC.

Finally, the electron affinity, χ, and the relative dielectric constant, ε_R, are, respectively, *3.7eV* and *9.66* [16].

A.2 Band-gap Narrowing Effects

Due to the heavy doping, the formation of energy bands close to the edges of conduction or valence bands induces an apparent reduction of the band-gap, whose effect is to increase the intrinsic concentration as $n_{ie} = n_i \exp\left(\Delta E_G k^{-1} T^{-1}\right)$. 4H-SiC band gap narrowing is described by Lindefelt model [89]:

$$\begin{aligned}\Delta E_{gd} &= 1.7x10^{-2}\sqrt{\frac{N_D^+}{10^{18}}} + 1.9x10^{-2}\left(\frac{N_D^+}{10^{18}}\right)^{\frac{1}{4}} + 1.5x10^{-2}\left(\frac{N_D^+}{10^{18}}\right)^{\frac{1}{3}} \\ \Delta E_{ga} &= 1.54x10^{-2}\sqrt{\frac{N_A^-}{10^{18}}} + 1.3x10^{-2}\left(\frac{N_A^-}{10^{18}}\right)^{\frac{1}{3}} + 1.57x10^{-2}\left(\frac{N_A^-}{10^{18}}\right)^{\frac{1}{3}}\end{aligned} \quad \text{(A.4)}$$

A.3 Incomplete Ionization

At room temperature 4H-SiC is affected by the freeze-out phenomena due to the distance between the energy levels of the impurity concentration and of the relative band edge. In fact, the dopant activation energy of Aluminum (acceptor), ΔE_a, and of the Phosphorous (donor), ΔE_d, are, respectively, *200±20meV* [130] and *70±5meV* [131]. For an acceptor atom, the activated concentration is:

$$N_A^+ = N_A\left[1 + g_a e^{\frac{E_a - E_{Fp}}{kT}}\right]^{-1}$$

where g_a is the degeneracy factor of valence band, and the ionization rate, ξ_a, is:

$$\xi_A = \frac{N_A^-}{N_A} = \frac{\sqrt{1+4g_a \frac{N_A}{N_V(T)} e^{\frac{\Delta E_a}{kT}}} - 1}{2g_a \frac{N_A}{N_V(T)} e^{\frac{\Delta E_a}{kT}}} \quad \text{(A.5).}$$

A.4 Carrier Recombination Mechanism

4H-SiC recombination processes are mainly two: Auger and Shockley-Read-Hall (SRH) processes. The effective lifetime is given by the superposition of the effects as:

$$\tau_{EFF} = \tau_{SRH} \left|\right| \tau_{Auger}$$

Auger recombination is significant only at high injection levels in which the Auger life-time follows the law:

$$\tau_{Auger} = \frac{1}{\left(C_n + C_p\right)\Delta^2} \quad \text{(A.6)}$$

where Δ represents the excess carriers density, $C_n = 5\times10^{-31} cm^6 s^{-1}$ and $C_p = 2\times10^{-31} cm^6 s^{-1}$ are the Auger coefficients [132]. The trap-assisted SRH recombination lifetime is described by the semi-empirical formula [133]:

$$\tau_{n,p}^{SRH} = \frac{\tau_{n0,p0}}{1+\frac{N}{N_{n,p}^{SRH}}} \quad \text{(A.7)}$$

where $\tau_{n0(p0)}$ are the lifetime coefficient value depending by the process, N is the total impurity concentration and $N_{n,p}^{SRH} = 5\times10^{16} cm^{-3}$ is a fitting coefficient.

A.5 Mobility Models

Mobility parameter is a quantity that summarizes different scattering processes, as lattice vibration, carrier-carrier and carrier-impurity ions interactions, bulk and surface imperfections. For 4H-SiC semiconductor two mobility models have been considered, depending on the electrical field.

A.5.1. Low Field Mobility Model

For low field mobility, the phenomenological model of Caughey and Thomas [134], including the temperature dependence for T > 300°K:

$$\mu_{n(p)}^{low}(T,N) = \mu_{0n(p)}^{\min}\left(\frac{T}{300}\right)^{\alpha_{n(p)}} + \frac{\mu_{0n(p)}^{\max}\left(\frac{T}{300}\right)^{\beta_{n(p)}} - \mu_{0n(p)}^{\min}\left(\frac{T}{300}\right)^{\alpha_{n(p)}}}{1+\left(\frac{N}{N_{n(p)}^{crit}}\right)^{\delta_{n(p)}}\left(\frac{T}{300}\right)^{\gamma_{n(p)}}} \tag{A.7}$$

The parameter values are from [135] for electron mobility, while for holes one they are obtained by fitting (A.7) with the experimental measurements at ambient temperature from [136] and at different temperatures from [137].

A.5.2. High Field Mobility Model

At high electric field, the mobility is not anymore field-independent and the mobility changes as follows [135]:

$$\mu_{n(p)} = \frac{\mu_{n(p)}^{low}}{\left[1+\left(\frac{\mu_{n(p)}^{low} E}{v_{sat}}\right)^{\beta}\right]^{\frac{1}{\beta}}} \tag{A.8}$$

where v_{sat} and β vary with the temperature as:

$$\begin{cases} v_{sat} = \dfrac{v_{\max}}{1+0.6\ e^{\frac{T}{600}}} \\ \beta = \beta_o + a\ e^{\frac{T-T_{ref}}{b}} \end{cases}$$

whose parameter values are reported in Table [135]. All available measured data refer to electron current flows perpendicular to the *c*−axis, while, because no measured data for holes are presently available, hole velocity is considered even to half than electron one, being generally less in all semiconductors.

A.6 Impact Ionization

Under large electric field, the energy acquired by a carrier can be so high that, by colliding with another carrier, it can generate an electron-hole pair. The generation rate depends on the impact ionization coefficients, *IMP*, and a higher *IMP* means a higher generation rate. The empirical relationships of *IMP* is as follows [138]:

$$IMP_{n,p} = c_{n,p} e^{-d_{n,p}/E}$$

where $c_{n,p}$ and $d_{n,p}$ are the impact ionization parameters which for 4H-SiC are $c_n=4.075\cdot10^5 cm^{-1}$, $c_p=1.63\cdot10^7 cm^{-1}$, $d_n=1.67\cdot10^7 Vcm^{-1}$ and $d_p=1.67\cdot10^7 Vcm^{-1}$ [139].

	PARAMETERS	UNITS	VALUES
PHYSICS	ε_R		9.66
	X	[eV]	3.7
	$E_G^{300°K}$	[eV]	3.23
	E_G^{α}	[eV/K]	3.3×10^{-4}
	$N_{C,V}^{300°K}$	$[cm^{-3}]$	1.66×10^{19}, 3.29×10^{19}
BAND-GAP NARROWING	ΔE_{gd}	[eV]	see (A.4)
	ΔE_{ga}	[eV]	see (A.4)
FREEZE-OUT	$\Delta E_{a,d}$	[eV]	19×10^{-2}, 7×10^{-2}
	$g_{a,d}$		4,2
LIFETIME	$N_{n,p}^{REF}$	$[cm^{-3}]$	5×10^{16}
MOBILITY	$\mu_{0n,p}^{MAX}$	$[cm^2V^{-1}s^{-1}]$	950,125
	$\mu_{0n,p}^{min}$	$[cm^2V^{-1}s^{-1}]$	40,15.9
	$N_{n,p}^{crit}$	$[cm^{-3}]$	2×10^{17}, 1.76×10^{19}
	$\alpha_{n,p}$		-0.5
	$\beta_{n,p}$		-2.4,-2.15
	$\gamma_{n,p}$		-0.76,-0.34
	$\delta_{n,p}$		0.76,0.34
FIELD DEPENDENT MOBILITY	$v_{MAXn,p}$	$[cm\ s^{-1}]$	4.77×10^7, 2.66×10^7
	β_o		0.816
	T_{ref}	[K]	327
	a		4.27×10^{-2}
	b	[K]	98.4
IMPACT IONIZATION	$c_{n,p}$	$[cm^{-1}]$	4.075×10^5, 1.63×10^7
	$d_{n,p}$	$[Vcm^{-1}]$	1.67×10^7, 1.67×10^7

Table A.1 4H-SiC physical parameters used in the simulations.

APPENDIX B

SYMBOLS	
A_D	Diode area [cm^2]
D_a	Ambipolar diffusion coefficient [cm^2s^{-1}]
$D_{n(p)}$	Electron (hole) diffusion coefficient into the base [cm^2s^{-1}]
$D_{nA(pC)}$	Electron (hole) dif. coef. into the anode (cathode) [cm^2s^{-1}]
E	Electric field [Vcm^{-1}]
E_C	Critical electric field [Vcm^{-1}]
E_G	Band-gap [eV]
h_{FE}	Common source (emitter) current gain
J_B	Rec. current density into the neutral base region [Acm^{-2}]
J_D	Drain current density [Acm^{-2}]
J_{Diode}	Diode total current density [Acm^{-2}]
$J_{F(R)}$	Forward (reverse) total current density [Acm^{-2}]
J_G	Gate density [Acm^{-2}]
$J_{n(p)}$	Electron (hole) current density [Acm^{-2}]
$J_{nA(pC)}$	Electron (hole) cur. dens. injected in the anode (cathode) [Acm^{-2}]
J_{SC}	Rec. current density in the p^+-n depletion layer [Acm^{-2}]
k	Boltzmann constant [eVK^{-1}]
L_a	Ambipolar diffusion length in the base [cm]
L_d	Debye length [cm]
n	Electron concentration [cm^{-3}]
$N_{a(d)}$	Acceptor (donor) density [cm^{-3}]
$N_a^-(N_d^+)$	Ionized donor (acceptor) density [cm^{-3}]
$N_{A(B)(C)}$	Doping density of anode (base) (cathode) [cm^{-3}]
N_{eff}	Effective doping [cm^{-3}]
N_{EPI}	Epilayer density [cm^{-3}]
n_i	Intrinsic carrier concentration [cm^{-3}]
$N_{n,p}^{REF}$	Reference density in the carrier lifetime expression [cm^{-3}]
p	Hole concentration [cm^{-3}]
$p_{F0(FW)(T0)}$	Non-homogenous solution of the continuity equation [cm^{-3}]
p_{MAX}	Peak of hole concentration [cm^{-3}]
p_S	Homogenous solution of the continuity equation [cm^{-3}]
p_{SP}	Hole density at the saddle point [cm^{-3}]
q	Electron charge [A s]

$R_A(R_C)$	Specific resistance of anode (cathode) [Ωcm^2]
R_B	Specific resistance of base [Ωcm^2]
R_{EXT}	External specific resistance [Ωcm^2]
$R_{n+(p+)}$	Contact resistance of $n(p)$-type region [Ωcm^2]
R_{ON}	Specific ON-state resistance [Ωcm^2]
R_S	Specific parasitic resistance [Ωcm^2]
S_A (S_C)	Effective recombination velocity of anode (cathode) [cms^{-1}]
T	Temperature [K]
t_S	Storage interval [s]
$U_{n(p)}$	Electron (hole) recombination rate [$s^{-1}cm^{-3}$]
V_{bi}	Built-in voltage of the p^+-n junction [V]
V_{bl}	Blocking voltage [V]
V_D	Total diode voltage [V]
V_{DIF}	Sum of Dember voltage and the voltage across the n-n^+ junction of p-i-n diode [V]
V_{DS}	Drain-source voltage [V]
V_{EXT}	Power supply [V]
$V_{G/CH}$	Gate-channel potential drop [V]
V_{GS}	Gate-source voltage [V]
V_{OHM}	Ohmic voltage [V]
V_{pn}	Applied voltage across the p^+-n junction [V]
V_{n+n}	Potential drop at the n^+-n junction [V]
v_{SAT}	Saturation velocity [cm s^{-1}]
$V_{S/CH}$	Source-channel potential barrier [V]
V_T	Thermal voltage [V]
$V_{I(II)(III)}$	Potential drop in Zone I (II) (III) [V]
W^*	Maximum width of Zone II [cm]
W_A	Anode width [cm]
W_B	Base width [cm]
W_C	Cathode width [cm]
W_{SC}	p^+-n depletion layer width [cm]
X_{CH}	Channel width [cm]
Y_{CH}	Channel depth [cm]
Y_D	Drain depth [cm]
Y_{EPI}	Epilayer depth [cm]
Y_G	Gate junction depth [cm]
Y_R	Gate-source distance [cm]
Y_S	Source depth [cm]
Z	Length [cm]
ΔE_g	Effective bandgap narrowing[eV]
ε_R	Relative dielectric constant [Fcm^{-1}]

λ	Thermal conductivity [$Wcm^{-1}K^{-1}$]
$\mu_{n,p}$	Electron (hole) mobility [$cm^2V^{-1}s^{-1}$]
τ_a	Ambipolar lifetime in the base [s]
$\tau_{n(p)}$	Electron (hole) lifetime of base [s]
$\tau_{nA(pC)}$	Electron (hole) lifetime of anode (cathode) [s]
$\tau_{0n(0p)}$	Electron (hole) lifetime coefficient [s]
χ	Electron affinity [eV]

APPENDIX C

The static model of *p-i-n* consider the diode current density as follows:

$$J_D^0 = J_{SCR}^0 + J_B^0 + J_{pC}^0 + J_{nA}^0 = J_{SCR}^0 + J_{DIF}^0 \tag{C.1}$$

where the terms on r.h.s represent, respectively, the recombination in the space charge region and in the neutral base and the minority currents injected in the cathode and the anode and they can be expressed in terms of $p^0(0^+)$ according to the following expressions:

$$J_{SC}^0 = q\frac{W_{SC}^0 n_i}{2\sqrt{\tau_p \tau_n}}\left(e^{\frac{V_{pn}^0}{2V_T}} - 1\right) \tag{C.2}$$

$$J_B^0 = q\frac{L_a^0}{\tau_a^0}\frac{\left(\cosh\left(\frac{W_B}{L_a^0}\right) - 1\right)}{\sinh\left(\frac{W_B}{L_a^0}\right)}\left(p^0\left(0^+\right) + p^0\left(W_B\right)\right) \tag{C.3}$$

$$J_{pC}^0 = qS_C p^0\left(W_B\right)\left(1 + \frac{p^0\left(W_B\right)}{N_B}\right) \tag{C.4}$$

$$J_{nA}^0 = qS_A p^0\left(0^+\right)\left(1 + \frac{p^0\left(0^+\right)}{N_B}\right) \tag{C.5}$$

and $S_C = \sqrt{\frac{D_{pC}}{\tau_{pC}}} \frac{N_B}{N_{dC}} e^{\frac{\Delta E_{gC}}{kT}} \coth\left(\frac{W_C}{L_{pC}}\right), S_A = \sqrt{\frac{D_{nA}}{\tau_{nA}}} \frac{N_B}{N_{aA}} e^{\frac{\Delta E_{gA}}{kT}} \coth\left(\frac{W_A}{L_{nA}}\right)$ the effective recombination velocities; it is relevant to note that L_a^0 is $p^0(0^+)$-dependent ambipolar length and the carrier density $p^0(W_B)$ is calculated as a function of the independent variable $p^0(0^+)$ through a third-order polynomial [140]. Likewise, the diode voltage V_D^0 can be expressed as sum of the various voltage components:

$$V_D^0 = V_{pn}^0 + V_{DIF}^0 + V_{OHM}^0 \tag{C.6}$$

where V_{pn}^0 is the voltage across the p^+-n junction, V_{DIF}^0 is the sum of the Dember voltage and that across the n-n^+ junction and V_{OHM}^0 accounts for the ohmic voltage in the base and terminal regions. As shown in [140], the terms of (C.6) can be rewritten as:

$$V_{pn}^0 = V_T \ln\left(\frac{p^0(0^+)N_B}{n_i^2}\right) \tag{C.7}$$

$$V_{DIF}^0 = V_T \ln\left[\left(\frac{p^0(0^+) + \frac{D_n N_B}{D_n + D_p}}{p^0(W_B) + \frac{D_n N_B}{D_n + D_p}}\right)^{\frac{D_n - D_p}{D_n + D_p}} \left(1 + \frac{p^0(W_B)}{N_B}\right)\right] \tag{C.8}$$

$$V_{OHM}^0 = J_D^0 \left(R_C + R_A + R_B + R_S\right) = J_D^0 R_D^0 \tag{C.9}$$

where $R_{C(A)} = W_{C(A)} \Big/ \left(q\mu_{n^+(p^+)} N_{dC(aA)}\right)$ and R_B represent the specific resistance of the terminal regions and the modulated base, respectively, and, finally, R_S accounts for the parasitic contribution, which is normally set equal zero if not otherwise specified.

Finally, the hole carrier distribution is reported as follows:

$$p^0(x) = \frac{p^0(W_B)\sinh\left(\frac{x}{L_a^0}\right) - p^0(0^+)\sinh\left(\frac{x-W_B}{L_a^0}\right)}{\sinh\left(\frac{W_B}{L_a^0}\right)}$$

APPENDIX D

In this APPENDIX the evaluation of the homogeneous solution coefficients is proposed.

D.1 Eigen Values Calculation

In order to evaluate the eigen values, the constancy of the total current density along the base is assumed as boundary condition. So, by the equality of the recombination rates and because the differences of the carriers concentrations along the base are negligible, the sum of electron and hole continuity equations can be written, as follows:

$$(D_p - D_n)\frac{\partial^2 p_S}{\partial x^2} = (\mu_p + \mu_n)\frac{\partial p_S}{\partial x} \tag{D.1}$$

where the electron and hole current densities are expressed in terms of the diffusion and drift components and $D_{n,p}$ and $\mu_{n,p}$ are assumed spatially constant. Because (D.1) is valid at $x=0^+$ and $x=W_B$, it is possible writing the following equivalence by using (4.8):

$$\frac{\left.\frac{\partial^2 p_S}{\partial x^2}\right|_{x=0^+}}{\left.\frac{\partial^2 p_S}{\partial x^2}\right|_{x=W_B}} = \frac{\left.\frac{\partial p_S}{\partial x}\right|_{x=0^+}}{\left.\frac{\partial p_S}{\partial x}\right|_{x=W_B}} \rightarrow \frac{B}{C} = \frac{B\cos\left(\frac{k}{\sqrt{D_a}}W_B\right) + C\sin\left(\frac{k}{\sqrt{D_a}}W_B\right)}{-B\sin\left(\frac{k}{\sqrt{D_a}}W_B\right) + C\cos\left(\frac{k}{\sqrt{D_a}}W_B\right)} \tag{D.2}$$

Since $B \neq C$, (D.2) is verified only if $\cos\left(kW_B/\sqrt{D_a}\right) = 1$ and $\sin\left(kW_B/\sqrt{D_a}\right) = 0$, which implies $k_n = n\pi\sqrt{D_a}/W_B$ with $n \in \mathbb{N}$.

D.2 B_n and C_n Calculation

The model uses as initial condition the variation of the recombination current density, resulting in an original solution of the hole homogeneous solution; in fact, other models use the steady-state hole concentration as initial condition.

Using (C.10) for evaluating the variation of the recombination current under stationary conditions:

$$\Delta J_P^0(x) = J_P^0(x) - J_P^0(W_B) = q\int_x^{W_B} \frac{p^0(x)}{\tau_a}\,dx$$

this last can be expanded into Fourier-series and compared, term by term, with the corresponding spatial variation calculated at $t=0^+$ from the continuity equation of the homogeneous solution:

$$\Delta J_P^0(x,0^+) = J_P(x,0^+) - J_P(W_B,0^+) = q\int_x^{W_B} \frac{\partial p_S(x,0^+)}{\partial t} + \frac{\partial p_S(x,0^+)}{\tau_a}\,dx$$

with $p_S(x,0^+)$ expressed from (4.8). From this comparison, the coefficients B_n and C_n can be written as:

$$B_n = \frac{W_B}{L_{AMB}(n\pi)^2}\frac{p^0(0^+) - p^0(W_B)\cosh\left(\frac{W_B}{L_{AMB}}\right)}{\sinh\left(\frac{W_B}{L_{AMB}}\right)}\left[(-1)^n - 1\right] +$$

$$+\frac{L_{AMB}}{W_B\left[1+\left(\frac{L_{AMB}n\pi}{W_B}\right)^2\right]}\left\{\frac{p^0(W_B)\left[\cosh\left(\frac{W_B}{L_{AMB}}\right)(-1)^n - 1\right] + p^0(0^+)\left[\cosh\left(\frac{W_B}{L_{AMB}}\right) - (-1)^n\right]}{\sinh\left(\frac{W_B}{L_{AMB}}\right)}\right\}$$

$$C_n = \frac{p^0\left(0^+\right)}{n\pi}\left[\frac{\cosh\left(\frac{W_B}{L_{AMB}}\right)(-1)^n - 1}{1+\left(\frac{L_{AMB}n\pi}{W_B}\right)^2}\right] + \frac{(-1)^n}{n\pi}\frac{p^0\left(W_B\right) - p^0\left(0^+\right)\cosh\left(\frac{W_B}{L_{AMB}}\right)}{1+\left(\frac{L_{AMB}n\pi}{W_B}\right)^2}$$

D.3 A_0 and A_1 Calculation

By assuming the equality of hole concentrations at $x=0^+$ and $x=W^-_B$ as initial conditions, the coefficients of the linear term of $p_S(x,t)$ are as follows:

$$A_0 = p^0\left(0^+\right) - \sum_{n=1}^{\infty} B_n$$

$$A_1 = \frac{p^0\left(W_B\right) - A_0 - \sum_{n=1}^{\infty} B_n(-1)^i}{W_B}$$

APPENDIX E

The temporal function of the closed-form of W_{SCR} in (4.27) is:

$$H(t)=\frac{\sqrt{|h_1|}W_{SC}(t_S)-1}{\sqrt{|h_1|}W_{SC}(t_S)+1}\left[\frac{\left(\frac{e^{\frac{t-t_S}{\tau_a}}+h_4}{1+h_4}\right)^{(h_3-h_4)}}{\left(\frac{e^{\frac{t-t_S}{\tau_a}}+h_5}{1+h_5}\right)^{(h_3-h_5)}}\right]^{\frac{2\sqrt{|h_1|}h_2}{h_5-h_4}\tau_a} \tag{E.1}$$

where the various coefficients are:

$$h_1=\frac{qN_B}{2\varepsilon}\frac{1}{V_{EXT}-V_{bi}+2V_T},\qquad h_2=\frac{\left(V_{EXT}-V_{bi}+2V_T\right)\mu_n}{W_B+q\mu_nN_B(R_{EXT}+R_C+R_A)},$$

$$h_3=\frac{\left(\mu_p+\mu_n\right)p_{MAX}(t_S)}{\mu_nN_B},\qquad h_4=\frac{p_{MAX}(t_S)}{N_B},$$

$$h_5=\frac{q\left(\mu_n+\mu_p\right)p_{MAX}(t_S)\left(R_{EXT}+R_C+R_A\right)}{W_B+q\mu_nN_B\left(R_{EXT}+R_C+R_A\right)}.$$

Related Publications

International

- Bellone S., Della Corte F.G., **Di Benedetto L.**, Licciardo G.D. "An Analytical Model of the Switching Behavior of 4H-SiC p+-n-n+ Diodes from Arbitrary Injection Conditions", *IEEE Trans. on Power Electron*., Vol. 27, no. 3, pp. 1641-1652, 2012.

- Bellone S., **Di Benedetto L.**, Licciardo G.D., "A Quasi-One-Dimensional Model of the Potential Barrier and Carrier Density in the Channel of Si and 4H-SiC BSITs"*, IEEE Trans. on Electron Devices*, Vol. 59, no. 9, pp. 2546-2549, 2012.

- Bellone S., **Di Benedetto L.**, "An Analytical Model of I_{DS}-V_{GS} Characteristics for Si and 4H-SiC BSITs and VJFETs"*, submitted on IEEE Trans. on Power Electronics.*

- **Di Benedetto L.**, Bellone S., Rubino A., "4H-SiC Schottky Barrier using V_2O_5 as anode", *submitted to Journal of Applied Physics.*

- Nipoti R., **Di Benedetto L.**, Albonetti C., Bellone S., "Al^+ Implanted Anode for 4H-SiC p-i-n Diodes", *submitted to Journal of ElectroChemical Society.*

- Bellone S., **Di Benedetto L.**, "Design and Performances of 4H-SiC Bipolar mode Field Effect Transistor (4H-SiC)"*, submitted on IEEE Trans. on Power Electronics.*

- Bellone S., Della Corte F., **Di Benedetto L.**, Freda Albanese L., Licciardo G. D., "A Self-Consistent Model of the Static and Switching Behaviour of 4H-SiC Diodes", *IEEE International Semiconductor Conference, CAS,* 2010.

- **Di Benedetto L.**, Bellone S. "A Model of the Voltage Barrier in the Channel of 4H-SiC Normally-off JFETs", *IEEE International Semiconductor Conference, CAS,* 2012.

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National

- Bellone S., Della Corte F.G., **Di Benedetto L.**, Licciardo G.D., Pezzimenti F., "Investigation of 4H-SiC Bipolar Mode Field Effect Transistor (BMFET) as High Power Transistor", *Proc. of GE2011*, ISBN:978-88-95612-85-0, pp.35. 2011.

- **Di Benedetto L.**, Bellone S., "An Analytical Model of the Potential Barrier for the I_D-V_{GS} Curves Calculation of 4H-SiC Bipolar JFETs", *Proc. of GE2012*, ISBN: 978-88-6741-012-5, pp.39, 2012.

Book chapter

- Bellone S., Della Corte F.G., **Di Benedetto L.**, Licciardo G.D., "A review of the physical parameters for the analysis and simulation of SiC bipolar devices", Title: *Numerical Simulation*. Academy Publish Editor, *in press*.

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