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TESI DI DOTTORATO

A study on the role of dielectric and its interface in the performances of Organic Thin-Film Transistors

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“So once you know what the question actually is, you'll know what the answer means.”

Douglas Adams (The Hitchhiker's Guide to the Galaxy)

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In loving memory of my uncle,
Professor Pasquale Caruso

Contents

Introduction

Nowadays, it has become accepted that the word "electronic" qualifies an object for performance and superior skills and even introduces a degree of "intelligence" (we usually speak about such smart-phones, intelligent washing machines etc.), meaning that the machine has a certain logic that allows it to make some (often not) simple decisions. The introduction of electronics in everyday life has led to the birth of what today is called *information society,* where information exchange and processing (voice, images, textbooks, geographic data etc…) has to be very fast and in even more growing amounts but, more important, as technology advances, common objects designed for different purposes are fabricated in order to embed some information processing and storage capability.

For these reasons, if a well-established part of electronics concentrated its efforts on miniaturization, computational capabilities and volumes etc., a second part considers as its main purpose not the absolute performance in computing but the possibility to fabricate simple or complex devices or systems which are impossible to fabricate by means of standard silicon technology.

Emissive, thin, transparent, optically active, flexible, light emitting, light sensing, energy harvesting devices, low-cost circuitry, displays and antennas are just some examples and applications of Organic Electronics (OE), a branch of the science and technology addressing the electronic devices made from carbon-based materials and their integration.

Since the first evidences of the potential of organic materials in electronics when employed as conductors [1] or semiconductors [2] a multiplicity of desirable features made them appealing from industrial point of view as much to become a research priority of many industries, universities and research institutes worldwide.

2 Introduction

The ability of today's chemistry to synthesize organic molecules (Molecular Engineering) tailored for specific purposes and with features not common in inorganic semiconductors as silicon etc. has spread the objectives in the current landscape of applied scientific research and product development from the material development to device integration and then to device engineering, circuitry integration and optimization.

This run has, time after time, required the profusion of ever greater efforts on the implementation and optimization of electronic devices which can be integrated into circuitry fabricated on large area, flexible substrates with low-cost manufacturing processes reduced complexity and high yield and productivity.

As a result, a variety of fundamental electronic devices has been developed on the basis of organic materials (see figure 1).

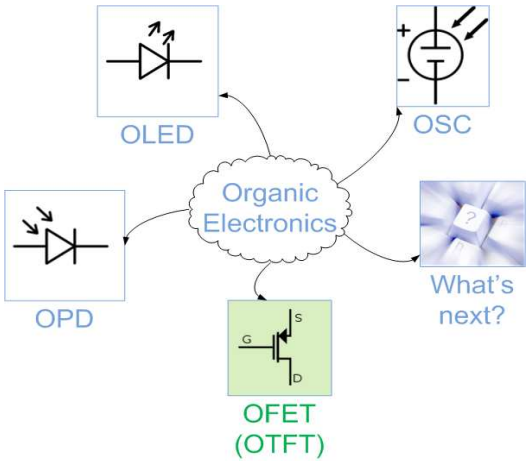

figure 1: organic electronics applications in basic devices.

Organic Light-Emitting Diodes [3] are just one of the most cited and exploited of organic semiconductors applications to electronic devices in because of the advances in opto-electronics and display technology. Furthermore, there is a plethora of studies which report Organic Semiconductors (OSCs) to be effective as building blocks of sensors, lasers, photodetectors, solar cells, rechargeable batteries, organic thin film transistors, RFIDs, wireless power transmission equipments etc.

The drawbacks of organic technology are often related to low charge-mobility and poor electrical performances. In part this is due to chemical, electrical and environmental stability issues and to the fact that process technology is still developing its instruments, methods and materials. For these reasons the cheaper processing technology of OE has still not reached the productivity and yield standards of the silicon technology.

In order to meet the technological challenges of OE that in the always-demanding landscape of organic active matrix display (AMOLED)[3][4], the devices involved in the driving logic of pixels are particularly critical when coupled to organic emissive elements (OLED stacks) because from their performances depend refresh rates, image brightness and screen pixel densities. On a scale of deeper detail, the creation of screens for large area electroluminescent displays cannot be separated from the design and optimization of a backplane that for each pixel is able to drive the optically active element at constant current, and to persist the information's state between a refresh and the other image.

The primary building block of digital or driving logic in organic electronics is the Organic Thin-Film Transistor (OTFT). In this kind of device, like in conventional FETs, the voltage applied to an insulated terminal controls the concentration of mobile charge in a resistive conduction channel (see figure 2). Thus, the current flowing between the two electrodes (Source and Drain) at the edge of the channel is modulated by means of the variation of the charge induced by the gate potential being the current density *j* bound to the charge density *n* in an n-type semiconductor neglecting the p-type carriers and to electric field "$\mathcal{E}$"[5]:

eq. 1

$$J_{DS} = q\mu_n n\mathcal{E}$$

Drain current can then be varied between two extreme conditions: from an off-state (no-current) and a saturation state (on status).

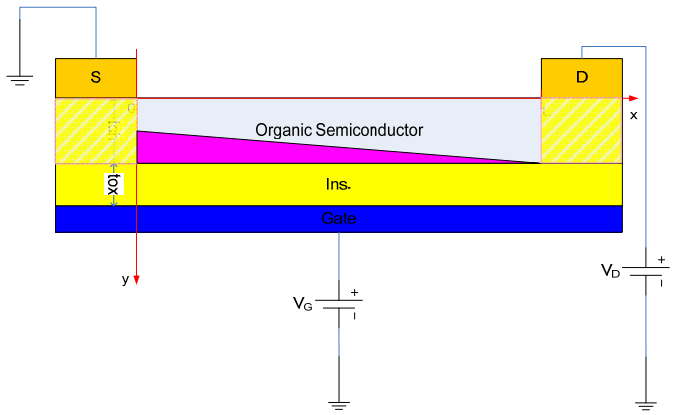

figure 2: basic scheme of an OTFT. S=Source electrode, D=Drain electrode, t_{ch} = channel semiconductor thickness, t_{ox}=gate insulator thickness, L=channel length.

For the reasons that have been already mentioned, the role of this kind of switching device is crucial in information displays field, thus major technology investments must be made to optimize the characteristics related to switching the power status of the pixel in order to obtain sufficient dynamics for a proper representation of moving pictures, movies, or whatever as required by the specifications set by applications where the display is intended.

Some examples of applications of OTFTs can be seen in literature results cited in figure 3

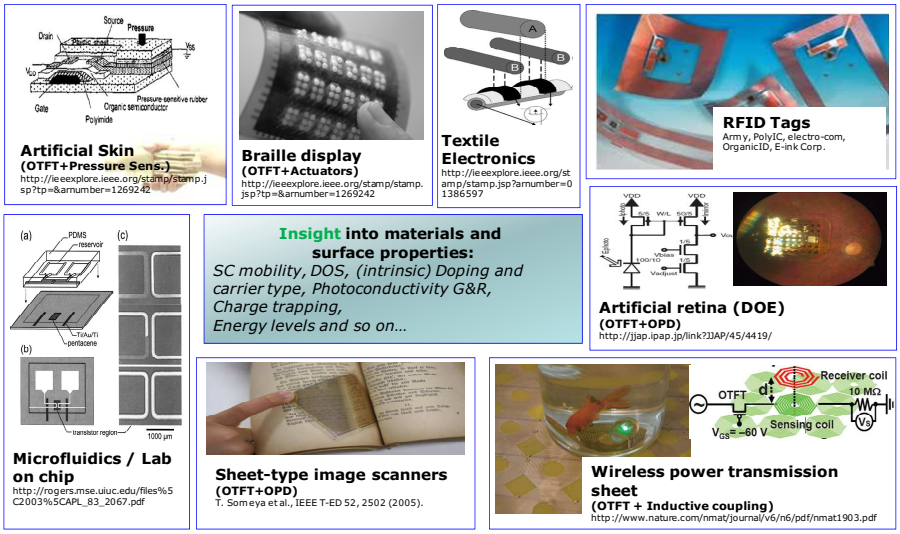

figure 3: an overview of applications of OTFTs as a building blocks of organic circuitry

In addition to the applications including organic FETs, it should be noted that the investigation methods of materials science often utilize these transistors as an a tool and an experiment employed to characterize the physical properties of semiconductors, insulators and interfaces by taking advantage of the principles operation and the fundamental physics of the device which will be discussed in the next chapter.

Motivation and purpose of this thesis

The theme of the present PhD thesis is the role played by the gate dielectric in the electrical performance of organic transistors and is based on the research activities described above. When talking about performances, not just charge mobility has to be considered but also it's necessary to take into account gate capacitance, threshold voltages, gate leakages and static power dissipations, operating voltages, drain currents and so on in order to get a deeper insight of what kind of specifications an OTFT device should obey to be suitable for industrial/commercial purposes.

In particular, in the present work the characteristics of the OTFTs have been analyzed in relation to manufacturing parameters and processes, focusing on non-ideal behaviors and aiming to optimize the characteristics of the transistor acting on morphologies, geometries and process conditions.

Excluding this introduction and the conclusions, the thesis is divided into four chapters.

The **first chapter** is a brief discussion about the working principles of OTFTs. The approach aims to reduce the complexity of the analysis in order to discuss the basic tools to study OFETs from the electrical point of view.

In the **second chapter**, a broad overview of the state of the art of technology for innovative methods of manufacturing for OTFTs shows topologies, materials and processing technology and integration issues and compares strengths and weaknesses to guide the experimental work subsequently documented by means of process recipes and details.

In the **third chapter** gate-leakage non-idealities are analyzed by changing the dielectric material in comparable structure topologies modeling the device by means of a circuital equivalent.

The **fourth chapter** is devoted to gate field-mobility and thermal analyses performed to investigate the main parameters changes in OTFT devices. In detail, by acting on dielectric material and gate insulator surface, we analyzed the a relationship between the nature of gate dielectric-semiconductor interface and the insulator itself. In order to accomplish this, a common device reference

structure has been designed and developed on the basis of chapter 2 and 3 considerations.

The study was addressed by characterizing the devices by measuring the static curves of output characteristics and gate-drain (input-output) trans-characteristics. Activation energy of the mobility of charge carriers in thermal measurements have also is extracted in the aim to investigate charge transport at dielectric-channel interface.

The tools employed in the proposed analyses are based on the model parameters of field effect transistors (mobility, threshold voltage, saturation current) and non-ideal factors linked to leakage currents but also gate-field dependent mobility models have been studied and introduced to model the presence of trap levels in disordered semiconducting mediums like in our case.

Among the adopted models, particular attention was paid to the extraction tools, modeling and analysis of gate leakage. The introduction of an equivalent circuit of the studied TFTs to separate intrinsic behaviors from non ideal-drifts has been performed. The developed simple model has been applied to characterize the thermal annealing effects on complete devices and to make consideration about the drift of gate currents.

Specific data concerning the development of manufacturing processes of OTFT were provided showing the routes that have enabled it to increase integration level and overall performance of studied transistors.

The survey on the major sources of non-idealities related to the dielectric-dielectric interface and channel modeling and characterization and analysis has led to the identification of morphological and process factors that can influence the mobility and current saturation in OTFT considered. Finally, an innovative inorganic dielectric deposited by liquid-phase using sol-gel process has been introduced to reveal specific characteristics compared to the data acquired so far. This was made possible by the methods of extraction of physical parameters such as current channel the energy of Meyer-Neldel without which it would not be possible to identify these correlations and the found exceptions.

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Chapter 1

Working principles

An Organic Thin-Film Transistor (OTFT) is an electronic device which unlike conventional silicon-based devices is built by means of thin-film deposition of organic materials; it utilizes the field-effect principle to control the density of current (j) flowing between two electrodes (Source and Drain) by varying the voltage applied to a third electrode terminal named Gate.

The gate terminal is insulated from the rest of the device, like in a capacitor's plate, then the gate current could be considered the leakage current making the drain signal controlled by a small-power signal (the gate voltage V_G).

Since OTFT shares with the MOSFET (Metal-Oxide Semiconductor Field-Effect Transistor) device this important feature and a part of the working principles, it has been supposed to play the same role in Organic Electronics than the one played from MOSFETs.

In conventional electronics FET-based circuits are extensively employed as signal amplifiers, switches, transmission gates logic, buffers, and drivers and so on.

For all these reasons MOSFETs are, in fact, considered the cornerstone of modern electronics but despites of the first-order similarities of OTFTs with MOSFETs, the integration of OTFT-based circuits cannot be considered straightforward not only because of technological reasons but also from the designer's point of view because of OTFT's intrinsic limitations and peculiarities which in part will be analyzed in the present chapter.

In inorganic TFTs and MOSFETs, the conduction type, (more precisely: the type of charge carrier involved in the conduction mechanism) is determined from the presence and the doping of the drain and source wells. Differently from their inorganic parents, in OTFTs the type of charge carrier involved in the conduction mechanism is not bound to doping but to the charge mobility of each

carrier and to the energy gap between the work-function of injecting S/D contacts and conduction/valence levels in the Organic Semiconductor.

Being thin-film FETs, differently from MOSFETs, TFTs and OTFTs lack of a substrate contact thus cannot work in inversion mode but just in accumulation and depletion mode.

1.1 A model for DC behavior for OTFTs

In this chapter a first-order description of the working principles of OTFTs is discussed. Some kind of *heavy* assumptions will be taken if necessary to go through an explanation of the DC electrical model of the device and to gain basic instruments necessary to evaluate device's performances and characteristics.

Physical details, interpretations and higher-order analyses are left to semiconductor's physics publications [1][2] and books [3] .

1.2 Model hypotheses

hp. 1) Device structure

In our analysis, OTFT's structure will be schematized as in figure 1 and considered variables depicted on the schema.

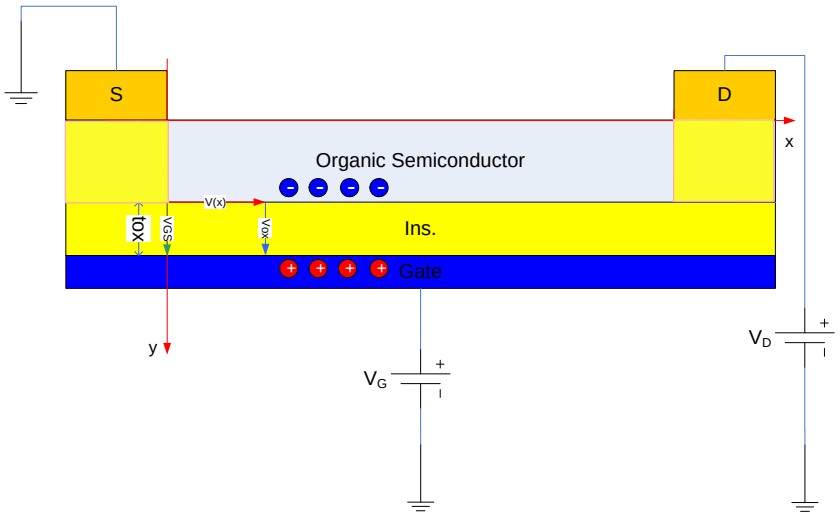

figure 1: theoretical schematization of an OTFT device structure. S=Source, D=Drain, Ins. = gate insulator

In figure 1, we named t_{ch} the channel thickness, t_{ox} the insulator thickness, V_{GS} the gate to source voltage, V(x) the voltage along the channel starting from the source's position.

hp. 2) Source and drain are considered as metal-semiconductor contacts having an ohmic behavior. In this case, their electrical resistance is hypothesized to be constant with the applied voltage.

For a contact between a metal and a n-type semiconductor this basic condition is reached when the energetic barrier φ_B from metal work-function φ_M to semiconductor material electron affinity χ_S is zero or negative being $\varphi_B = \varphi_M - \chi_S$ where φ_M is evaluated as the difference between the vacuum level (E_0) and the Fermi level (E_F) in the metal and χ_S is the difference between E_0 and the conduction band level in the semiconductor E_C.

More precisely,

$$\varphi_M \equiv E_0 - E_{F(Metal)}$$
$$\chi_S \equiv E_0 - E_{F(Semiconductor)}$$

for a metal/(n-type semiconductor) junction the barrier is:

$$\varphi_B = \varphi_M - \chi_S$$

and for a metal/(p-type semiconductor) junction:

$$\varphi_B = (E_G + \chi_S) - \varphi_M$$

Being $E_G = E_C - E_V$ the semiconductor's band-gap. In this case the barrier is the distance of the metal's Fermi level from valence band of the semiconductor.

hp. 3) Carrier diffusion effects are neglected and, for the matter of simplicity, n-type conduction hypothesized neglecting p-type carrier concentrations and currents. Once neglected diffusion currents, just the drift contribution $\underline{j_t}$ to current density will be considered.

hp. 4) Decoupling between injection mechanisms and field-effect. The charge density injected from source to channel $n_{DS}(x,y)$ will be considered independent from the charge density induced in the channel by the field effect $n_G(x,y)$ due to the gate potential V_{GS} and will be treated separately.

hp. 5) Charge mobility μ will be thought constant in the semiconductor material, and then its value will be considered in first approx. uniform and independent from applied voltages V_{GS} and V_{DS}.

hp. 6) Gradual channel approximation (GCA). The rate of variation of the lateral field $\mathcal{E}_x$ within the channel is considered much smaller than the rate of variation of the vertical field $\mathcal{E}_y$. An easy case in which this condition can be reached is when the channel length is assumed much higher than insulator thickness and the potentials V_{GS}, V_{DS} in the same range. Then:

$$t_{OX} << L \Rightarrow \mathcal{E}_x << \mathcal{E}_y$$
$$\left|\frac{\partial \mathcal{E}_x}{\partial x}\right| << \left|\frac{\partial \mathcal{E}_y}{\partial y}\right|$$

Thus, in GCA the voltage along the channel *V(x)* will be considered "smoothly" varying with the position abscissa x.

hp. 7) The insulator is not leaky, then we can consider I_G=0A.

1.2.1 **Problem definition and decoupling**

Under the abovementioned assumptions, the device's study can be decoupled along the x and y coordinates. In fact the current density in expression can be simplified as in eq. 1 and rewritten in eq. 2

eq. 1
$$J_{DS} \cong J_n \cong J_n^t = q\mu_n n\mathcal{E}$$
$$n = n_G + n_{DS} + n_0$$

eq. 2 $$J_{DS} = q\mu_n\left(n_G + n_{DS} + n_0\right)\underline{\mathcal{E}}$$

where n_G is the charge density induced by the field-effect, the n_{DS} is the charge density injected from the source and n_0 is the charge density already present in the channel.

Then, the Poisson's equation can be also rewritten as in eq. 3:

eq. 3 $$\nabla\underline{\mathcal{E}} = \frac{\rho}{\varepsilon} \cong \frac{\rho_n}{\varepsilon} = -\frac{q\left(n_G + n_{DS} + n_0\right)}{\varepsilon}$$
$$\frac{\partial\mathcal{E}_x}{\partial x} + \frac{\partial\mathcal{E}_y}{\partial y} \cong -\frac{q\left(n_G + n_{DS} + n_0\right)}{\varepsilon}$$

along the two directions.

By using the GCA, we can split the two-dimensional problem seen in eq. 3 in a couple of monodimensional equations as in eq. 4.

eq. 4 $$\frac{d\mathcal{E}_y(y)}{dy} = -\frac{q\left(n_G(y) + n_0\right)}{\varepsilon}$$
$$\frac{d\mathcal{E}_x(x)}{dx} = -\frac{qn_{DS}(x)}{\varepsilon}$$
$$\underline{J}_{DS} = q\mu_n\left(n_G + n_{DS} + n_0\right)\underline{\mathcal{E}}$$

1.2.2 **Drain current calculation**

The drain current can be obtained by integrating the current density on the section $\underline{S}_{wy}(x)$ of the channel material at the abscissa x shown in figure 2.

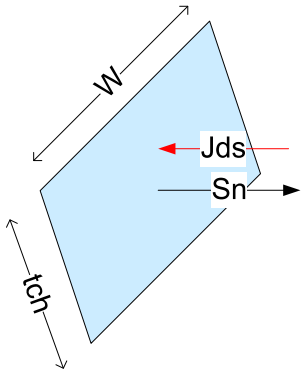

figure 2: integration section for the channel current

Where $\underline{J}_{DS}$ is the current density in the channel, W the channel width and S_n the direction normal to the surface $\underline{S}_{wy}(x)$ that we will hypothesize to be along x.

Thus, we can write:

$$I_D = \iint_{S_{WY}(x)} \underline{J}_{DS} \cdot \underline{dS} =$$

$$= -\int_0^{t_{ch}} \int_0^W q\mu_n \left(n_G + n_{DS} + n_0\right) \mathcal{E}_x \cdot dydw =$$

$$= -W\mu_n \mathcal{E}_x \int_0^{t_{ch}} q\left(n_G + n_{DS} + n_0\right) dy =$$

$$= -\mu_n W\left(-Q_G - Q_{DS} - Q_{n0}\right) \mathcal{E}_x(x)$$

eq. 5

Then, it will be necessary to evaluate the superficial charges involved in the calculation Q_G, Q_{DS} e Q_{n0} at the position x.

As in a capacitor, the gate-induced charge can be written as follows:

$$Q_G = -C_{ins} V_{ins} = -C_{ins}\left(V_{GS} - V(x)\right) \qquad \text{eq. 6}$$

Where C_{ins} is the specific capacitance of the gate which can be calculated as:

$$C_{ins} = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} \qquad \text{eq. 7}$$

being ε_0 the vacuum dielectric permittivity and ε_r the relative permittivity of the dielectric.

$$\left.\begin{aligned} Q_{DS} &= -\int_0^{t_{ch}} qn_{DS}\cdot dy \\ \frac{d\mathcal{E}_x(x)}{dx} &= -\frac{qn_{DS}(x)}{\varepsilon_{ch}} \end{aligned}\right\} \Rightarrow$$

eq. 8
$$Q_{DS} = \varepsilon_{ch}\int_0^{t_{ch}} \frac{d\mathcal{E}_x(x)}{dx}\cdot dy = \frac{d\mathcal{E}_x(x)}{dx}\varepsilon_{ch}\int_0^{t_{ch}} dy \Rightarrow$$
$$Q_{DS} = t_{ch}\varepsilon_{ch}\frac{d\mathcal{E}_x(x)}{dx}$$

Keeping in mind that, because of the hp.4, Q_{DS} has been supposed to depend only from source-injected charge and then from the electric field along channel's direction ($\mathcal{E}_x$), we can calculate it using the Poisson's equation like in eq. 8 then, charge densities can be summarized in eq. 9.

eq. 9
$$Q_{DS} = t_{ch}\varepsilon_{ch}\frac{d\mathcal{E}_x(x)}{dx};\quad Q_G = -C_{ins}(V_G - V(x));\quad Q_{n0} \equiv -C_{ins}V_0$$

Performing substitutions of eq. 9 in eq. 5 we can estimate the channel's current as in eq. 10.

eq. 10
$$I_{DS} = -\mu_n W(Q_G + Q_{DS} + Q_{n0})\mathcal{E}_x =$$
$$-\mu_n W\mathcal{E}_x\left[C_{ins}(V_G - V(x)) - t_{ch}\varepsilon_{ch}\frac{d\mathcal{E}_x(x)}{dx} + C_{ins}V_0\right]$$

This expression is still channel-position dependent then, it has to be integrated along the abscissa *x* to relate I_{DS} to electrode's external potentials like in eq. 11 being X a generic coordinate in the channel's length.

eq. 11
$$-\int_0^X \frac{I_{DS}}{\mu_n W} dx = \\ = \int_0^X \mathcal{E}_x(x)\left[C_{ins}(V_G - V(x)) - t_{ch}\varepsilon_{ch}\frac{d\mathcal{E}_x(x)}{dx} + C_{ins}V_0 \right] dx$$

Then, being

eq. 12
$$\mathcal{E}_x(x) = -\frac{dV(x)}{dx}$$

We can substitute the potential in eq. 11, we obtain:

eq. 13
$$-\int_0^X \frac{I_{DS}}{\mu_n W} dx = \\ = \int_0^X -\frac{dV(x)}{dx} C_{ins}(V_G - V(x))dx + \\ \int_0^X -\frac{dV(x)}{dx}\left(-t_{ch}\varepsilon_{ch}\frac{d\mathcal{E}_x(x)}{dx} \right) dx + \\ + \int_0^X -\frac{dV(x)}{dx} C_{ins}V_0 dx$$

Then,

eq. 14
$$-\int_0^X \frac{I_{DS}}{\mu_n W} dx = \\ = -C_{ins}\left(V_G V(X) - \frac{V^2(X)}{2} \right) + \\ \int_0^X -t_{ch}\varepsilon_{ch}\frac{d\mathcal{E}_x(x)}{dx}\frac{dV(x)}{dx} dx + \\ -C_{ins}V_0 V(X)$$

In eq. 14, an approximated estimation of the contribution to the I_{DS} due to charge injection is related to the second term. Such term can be rewritten as in eq. 15:

eq. 15
$$\int_0^X t_{ch}\varepsilon_{ch}\frac{d\mathcal{E}_x(x)}{dx}\frac{dV(x)}{dx}dx = \int_0^X t_{ch}\varepsilon_{ch}\frac{d\mathcal{E}_x(x)}{dx}(-\mathcal{E}_x(x))dx = \\ = \int_0^X t_{ch}\varepsilon_{ch}\cdot d\mathcal{E}_x(x)(-\mathcal{E}_x(x)) = -\frac{t_{ch}\varepsilon_{ch}(\Delta\mathcal{E}_x)^2}{2}$$

with $\Delta\mathcal{E}_x \equiv \mathcal{E}_x(X)-\mathcal{E}_x(0)$.

Therefore, it's possible to relate the injected current contribution (Injection-FET – IFET [1]) to the electric field magnitudes near the electrodes by eq. 15 then, by extending the integration results to the [0, L] interval by putting X=L, a drain current approximation can be derived as follows:

eq. 16
$$-\int_0^{X=L}\frac{I_{DS}}{\mu_n W}dx = -C_{ins}\left(V_G V_{DS}-\frac{V_{DS}^2}{2}\right)-\frac{t_{ch}\varepsilon_{ch}(\Delta\mathcal{E}_x)^2}{2}-C_{ins}V_0V_{DS}$$
$$\frac{I_{DS}}{\mu_n W}L = C_{ins}\left(V_G V_{DS}-\frac{V_{DS}^2}{2}\right)+\frac{t_{ch}\varepsilon_{ch}(\Delta\mathcal{E}_x)^2}{2}+C_{ins}V_0V_{DS}$$

eq. 17
$$I_{DS} = \mu_n\frac{W}{L}\left[C_{ins}\left(V_G V_{DS}-\frac{V_{DS}^2}{2}\right)+\frac{t_{ch}\varepsilon_{ch}(\Delta\mathcal{E}_x)^2}{2}+C_{ins}V_0V_{DS}\right]$$

Or simply:

eq. 18
$$\boxed{I_{DS} = \mu_n C_{ins}\frac{W}{L}\left((V_G+V_0)V_{DS}-\frac{V_{DS}^2}{2}\right)+\frac{1}{2}\mu_n\varepsilon_{ch}t_{ch}\frac{W}{L}(\Delta\mathcal{E}_x)^2}$$

The formula in eq. 18 gives the static characteristics of the device in the accumulation mode when $V_{GS}+V_0 \leq V_{DS}$. Differently from the standard MOSFET equation [3] in the active region, there's an injection-dependant contribution (see eq. 18 and eq. 19).

$$\text{eq. 19} \qquad I_{DSinj} = \frac{1}{2}\mu_n \varepsilon_{ch} t_{ch} \frac{W}{L} \left(\Delta \mathcal{E}_x\right)^2$$

Such contribution (see eq. 19) takes into account the space-charge limited current near the drain electrode becomes relevant at high drain fields, for short channels and for relatively thick semiconductor layers and can explain some deviations from the standard model such as the lack of a saturation behavior for higher source-drain voltages.

The lack of saturation in the channel current can be observed after Koehler-Biaggio works [1] by adopting the same formalism utilized to model charge injection in insulators in the Gurney-Mott approach. Non-saturation effects are more pronounced at low gate voltages and ad it has been shown in figure 3.

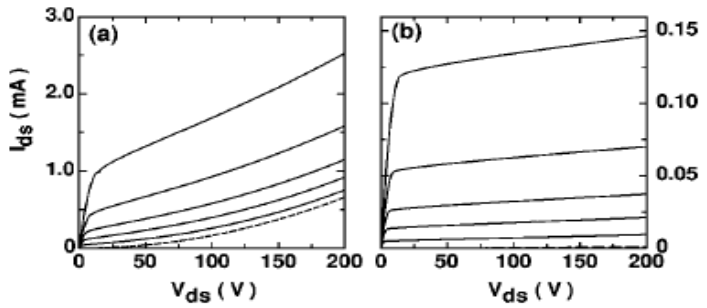

FIG. 2. Current-voltage ($I-V$) characteristics of two surface IFET. The simulation parameters are $C_i=1.76\times10^{-4}$ Fm^{-2}, $\mu=10^{-4}$ m^{2}V^{-1}s^{-1}, $n_0=10^{20}$ m^{-3}, $W=1.5$ nm, $D=100$ nm, $\epsilon=3$, $L=3$ μm (a), and $L=25$ μm (b). The curves were plotted with increasing gate voltage of 0 V [dashed curve, not visible in (b)], 3, 5, 7, 10, and 15 V (continuous curves).

figure 3: non-saturating behaviour of channel current due to the contribution of the injection at S/D electrodes as shown by Koehler-Biaggio in [1].

1.3 Brief on working regimes of OTFTs

In this section, a quick overview of operating regions for modeled OTFT devices is given to introduce terms and concepts which will be utilized in the next chapters.

Linear region

In the linear regime, a film of mobile charge is formed at the interface between the insulator and the semiconductor material.

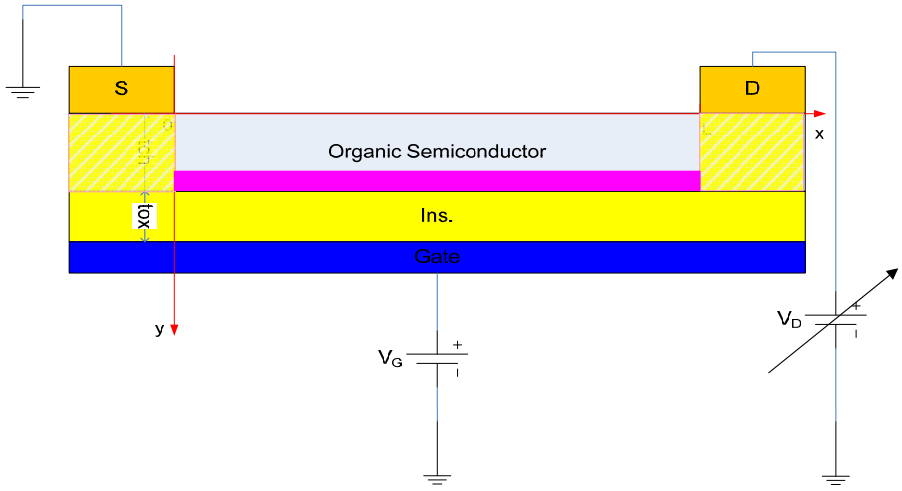

figure 4: OTFT working in the linear region representation; the purple zone is a simplified view of the mobile charge in the channel.

In the hypothesis of $V_{DS} \leq V_G + V_0$, we can consider valid the GCA and uniform the electric field component $\mathcal{E}_x$ along the D/S direction. Then, we can approximate it as: $\mathcal{E}_x \approx V_{DS}/L$ and neglect the injection current contribution which is bound to Q_{DS} and to the difference $(\mathcal{E}_x(L) - \mathcal{E}_x(0))^2$, then the channel current can be approximated by eq. 20

$$\text{eq. 20} \qquad I_{DS} = \mu_n C_{ins} \frac{W}{L}\left(\left(V_{GS} + V_0\right) \cdot V_{DS}\right)$$

and behaves as a resistor with the gate potential modulating its conductance.

Pinch-off

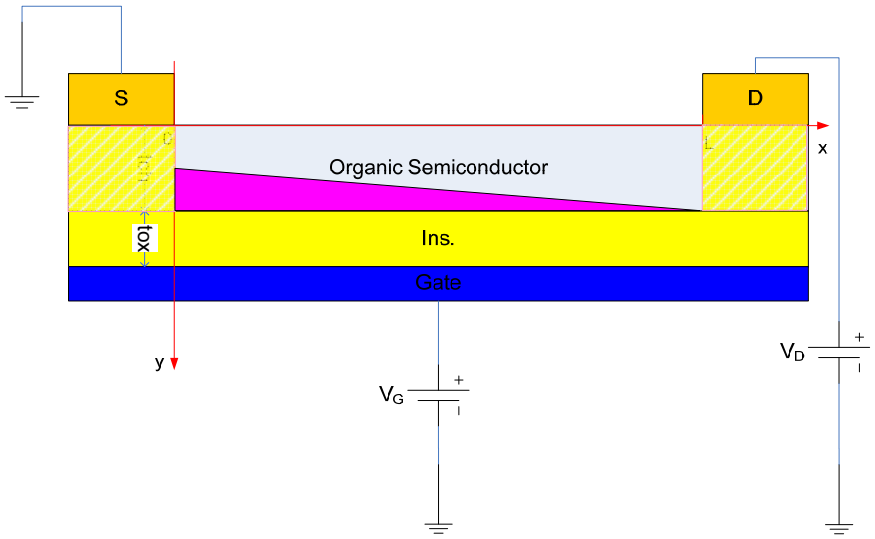

figure 5: OTFT polarization at the pinch-off

In this working region, operating voltages are in the range of $V_D \geq V_G + V_0$, thus there will be an abscissa x_0 such as if $x \geq x_0$ there will be no mobile charge in the channel (in other terms, the semiconducting layer is completely *depleted*). For $x < x_0$, as x approaches x_0, the mobile charge density becomes lower leading to the presence of a depleted region near the drain where the voltage drop will fall to zero (see figure 5 and figure 6). Then, there will be a range of x where the GCA is no more valid because the fields relationship ($\mathcal{E}_x << \mathcal{E}_y$) will fall. For the pinch-off condition, if $x > x_0$, $V(x) > V_{GS} + V_0$ and for $x > x_0$, we obtain the voltage drop across the conducting channel (eq. 21).

eq. 21
$$x = x_0 \Rightarrow Q_G + Q_0 = 0 \Rightarrow -C_{ins}\left(V_{GS} - V\left(x_0\right)\right) + Q_0 = 0 \Rightarrow$$
$$-C_{ins}\left(V_{GS} - V\left(x_0\right)\right) - C_{ins}V_0 = 0 \Rightarrow V\left(x_0\right) = V_{GS} + V_0$$

Thus, the channel current will become independent from the V_{DS} being $V_{GS}+V_0$ the voltage applied to the conducting channel.
Then we will have to use the characteristics reported in eq. 18 substituting:

$$V_{DS} \rightarrow V_{GS}+V_0$$
$$L \rightarrow x_0$$

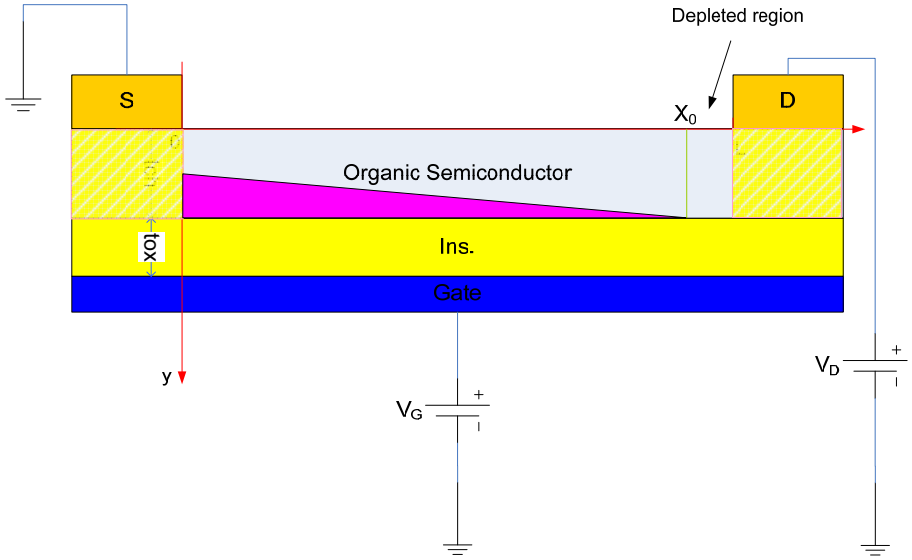

figure 6: depletion abscissa in the OTFT

If the length of the depleted region is neglected if compared to L, eq. 18 becomes:

$$I_{DS} = \mu_n C_{ins} \frac{W}{L}\left((V_{GS} + V_0)V_{DS} - \frac{V_{DS}^2}{2} \right)\Bigg|_{V_{DS}=V_{GS}+V_0} +$$

eq. 22

$$+ \frac{1}{2}\mu_n \varepsilon_{ch} t_{ch} \frac{W}{L} (\Delta \mathcal{E}_x)^2 =$$

$$= \frac{1}{2}\mu_n C_{ins} \frac{W}{L} (V_{GS} + V_0)^2 \Big|_{V_{DS}=V_{GS}+V_0} + \frac{1}{2}\mu_n \varepsilon_{ch} t_{ch} \frac{W}{L} (\Delta \mathcal{E}_x)^2$$

As described by eq. 22, the field-effect modulated component of the channel current saturates at the pinch-off, in the depleted region, the vertical electric field pushes the free carriers far from the semiconductor-channel interface and when x is in $[x_0,L]$, then $Q_G + Q_0 = 0$ then, the second term of the eq. 22 can also be considered in the depleted region:

$$I_D = -\mu_n W(-Q_{DS})\mathcal{E}_x(x) = \mu_n W \mathcal{E}_x(x) \int_0^{t_{ch}} -qn_{DS}\, dy =$$

eq. 23

$$= \mu_n W \mathcal{E}_x(x) \int_0^{t_{ch}} \varepsilon_{ch} \frac{d\mathcal{E}_x}{dx} dy = \varepsilon_{ch}\mu_n W t_{ch} \mathcal{E}_x(x) \frac{d\mathcal{E}_x}{dx}$$

By integrating in the depleted region $[x_0,L]$, we obtain:

$$\int_{x_0}^{L} I_{DS}\, dx = \int_{x_0}^{L} \varepsilon_{ch}\mu_n W t_{ch} \mathcal{E}_x(x) d\mathcal{E}_x$$

eq. 24

$$\Rightarrow I_{DS} = \varepsilon_{ch}\mu_n \frac{W}{L - x_0} t_{ch} \int_{x_0}^{L} \mathcal{E}_x(x) \frac{d\mathcal{E}_x}{dx} dx$$

Then,

$$I_{DS} = \varepsilon_{ch}\mu_n \frac{W}{L - x_0} t_{ch} \frac{(\mathcal{E}_x(L) - \mathcal{E}_x(x_0))^2}{2}$$

eq. 25

In the $[x_0,L]$ region, the density of free charge is very low if compared with the channel ($[0,x_0]$), then we can approximate the character of I_{DS} as shown in (eq. 26):

$$\mathcal{E}_x(x) >> \mathcal{E}_x(x_0) \approx \mathcal{E}_x(0) \quad \forall x > x_0 \Rightarrow$$
$$\Rightarrow I_{DS} \approx \varepsilon_{ch}\mu_n \frac{W}{L-x_0} t_{ch} \frac{(\mathcal{E}_x(L))^2}{2} \approx \varepsilon_{ch}\mu_n \frac{W}{L-x_0} t_{ch} \left(\frac{V(L)-V(x_0)}{L-x_0} \right)^2 \Rightarrow$$
$$\Rightarrow I_{DS} \propto \frac{(V_{DS}-V(x_0))^2}{(L-x_0)^3}$$

eq. 26

This explains the power-law behavior shown in figure 3 for high D to S fields.

1.4 Thermally activated conduction and compensation rules.

The dependence of charge mobility in organic semiconductor channels from temperature and gate fields for OTFT devices is one of the subjects which have attracted the attention of the recent literature studies [4][5][6][7] in the last years but still today, the charge transport in such materials is still not fully understood.

In organic semiconductors, such dependence has been described in terms of multiple charge trapping [14]), hopping [7], charge diffusion processes [4] etc. by starting from common evidence which is the starting point for all these models developments: the dependence of the thermal activation energy Ea for the mobility from the gate voltage. In particular, we are referring to a phenomenon which for the matter of simplicity we will call X (i.e. conductivity activation in the active region of the OTFT) and evidencing a thermally-activated behavior and following an exponential Arrhenius-like law versus the temperature (see eq. 27).

eq. 27 $$X = X_0 e^{\left(\frac{-E_a}{k_B T}\right)}$$

In eq. 27, k_B is the Boltzmann constant, T is the absolute temperature, Ea is the activation energy of the process. In the hypothesis of Arrhenius-behavior Ea can be extracted by experimentally like suggested in [9].

The rule which is empirically obeyed for a wide variety of thermally-activated physical processes is about the pre-factor X_0 in the eq. 27 and implies X_0 growing exponentially with the activation energy Ea like in

$$\text{eq. 28} \qquad X_0 = X_{00} e^{\left(\frac{-E_a}{E_{MN}}\right)}$$

Such feature goes under the name of Meyer-Neldel Rule (MNR) from the names of its discoverers [9].

In eq. 28 X_{00} is a constant (non-thermally activated) pre-factor; E_{MN} is the characteristic energy of the process and is named Meyer-Neldel Energy (MNE). By substituting the MNR law (eq. 28) in the Arrhenius law (eq. 27), we obtain:

$$\text{eq. 29} \qquad X = X_{00} e^{\left[-E_a\left(\frac{1}{k_B T}-\frac{1}{E_{MN}}\right)\right]}$$

This implies the existence of a typical temperature $T_{MN}=E_{MN}/k_B$ (named *isokinetic* temperature) which makes the process X independent from Ea and finally from the physical parameters which make Ea change.

In the case o fan OTFT, once named *X* the channel's mobility, for $T = T_{MN}$ the Activation energy becomes independent from the gate voltage. This will be by now the meaning that we attribute to the T_{MN}. As we told before, MNR (eq. 29) has been observed for a plethora of physical processes but the quest for the link between the macroscopic source of this behavior and the physical meaning of E_{MN} is still matter of discussion[4] because of its potentiality to be a general rule for the determination of the break-even point in the competition of two opposed activated processes. That's why it has also been referred as compensation *rule.*

1.5 Models for the extraction of the channel current

In the study of OTFTs, it's necessary to consider the contribution to Source and Drain currents due to a non ideal behavior of the gate dielectric which acts as a leaky insulator. This implies a non-perfect insulation of the gate versus the channel and then versus S/D contacts which are usually named *gate-leakages*. The presence of such parasitic currents which reflects in a non-null gate current $I_G \neq 0$ and then in a static power dissipation in the gate, makes not straightforward the determination of the channel current (I_{ch}) which otherwise can be confused with the drain-to-source current (I_{DS}). This non-ideality makes complicated the derivation of the channel current (the one which is usually predicted by the physical models i.e. in eq. 18 or in the ubiquitous utilizations of the MOSFET equations). In a deeper detail, from static measurements, we can measure I_D, I_S and I_G but for physical modeling purposes, I_{ch} is the parameter which cannot be directly measured but which is the only one, in a static context, which can be thought directly connected to charge transportation in the semiconductor channel.

Nevertheless, because of the failure of the approximation of I_{ch} to I_{DS}, performance parameters for the OTFT, transconductance, field-effect mobility, on/off ratio, threshold voltage, on-set voltage etc. cannot be directly extracted then also modeling can be sometimes not physically consistent because of the presence of these parasitic currents. Then, also the extraction of working parameters under thermally activated conditions suffers from an undesired shift in the electrical behavior from the real phenomenon and also from theoretical models.

For devices having negligible gate-leakages, it's easy to suppose $I_S \approx I_D \approx I_{DS} \approx I_{ch}$ otherwise channel current has to be estimated in an indirect way. Such kind of non-ideality is much more relevant for long-channel devices because of a larger leakage section [10][11]. In fact, I_{ch} grows linearly with the W/L ratio as in the first-order MOSFET model but the gate current I_G is related to channel's surface (W·L) then, in a perspective of first approximation,

$$\text{eq. 30} \qquad \frac{I_{DS}}{I_G} \propto \frac{\frac{W}{L}}{W \cdot L} = \frac{1}{L^2}$$

Thus the effect of the gate leakage on the error in the estimation of the channel current from I_{DS} grows with the square of the drain to source distance. In literature, it has been successfully employed a method to extract the channel current in inorganic leaky MISFETs (Metal-Insulator-Semiconductor Field-Effect Transistor) which were affected from non-negligible gate dissipations [12][13]. The method is based on the observation of the variations of I_G with the bias being $I_G = I_G(V_{GS},V_{DS})$ and the extraction of the I_{ch} is made possible by making assumptions on the leakage current components. In detail, Palestri et. Al. started hypothesizing the gate current infinitesimal contribution along the channel direction x to decrease in an uniform way when moving from x = 0 to x = L then, for $V_{DS} \neq 0V$ the change in the gate current density should be considered a linear function of x. Under these conditions an approximation for I_{ch} can be calculated algebraically from measurable quantities with an error which is weakly dependent from bias voltages and at the first order, according to Esseni et. Al. the channel's current can be written as:

$$\text{eq. 31} \qquad I_{ch}^{extim} = \frac{I_s + I_D}{2} - \frac{I_{G0} - I_G}{6}$$

Where $I_{G0} = I_G(V_{GS})|_{VDS=0}$ is the gate current at $V_{DS} = 0V$ at a given V_{GS} and $I_G = I_G(V_{GS})|_{VDS}$ is the gate current for $V_{DS}>0$ at the same V_{GS}.

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Chapter 2

A survey on the state of the art Organic Thin-Film Transistors processing

This chapter is a brief overview of common features, technology and advances in the OTFT branch of Organic Electronics. This introduction, without pretending to be neither complete nor extensive has the objective to sketch out the framework in which the present thesis goes to insert itself. Some significant Literature results have been collected about materials, dielectrics, channel organic semiconductors and the related processing techniques to make easier the tagging of the major on-going activities in OTFT and in the interest sectors where investigations and optimizations are still necessary.

2.1 Performance parameters

Performance of a single organic FET can be evaluated by considering results already assessed for MOSFET devices because they share with them part of the working principles, first-approximation models and some circuital topologies they are intended to be used for [3][4][5].

In particular for the sake of their technological and design relevance a great part of the attention is today dedicated to:

- Charge mobility (μ)
- Gate leakages
- Gate breakdown voltages
- I_{on}/I_{off} ratio
- Threshold and on-set voltages
- Sub threshold slope

- Ageing and stress factors
- Dynamic/AC behaviours

These parameter are known to be relevant in the determination of the switching speed, static and dynamic power dissipations, logic thresholds and noise margins in digital logics based on MISFETs and finally in the design on complementary-logic circuitry.

Keeping in mind these considerations, it's natural to understand why among the principal efforts of the research in material development there is the achievement of high charge mobility values, elevated on/off ratios and low working voltages (and threshold voltages).

For these reasons, for a long time, the attention has been kept on the synthesis and development of organic materials which, when employed as channel semiconductors, would result in high field-effect mobility and low concentration of trap states.

As technology advances and as research deepens its knowledge of new material's physics and chemistry, from the study of new chemical formulations and novel processing technologies, the focus is moving to integration and optimization-related issues switching to higher order perspectives and to system-specific aspects like the necessity to have the availability of both n-type and p-type OFETs but also to make predictable controllable and repeatable the threshold voltages.

Furthermore, another fundamental issue is related to device processing, in fact to make effective the employment of OTFTs, it has become evident the need for fabrication workflows which fit the realization of complementary CMOS-like circuits. From this point of view, the evidence that the maximum operating frequencies (clock-frequencies) are connected (from the device's point of view) not only to channel's mobility but also to the capacitive load effect of the gates on the driver circuits, recalls that aspects as gate overlaps and geometric tolerances in layouts and then to design rules have to be addressed [27].

Also environmental and stability issues are emerging as an industrial scenario comes to be prospected: the need for organic materials and devices which exhibit low sensitivity to external contaminations, humidity, oxygen, light etc. are even more

emphasizing the role played by passivation, encapsulation and packaging techniques.

Pushing once more forward the challenges that have to be meet in this field, it will be soon a must the implementation of a scalable and integrable technology consisting of standard libraries of devices, layouts etc. to enable the industrial design to develop new products based on this class of transistors. But, in order to achieve this objectives and beyond some material developments, processes and modeling topics have to be addressed and faced with a system-oriented approach.

2.2 Technological overview

As we told before, from the perspective of a single OTFT device, the main performance parameter is the field-effect mobility of carriers in the channel of the transistor which, for our purposes is not the material's intrinsic property but the on extracted from device's characteristics (μ_{FET}) taking then into account issues related to purity, thin film processing and features, surface traps etc. Its main role played in CMOS-based logic gates is related to switching behaviours, speed and clock-related dissipated power.

Furthermore, the current scientific/technological landscape in material science is well-described by the progresses of such parameter versus time.

In the following image (figure 1) we report the evolution of OTFT performances for p-Type transistors in the last two decades taken from a sector review [4]:

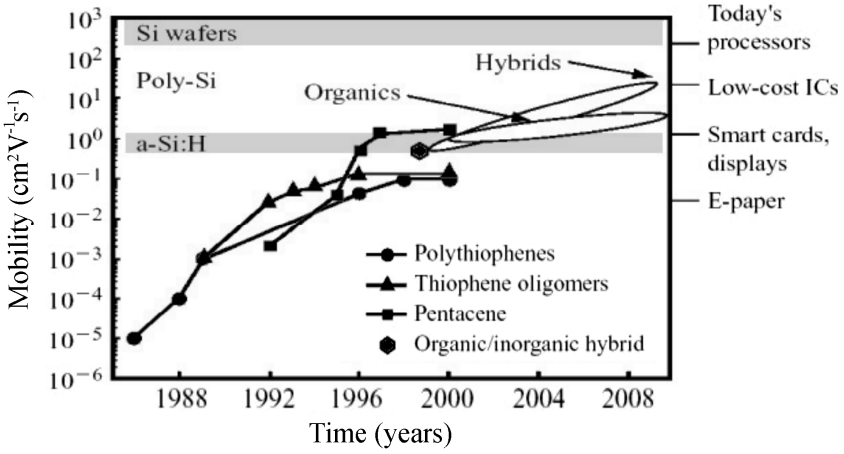


figure 1: evolution of p-type organic semiconductors in OTFT devices studied from charge mobility point of view[4].

If we compare the evolution of p-type materials with the n-type ones in OTFT technology, we can see that performances were till to 2001 under the threshold of what was possible to do industrially with amporphous silicon-based devices commonly employed in LCD driving backplanes [6] making the n-type organic devices still not competitive for large-area applications.

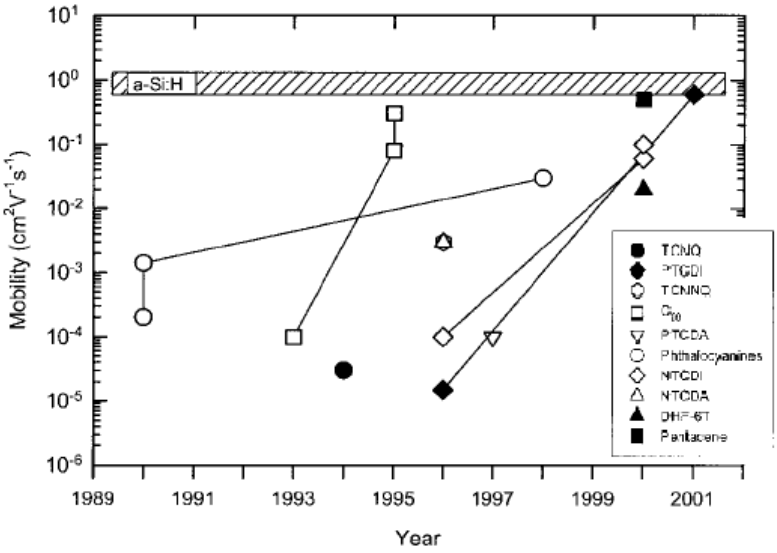


figure 2: the evolution of n-type devices and materials till to 2001 [6]

Only after those years, a consistent number of valuable results have been obtained in the field of n-type organic semiconductors also thanks to the works of Facchetti, Marks et. al. who addressed fundamental issues involving the synthesis, the stability and processing of this class of organic semiconductors with a novel approach [18][26][37].

2.3 Common architectures for OTFT layouts

Depending on the deposition and patterning processes used for manufacturing of TFT, it's possible to distinguish between four main distinct topologies based on the location of the gate electrode, source and drain compared to the channel and substrate.

2.3.1 Bottom-gate top-contacts structure (BGTC)

In such architecture, the gate is located directly in contact with the substrate. Therefore the patterning process is simplified (see figure 3). As an instance, if gate was made of inorganic materials (metals, transparent conductive oxides (TCO), etc.), it might be patterned by conventional photolithography or other methods involving the use of acids and solvents which cannot come in contact with organics. In this case, the parameter to consider is, of course, the compatibility of the patterning and the etching processes with the material from which the substrate is made.

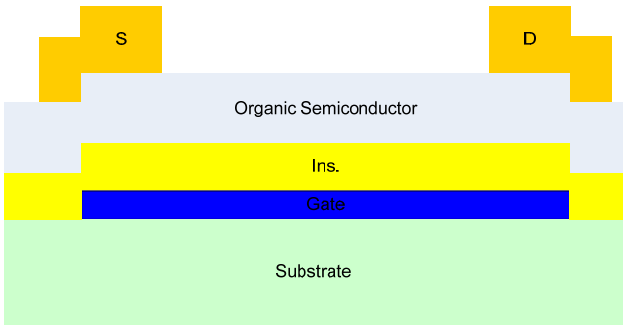


figure 3: a sketch of the structure of a bottom-gate top-contacts device

It is easy to convince oneself that this kind of topology, easily allows to obtain structures with micrometer-sized gate structures but this not always results in transistor with micrometric channel lengths because on the other hand, this feature depends also from source and drain electrodes patterning ("S" and "D") and the alignment with the gate itself.

In fact, usually the metal contacts are deposited by vapor phase through a shadow mask which makes particularly difficult to obtain structures with low gate-overlaps and, at the same time, to have a small channel length.

Once considered the above limitations, the BGTC structure can be considered particulary useful as a test structure for the channel material thanks the simplicity of the device's processing which, in the most usual case, sets channel width and length (*W* and *L*) during the deposition of patterned source and drain.

2.3.1.1 Alternative means in device's contacts patterning

Obviously, for metals and other inorganics, subtractive patterning methods already employed in the realization of active-matrix displays exist and now would allow the creation of bottom-contacts or top-gated structures. Among them, we remember the cold-welding process used by Kim, Forrest and Burrows in the definition of the geometry of the cathodes in OLED devices [11].

This method is based on a process characterized by the welding between a metallic film and a mould coated by the same metal and by the application of a convenient pressure to bring the two surface in close contact performing the junction without the need of heating the system (see figure 4). In this case, the mould extraction is able to perform a micrometric-scale patterning of a metal film deposited on organic layers like in an sort of inverse *lift-off* process .

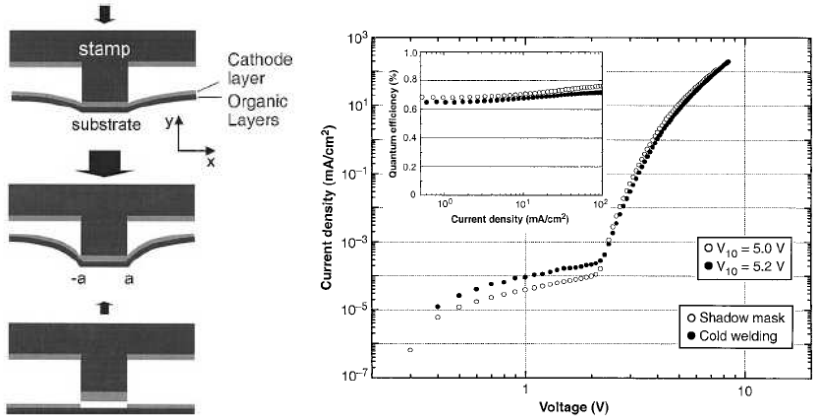


figure 4: A cold-welding/lift-off method for the patterning of metallic films when deposited on organic materials. The techniques produces OLED devices having performances really closet o the ones patterend by stencils [11].

2.3.2 Top-gate bottom-contacts (TGBC) structure

In this case, Source and Drain geometries are the one that benefit of a simpler and more robust processing technique because they are (similarly to the gate in the case of BGTC) deposited directly on the substrate (see figure 5). There's no need to say that substrates are less critical in the device fabrication than OSCs and often allow standard photolithography and other common deposition processes.

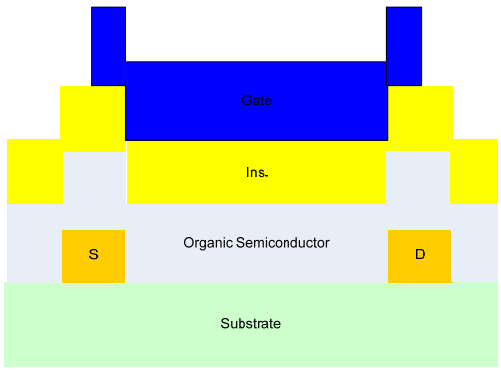


figure 5: top-gate bottom-contacts (TGBC) process.

Examples of top-gate bottom-contacts architectures are shown and explained in literature on prototypes having high performances and also advanced features from the technological perspective. For instance, in [12], a TGBC OTFT having a channel made by pentacene has been processed by thermal evaporation of both the semiconductor and the insulating stack and also the gate. This processing technique led to the integration of a simple organic pixel (an OFET driving an OLED) sketched in the figure 6 taken from literature results[12].

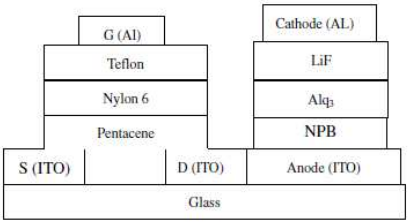


figure 6: integration of organic display pixels by an evaporation-based technology [12]

We also have to add that, once the channel's OSC has been deposited photolithographic processes could still be possible if the gate insulator is a good encapsulant or if appropriate encapsulation techniques are adopted like in [14]. Infact, as we can state by reading the referred work [14] and from figure 7, a silicon nitride (SiN_x) can have enough barrier properties to make gate pattering possibile. In the specific case, a SiN_x film has been deposited by PECVD at low temperature (75°C)[13] and acted as an encapsulant for the subsequent gate patterning processes.

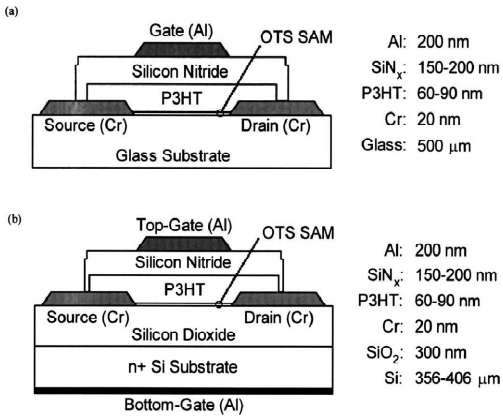


figure 7: Top-gated OTFT architectures are fabricated by photholithography of the gate electrode on a protective SiN_x gate dielectric acting as a barrier[14].

2.3.3 Bottom-gate bottom-contacts (BGBC) structure

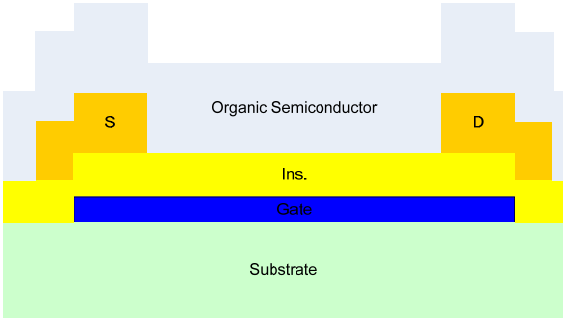


figure 8: bottom-gate bottom-contacts structure (BGBC)

The BCBG topology is the most convenient topology from the industrial standpoint because makes it possible to obtain both a better alignment and sufficiently small structures. In fact, this is the topology on which the research it is most concentrated because it allows manufacturing process on flexible substrates and enables device's printing workflows.

It's also worth of notice that, except particular cases, Top-Contacts devices (TC) have been reported to offer a lower contact resistance than their Bottom-Contacts homologous (BC). This behavioral asymmetry in contacts is principally bound to the

deposition process of the OSC. In fact, electrical and structural properties of the semiconducting film can change if deposited on a metal surface or not. As an instance, theoretical and experimental studies [8][9] prove that a gold deposition on pentacene shows traces of metal diffusion in the OSC film reducing the electrical potential barrier at the contact-channel interface.

2.4 Organic conductors and channel semiconductors

At a first glance, a material's conductivity is proportional to the product between the concentration of free charge carriers and their mobility in the abovementioned material. The physical parameters that drive such charge density are summarized as follows:

- The thermally-activated intrinsic mobile charge population in the material (depending on the temperature T and the bandgap energy E_g);
- The extrinsic carrier population due to a wanted/unwanted doping of the material;
- The eventual presence of an optical excitation;
- The Field-Effect;
- The charge injection;

Nevertheless, it's necessary to take into account the link between the charge mobility and the following factors:

- Charge transport phenomenons;
- The presence of charge traps;
- The molecular order of channel semiconductor

Also for these reasons the Organic Electronics world is always changing in the quest for the optimal combination among the virtually unlimited mixes between organic conductors and their dopants which as an instance can change a low-conductance polymer (in common

polymers conductance are typically in the order of $\sigma<10^{-5}$ S/cm) in a doped conductor (30 S/cm) as many works report.

2.4.1 Patterning and technology-related issues for channel films in OTFTs

One of the major issues which become relevant when switching from the study of a single OFET device to the realization of a working circuitry for a given application is the patterning of the organic materials when employed as gate dielectrics but principally as channel semiconductors. In fact, elevated On/Off ratios and reduced off-currents can be obtained if one is able to break the undesired conducting paths between semiconductor zones outside the active area in the OTFT.

Such patterning process is delicate for many reasons. In fact, because of their nature, organic films properties are damaged by the exposure to standard patterning processes where the adoption of solvents, wet and dry etchings and the irradiation technologies in the regions where active and dielectric areas have to be defined. That's why intrinsically-additive technologies, where a subsequent patterning becomes unnecessary, like in the Ink-Jet Printing case (IJP) are even more studied, appreciated and employed.

Anyway, because of the feature sizes reached by conventional optical patterning methods applied to inorganic electronics efforts in the direction of applying them also to organic materials have been encouraged and done. As an instance, we can talk about pentacene patterning. Pentacene has been for a long time attractive and studied because of its characteristics of high mobility (as a p-type semiconductor) and environmental stability; for these reasons it is worldwide known to be one of the major candidates for the fabrication of industrial-scale p-type OTFTs. Then, pentacene patterning has become also a relevant issue.

In the technique we're going to cite next, a chemical precursor of pentacene is solution-processed and deposited (solution-processing is one of the most interesting alternatives to the vacuum processing of OSCs because of it is extremely less expensive and scalable than thermal evaporation and other processing technologies). The channel

region is patterned by the utilization of photochemical reaction by inducing the polymerization of the zones to persist by means of UV irradiation through a photolithographic mask [15]. In figure 9 the process steps and details are shown by the reference Authors.

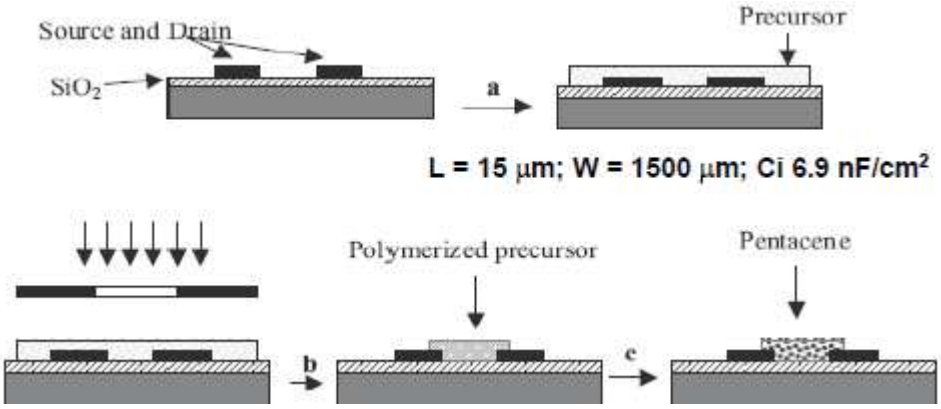


figure 9: process flow-chart of the patterning techniques adopted for pentacene OTFTs in [15]

After the removal of non-polymerized film regions, a subsequent thermal annealing changes the precursor in pentacene molecules. Electrical performances of obtained OTFTs are acceptable for a bottom-contacts OFET (~ 0.02 $cm^2/V*s$) even if they are about one order of magnitude below the common devices deposited in ultra-high vacuum by thermal evaporation. On/off ratios for I_D were also acceptable ($I_{on}:I_{off} > 2*10^5$).

Channel geometries and other patterns showed to be good also on the micron-scale as the Authors showed in figure 10 by making optical microscopy.

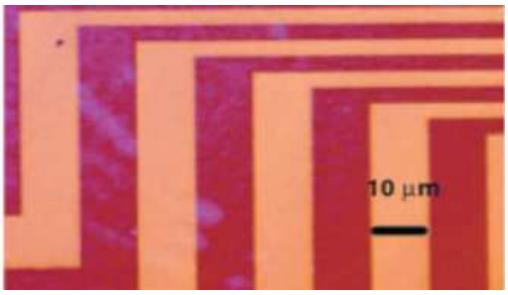


figure 10: optical imaging of micrometric structures obtained in [15] by local optical polymerization of pentacene precursor films.

In bottom-contacts structures, it is also possible the definition of the channel island by means of processes based on Self-assembled Monolayers (SAM). Such processes act by preventing the adhesion of the channel material to the substrate outside the active surface. In particular it is interesting to consider the process reported in [10] because Authors remarked that it can be useful to break the technological limits, mainly in terms of resolution, which printing techniques and conventional equipments introduce in OTFT downscaling. In a referred work [10], a substrate having S and D pre-patterned structures has been treated with OTS (octadecyltrichlorosilane) to create a low-surface energy monolayer on the top of the gate dielectric. Then the OTS monolayer in the device's channel has been irradiated in the DUV (deep UV) spectrum to make it removable because of the photochemical reaction which happens in such conditions. By choosing as channel material the 2,8-difluoro-5,11-bis(-triethylsilylethynyl)anthradithiophene, also known by its acronym, diF-TESADT, the Authors of the cited contribution have been also able to reduce the contact resistance by pre-treating the source and drain surfaces with a SAM made by pentafluorobenzenethiol (PFBT) and also obtaining self-aligned structures (see figure 11).

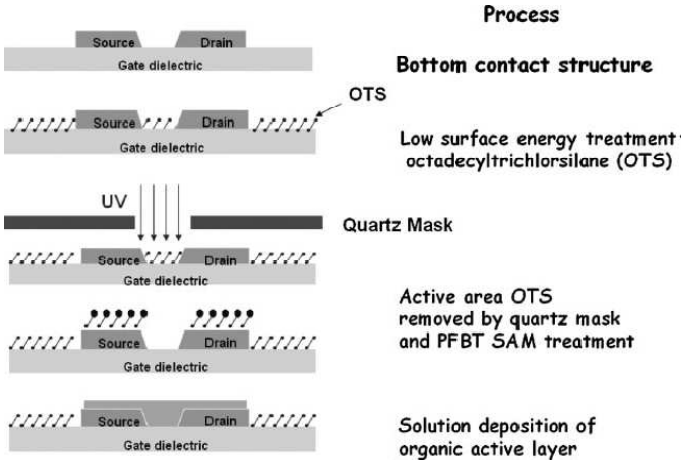


figure 11: Non-Relief-Pattern lithography (NRP) developed in [10]

NRP lithography allowed the realization of OTFT-based circuitries with fully defined islands and charge mobilities comparable with amorphous silicon (aSi) about 0,12cm^2/Vs and on/off ratios higher than 10^5 as one can state from figure 12.

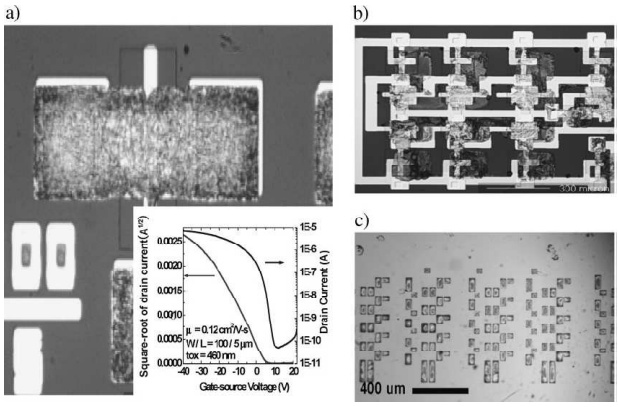
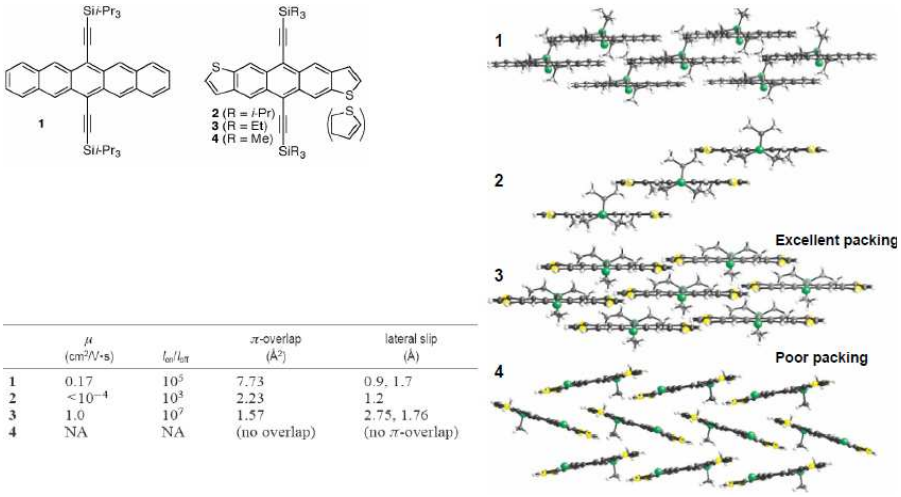


figure 12 OTFT islands realized by means of photochemical pattering and lift-off of a self-assembled monolayer.

2.4.2 Solution processing and structural order

As we already mentioned, one of the other needs which arise with increasing importance is to adopt materials that are deposited from solution phase and then avoiding vacuum deposition processes

and other techniques which are inherently expensive, difficult to maintain and scale-up and down. For this reason, as an instance, starting from promising molecule pentacene (or other acene) through a process of molecular functionalization, Anthony and others [16], obtained high hole mobilities in field effect transistors thanks to the high molecular order which the interaction of the functional groups added to pentacene imposed to the molecules of the material deposited (see figure 13).



	μ ($cm^2/V \cdot s$)	I_{on}/I_{off}	π-overlap ($Å^2$)	lateral slip (Å)
1	0.17	10^5	7.73	0.9, 1.7
2	$<10^{-4}$	10^3	2.23	1.2
3	1.0	10^7	1.57	2.75, 1.76
4	NA	NA	(no overlap)	(no π-overlap)

figure 13: comparison between OFET devices performances obtained in functionalized pentacene in relationship to ordering characteristics of modified molecules deposited films [16].

This depends on the degree of packing and order of the molecules and, therefore, on how the π orbitals overlap along the channel direction.

The goal of processes of functionalization of small molecules for organic semiconductors is to insert functional groups and to use solution processing allowing crystalline structures to self-assemble into lattices increasingly extended thus improving the order and the mobility and reducing the amount of defects.

An example of this is given by the study of Garnier on a still widely used class of oligomers (thiophenes)[17]. Authors attempted the formation of films with high mobility and, therefore, higher order

factor analysing, in particular, the hexathiophene (sexithiophenes) by means of XRD (X-Ray Diffraction) characterizations.

2.4.3 High performance n-type materials in OTFT processing

Studies on thiophenes (by Garnier et Al.) [17] have been also analyzed and enriched by Facchetti and Marks through the insertion of additional functional groups in the aim of reducing the energy levels of HOMO and LUMO (Highest Occupied Molecular Orbital / Lowest Unoccupied Molecular Orbital) of these materials [18] and thus to make possible their operation as semiconductors in n-channel TFTs (*n-TFT*).

In the referred studies, the best results were obtained on a standard topology (SiO_2 dielectric on a silicon gate, gold contacts underneath the channel) with the DFH-4T deposited on an heated substrate at temperatures T> 60 ° C. Device exhibited a mobility of 0.24 cm^2 / (V *s) and on/off ratios of 10^7.

In further works, other analyses and improvements have been obtained by means of the optimization and characterization on the molecular scale [19][20] by studying the variation of the electrical characteristics of films at different deposition temperature reaching outstanding results for such devices: $\mu_{DFHCO\text{-}4T}$ = 0.6 cm^2/Vs (n-type), $I_{on}/_{off} > 10^7$, V_T = 10V).

Since the characteristics of the interface and the deposition process have to be considered a key factor in device's operation, in other cited studies, the mobility, threshold voltages and ratio on / off are compared versus the type of dielectric, the deposition conditions materials, etc. [21] to investigate the link between device processing and measured performances. Because of the availability of a plethora of OSCs having good holes transport properties, many efforts have been concentrated on the achievement of OSCs having enough n-type conduction capabilities to be employed as channel materials in n-TFTs in enhancement operation (this operation mode is the only possible to achieve channel charge modulation in TFTs because of the lack of the possibility to perform in the inversion mode). As we told n-type

materials in OTFTs are a basic requirement in the realization of complementary logic-based or transmission-gate-based circuitries.

Besides Facchetti's works, it's necessary to cite some first fundamental contributions on phtalocyanines (which are p-type materials). In fact, after chemical molecular modifications by introduction of metallic substituents, it has been proved [22] that such phtalocyanines (since now: PC) are capable of good n-type mobilites as the referred work says. In that case, channel materials were deposited by sublimation in a vacuum chamber like other small molecules. In the same publication [22] it has been shown that modified PCs, similarly to other small molecules have performances strictly dependent from film morphology which depends from substrate temperature during the deposition (this factor is in fact able to govern the nucleation process at substrate-gas interface in the vacuum chamber during the evaporation).

As the inset in figure 14 says, thermal heating of the substrate holder can improve greatly the performances of the referred n-type OTFTs.

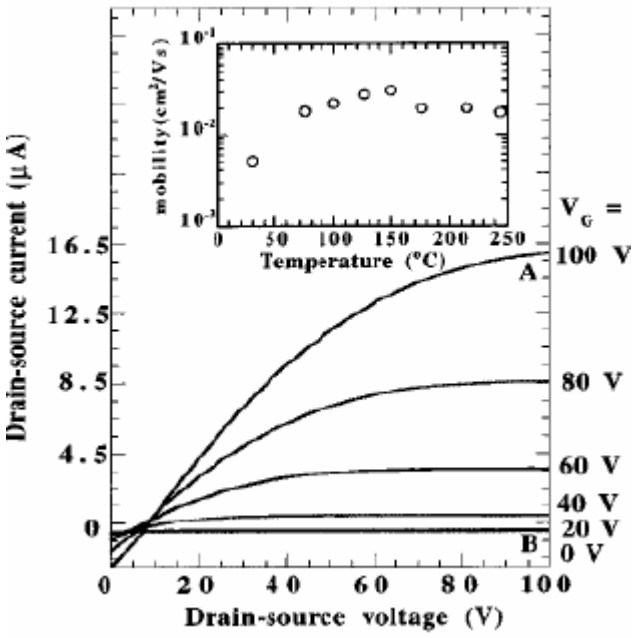
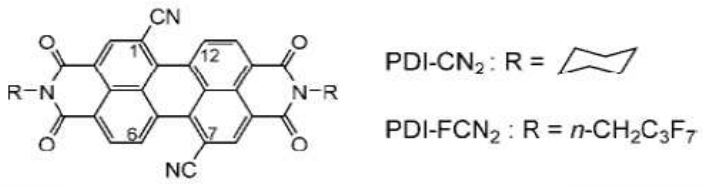


figure 14: in the inset, the dependance between deposition temperature and phtalocyanine n-type mobility as reported by Bao et al. in [22]

In literature results, n-type OSCs-related issues have been analyzed by studying the electrical characteristics obtained in OTFTs by utilizing different molecule's modifications [23] and remarking in some cases ambipolar operation regimes as in [25]. One common factor to a wide class of n-type OSCs is the poor environmental stability of such materials. In fact, in many referred works about n-type OTFTs, electrical characterizations have been done in controlled atmosphere chambers or in vacuum to prevent the interaction of such semiconductors with oxygen which is promoted because the low electron affinity of such materials (the LUMO level is close to the vacuum level).

Research studies in this direction have led to the synthesis and development of special kinds of Perylenes (PDI-FCN_2 etc.) by Facchetti, Wasielewski et al. in 2004 [26] which have exhibited good air-stability performances opening the way to further studies in this sector showing electron mobilities close to the ones obtained for benchmark p-type OSCs (including pentacene). Further improvements had to be expected in terms of on/off ratios (this is a fundamental factor in the reduction of static dissipation in logic gates and drivers [27]). figure 15 shows the chemical formula of referred perylenes in literature papers [26] and mobility values obtained.



Compound	λ_{abs} [nm][a]	λ_{em} [nm][a]	$E_{(1)}$ [V][b]	$E_{(2)}$ [V][b]	μ [$cm^2 V^{-1} s^{-1}$]	I_{on}/I_{off}
PDI-CN_2	530	547	−0.07	−0.40	0.10	10^5
PDI-FCN_2	530	545	+0.04	−0.31	0.64	10^4

[a] measured in THF (10^{-5}/10^{-6} M). [b] Measured in a solution of 0.1 M tetrabutylammonium hexafluorophosphate (TBAPF_6) in THF versus SCE.

figure 15: n-type perylene derivatives in OTFT fabrication. Chemical formula and device's performances as shown in [26]

2.4.4 Channel anisotropy

As result of structural characterization studies of organic materials with high crystallinity, the transport properties linked to the have been related to the molecular order of channel layers and to direction and orientation of the current density vector ($\underline{j} = \sigma\underline{E} = qn\mu\underline{E}$) when compared to the angle that meets the individual molecules of the semiconductor. From this point of view, highly anisotropic features were found in efficiency of transport as demonstrated in his studies about P_3HT (Poly (3-hexylthiophene)) by Sirringhaus et al. [28] conducted together with R. Friend in 1999 as shown in figure 16.

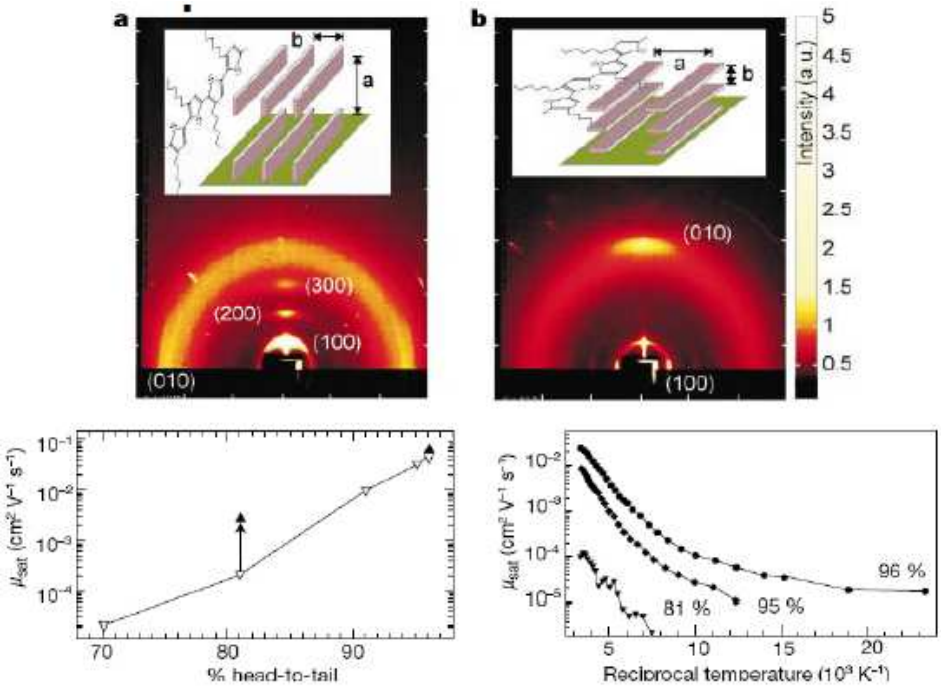


figure 16: anisotropy in charge transport shown in P3HT investigated by X-ray Diffraction experiments in [28].

2.5 Dielectric materials and surface optimizations

It is clear that the concentration of mobile charge induced in the channel of a FET by the gate field depends on the type of dielectric (dielectric constant) and its thickness, in particular, for an n-FET, in first approximation:

$$Q_n = q*n(x, V_G)*t_{ch} = C_{ins}*(V_G-V(x))=(\varepsilon_0\varepsilon_r/t_{ins})*(V_G- V(x))$$

where Q_n is the charge induced in the element of the channel at abscissa x, n is the carrier concentration, t_{ch} is the thickness of the channel, V_G is the gate voltage referred to source and $V(x)$ the voltage at the abscissa x evaluated from the source contact to the channel when the gradual channel approximation is supposed. In the end, t_{ins} is the thickness of insulator material and ε_r its dielectric permittivity.

Then, if we point the attention to such material, it is required that gate insulator material should have in the first instance:

- High dielectric strength
- High dielectric constant
- Possibility to be processed in thin films and pinhole-free
- Good morphologies: extremely smooth, without bumps and undulations
- High adhesion to the underlying layer

Another fundamental aspect is the nature of the interface between gate insulator and the semiconductor which is capable of controlling the morphology, microstructure, and most of the transport properties of the active material, by its superficial energy.

Taking into account the above considerations, it appears clear why there has been an intense scientific production about studies of the role of gate dielectrics and still much work has to be done.

An overview of the increased use of insulators in the organic FETs is provided in the review published in Advanced Materials by Facchetti et al. [30] where such materials are divided into four categories:

- Inorganic Materials
- Polymeric dielectrics
- Layer assembling

- Self-assembled monolayers (SAM)
- Multilayers (SAMT)

- Hybrid materials

2.5.1 Surface treatments on SiO_2 and other relevant dielectrics

SiO_2 is traditionally one of the most widely used gate insulators in VLSI electronics and it has particularly important in the category of inorganic dielectrics. It has been also used in the world of OE (Organic Electronics) for the realization of bottom-gate topologies with gate of monocrystalline silicon normally used as benchmark gate in the study of single channel materials.

However, this oxide, in particular when grown by thermal oxidation (high thermal budget) from a slice of crystalline silicon, cannot be a relevant player for the in OE applications because of its obvious processing limitations. Furthermore, there are many organic materials that exhibit dielectric constant higher than 3.9 (ε_r of SiO2) and lower dielectric losses which encourages the application of polymeric materials in the fabrication of gate dielectric layers.

Nevertheless, there are contributions in literature on the interface between silicon oxide and the channel through appropriate surface treatments [32] especially by HMDS (Hexamethyldisilazane), OTS (Octadecyltrichlorosilane) and other Fluoroalkyltriclorosilanes obtaining an improvement of the transport of charge.

This improvement is attributable to the fact that these treatments cause a change in surface energy of the interface and force a preferential orientation of the molecules in the channel.

As reported by prof. Kobayashi and Coworkers [33], it is possible to increase several orders of magnitude both the mobility of p-type transistors made by pentacene ($C_{22}H_{14}$) and mobility of n-type fullerene-based OTFTs (C_{60}) by silicon oxide interfaces treatment.

Those two kinds of semiconductors have been employed because they represented the state of the art in performances and well reproducible and studied results.

In figure 17 the improvements introduced by state-of-the –art surface treatments in the case of n-type and p-type OFETs fabricated on a SiO_2 gate dielectric.

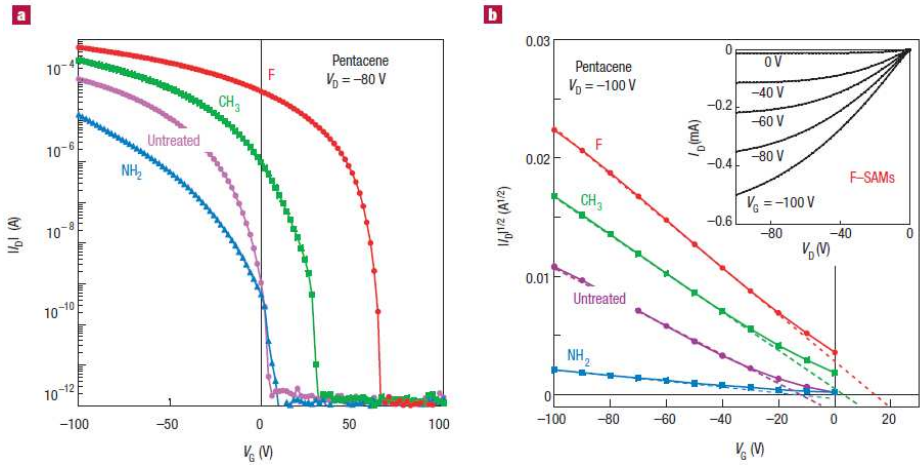


figure 17: Self-Assembled Monolayer (SAM) surface treatments on SiO_2 performed on P5 (pentacene) and C_{60} as reported by [33]

In particular, deposition treatments of Self-Assembled Monolayers (since now: SAM) made by NH_2, CH_3 and F are shown in figure 17.

Not less important is the action of the SAM on the threshold voltages of the same OTFT as shown by Kobayashi remarked before. In the abovementioned works of Veres et al. on surface treatments[32], it can be noticed a clear relationship between changes in surface energy of the insulator and the mobility obtained in P3HT (see also figure 18).

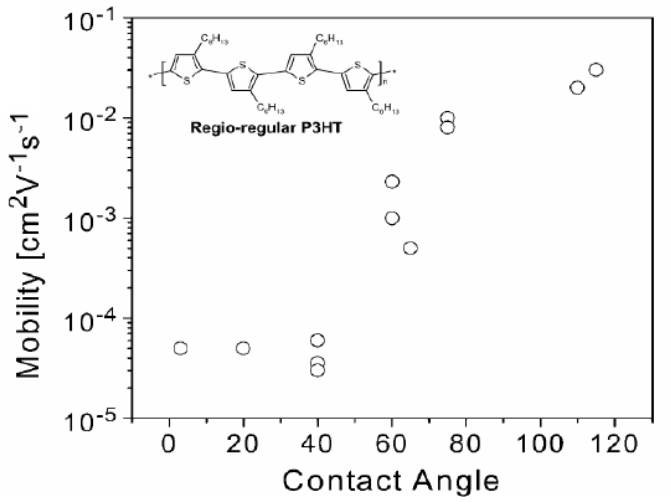


figure 18: the correlation between dielectric's surface energy and mobility is shown in bottom-gate structures in [32] by Veres et al.

These are just some examples of the capabilities of surfactant treatments in OTFT processing.

2.5.2 High-*k* dielectrics

Beyond interface properties, the use of a insulator having high dielectric constant ε_r (namely: high-*k* dielectric) is a good method to obtain operating voltages and logic levels sufficiently low to be compatible with the design rules which have to be obeyed to meet the basic market requirements in terms of power consumption and speeds.

As an instance, layers of materials based on metal oxides such as $Ba_xSr_{1-x}TiO_3$ obtained by magnetron sputtering, have showed good results in terms of mobility μ_p in pentacene that combined with a k (another symbol used to indicate ε_r) of 16, have allowed to obtain operating voltages around 5V and the threshold voltages below 1V as reported by Dimitrakopoulos on "Science" (see figure 19).

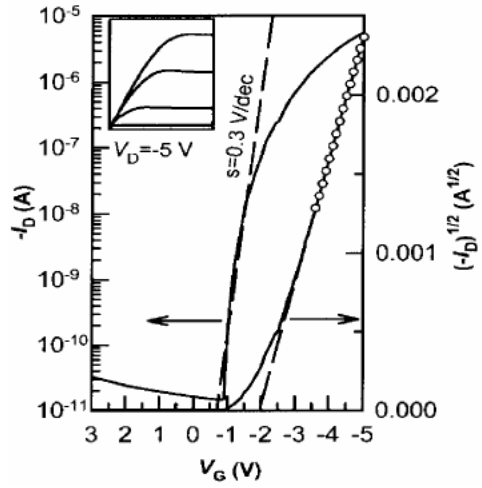


figure 19: OFET trans-characteristics having a gate dielectric made by $Ba_xSr_{1-x}TiO_3$ oxide as reported in [34]

Recent results (see figure 20), show a cerium oxide can been employed as a dielectric to further increase the field-effect as reported in [35]:

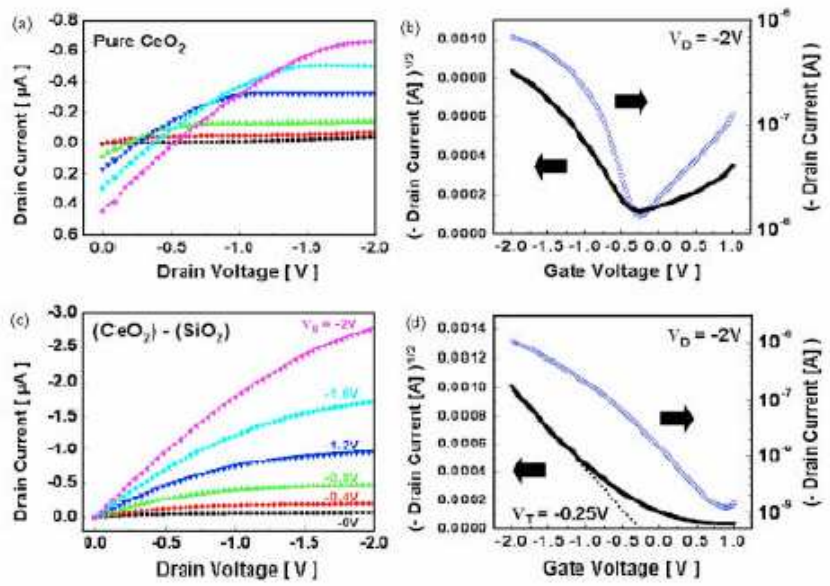


figure 20: Cerium oxide optimization reported in [35]. Gate leakages are reduced by the adoption of a CeO_2-SiO_2 in dielectric film fabrication. Mobility performances are outstanding as well.

As figure 20 shows, CeO_2 is characterized by high gate leakage currents as also figure 20 and figure 21 show which can be partly reduced by performing a further passivation by depositing a SiO_2 film on the top of the Cerium Oxide film.

More generally, it is given in the literature a more complete picture of the performance of inorganic dielectrics used in OTFT (for convenience we quote the chart in figure 22).

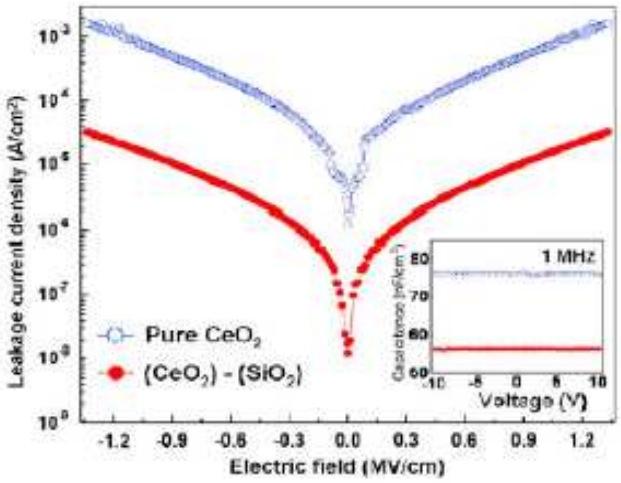


figure 21: gate leakages plots in [35]. The add of the SiO_2 layer reduces static gate leakages by two orders of magnitude.

Dielectric	Method [a]	D [nm]	C_i [nF cm^{-2}]	k	E_B [MV cm^{-1}]	Semicond.	μ [cm^2 V^{-1} s^{-1}]	I_{on}/I_{off}	Year
BZT	sputt.	122		17.3		Pentacene	0.32	10^5	1999
BST				16		Pentacene	0.4–0.5		
Si_3N_4				6.2		Pentacene	0.6		
Ta_2O_5	anodiz.	70		23	4–5	DH-5T	~0.03		2000
						FPcCu	~0.02		
Ta_2O_5	e-beam	100	180	21	>1	P3HT	~0.2		2002
Al_2O_{3+x}	sputt.	270	22	7	~3	Pentacene	0.14	10^6	2003
Al_2O_3	anodiz.	120	60		~8	PTAA	3×10^{-5}		2003
Ta_2O_5	anodiz.	86	248	24		Pentacene	0.24	10^4	2003
Ta_2O_5	sputt.		66			PcCu	0.01		2003
SiO_x	PECVD					Pentacene	0.2–0.4	~10^8	2003
SiN_x									
TiO_2	sputt.	97	373	41	~3	P3HT	5×10^{-3}	10^2	2004
Al_2O_3		93	79	8.4	~8	P3HT	6×10^{-3}	10^2	
Al_2O_3	anodiz	~7	600–700	9–11		P3HT	$1.1–1.4\times10^{-3}$		2004
						Pentacene	0.06–0.1		
Ta_2O_5–air	sputt.			25–1		Rubrene	1.5–20		2004
Gd_2O_3	IBDA	90	280	7.4		Pentacene	0.1	10^3	2004
TiO_2+PαMS	anodiz.	8+10	228			Pentacene	0.8	10^4	2005

[a] Dielectric deposition method.

figure 22: Comparison of the performance of inorganic dielectrics in OFET structures reported in [30].

2.6 Polymeric dielectrics

It is necessary to remember that the insulating polymer have the great advantage to be deposited from solution and therefore to be cheaper than the inorganic competitors. This is one of the reasons why in OE the last purpose is to realize whole organic circuitry (fully-organic). In the above-mentioned Facchetti's review [30] is reported a table that summarizes the performance of the OTFT realized with insulating polymer (see figure 23).

Dielectric	Method [a]	d [nm]	C_i [nF cm^{-2}]	k	E_B [MV cm^{-1}]	Semicond.	μ [cm^2 V^{-1} s^{-1}]	I_{on}/I_{off}	Year
CYPEL	Cast		6	18.5		6T	0.034		1990
PVA			10	7.8			0.00021		
PI	Print		20			P3HT	0.01–0.03		1997
PVP-CP	SC	260	~12	3.6	2–3	Pentacene	2.9	10^5	2002
PVP-CL		380	~ 2	4.0	1-2		3.0	10^5	
GR	SC	>1000	0.43–4.97			6T	~0.006	~10^2	2002
						DH-5T	~0.04	10^2–10^3	
						PcCu	~0.003	~10^2	
						Pentacene	~0.1	10^3–10^5	
CYPEL	SC	1200	8.85	12		P3BT	0.04		2004
PVP		900	5.59	5			0.0002		
PVA		500	17.8	10			0.03–0.003		
Polynorb.	SI-ROMP	~1200	~3			Pentacene	0.1–0.3	~10^2	2004
PVP-CL	Cast	600–700		3.5–5.4		Pentacene	~0.25	~10^3	2004
nanoTiO$_2$									
BCB	SC	50	235		>3	TFB	~ 0.0003	~10^4	2004
CPVP-C$_n$	SC	~15	~300	~6	3–6	Pentacene	0.1	~10^4	2005
CPS-C$_n$		~15	~225	~3	3-6		0.08	~10^4	

[a] Dielectric deposition method.

figure 23: Polymeric Dielectrics and OTFT performances [30]

2.6.1 Composite dielectrics

The improvement of static performance of the OTFT can be achieved also by means insulating composite materials. In [31] it is shown the comparison between a pentacene based OTFT device with

channel and gate in Pedot:PSS with a BGTC structure (see figure 24) with PVP (poly-4-vinylphenol) dielectric and the same material in which they are dispersed TiO_2 nanoparticles (as is known, the TiO_2 is a high-k dielectric, k = 80 [24]).

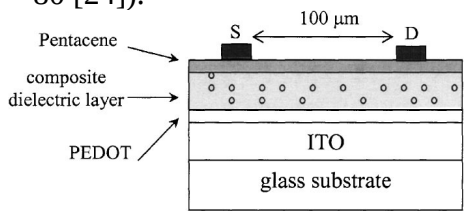


figure 24: The OTFT structure with insulator composite as shown in the Wilk's paper [24]

To quantify the difference in the device behaviour it is important consider the output characteristic of such kind of TFT (see figure 25).

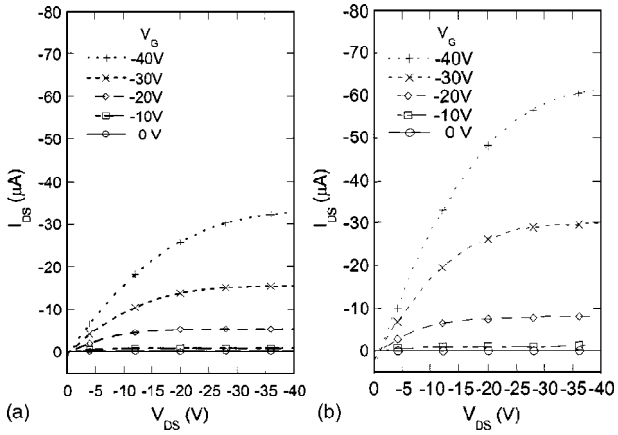


figure 25: the increase in the OTFT transconductance due to the use of nanocomposite dielectric with high-k materials [24]

A qualitative and quantitative explanation of this optimization is to be found clearly in the increase of dielectric constant of the film obtained as shown in figure 26 for different concentrations of nanoparticles.

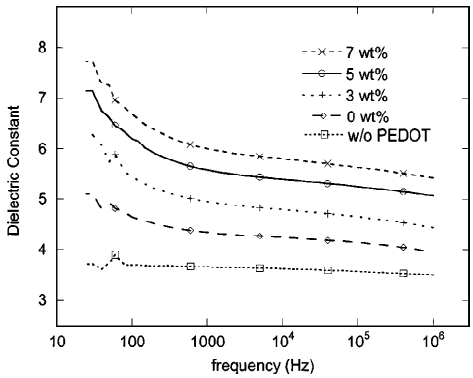


figure 26: C/f measurements on PVP dielectric films at different TiO_2-NP weight concentrations [24]

In the use of composite materials is crucial to ensure that the electrical insulation properties of the gate are preserved by the presence of dispersed particles. This is a necessary condition, together with the reduction of interface traps by surface treatment, for the realization of high-performance transistors. An example of this kind of study can be supplied by Wang, Lee et al. [29]. In this paper, the authors, studied the leakage current as a function of TiO_2 weight percentage dispersed in polyimide matrix (see figure 27).

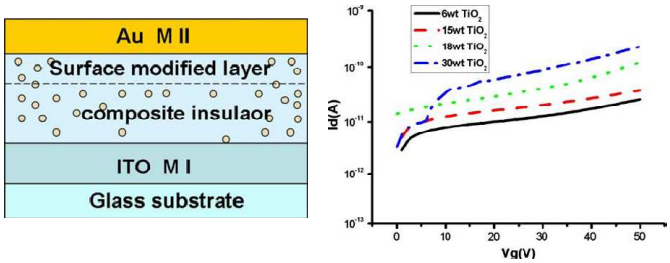


figure 27: current through the nanocomposite dielectric gate [29]

Moreover, the devices transcharacteristics are compared versus the concentration of NP showing a threshold in the worsening of the on-off ratio (figure 28).

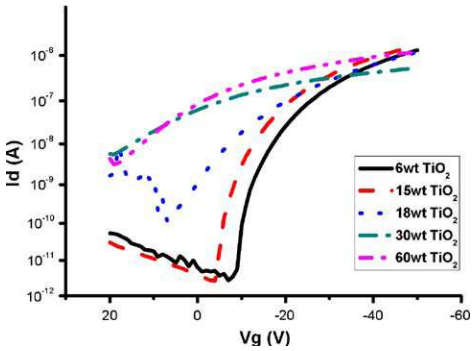


figure 28: Pentacene based OTFT transcharacteristics changing the titanium oxide nanoparticles in the dielectric polymeric matrix [29].

2.6.2 Self-assembled dielectrics

Self-assembled (SA) films can be used to realize an extremely thin (2 to 6nm) and virtually free of defects gate insulator obtaining, at the same time, dielectric strength of the order of tens of MV/cm as shown in the table of figure 29.

Dielectric	d [nm]	C_i [a] [nF cm^{-2}]	E_B [MV cm^{-1}]	Semicond.	μ [cm^2 V^{-1} s^{-1}]	I_{on}/I_{off}	Year
OTS	2.8	153	9–12	6T	0.00036	~10^4	2000
PhO-OTS	2.5	900	14	DE6T	0.2		2004
				Pentacene	1.0	~10^4	
SAMT-I	2.3	400 [1100]	5–6	DH-6T	0.04	~10^3	2005
SAMT-II	3.2	710 [2500]	6–7	DH-6T	0.02	~10^3	
SAMT-III	5.5	390 [760]	6–7	DH-6T	0.06	~10^3	
				6T	0.002	~10^3	
				DFHCO-4T	0.02	~10^3	
				FPcCu	0.003	~10^2	
				DH-PTTP	0.01	~10^2	

figure 29: evolution in the state of the art for the self assembled dielectrics [30].

Among the characteristics of the SA dielectrics, there is of course the possibility to obtain high gate capacitance, but also the advantage of being able to be realized by means of solution process, therefore with low complexity and cost (dipping, spin coating, IJP, etc.). For these and other reasons, they have attracted, over the years, great interest in the scientific community reaching quite encouraging results. For example, in the case of pentacene transistors, at this point

it is important to remember the Halik and Klauk paper published in 2005 on Nature [36] in which a SAM dielectric of only 2.5 nm is inserted in a benchmark structure, bottom-gate top contacts, made on silicon wafers.

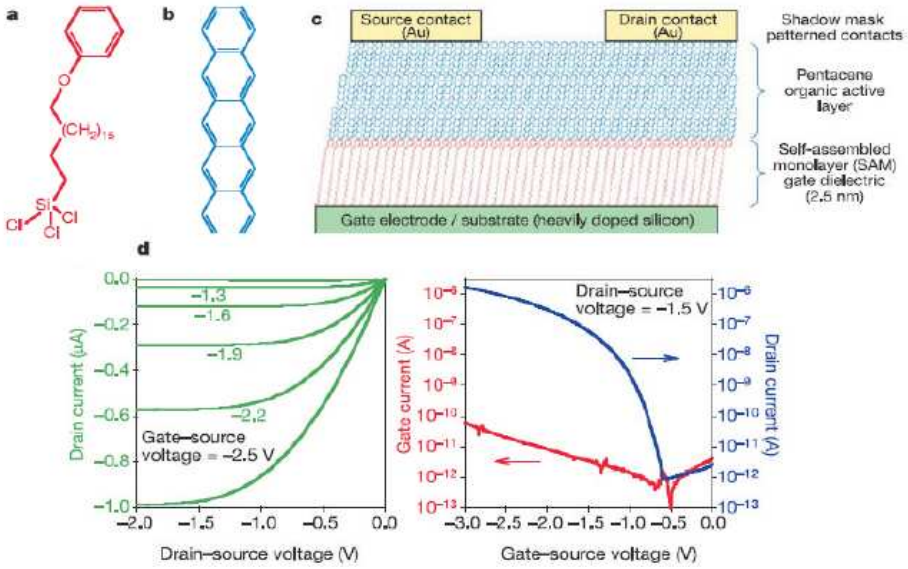


figure 30: Performance of an organic transistor made by the deposition of a SAM dielectric on which are grown by vapour phase three molecular layers of pentacene thin film [36].

The figure 30 shows the structure of the transistor made by the SAM technique to which we are referring. The mobility obtained with this kind of devices is of the order of $1cm^2/V*s$ the on/off ratio about 10^6 and operating voltages in the active region less than 3V.

The natural evolution of SAM dielectrics, as for the above mentioned high-k insulator, is the multi-layer structure (see figure 31): we will refer to these systems with a more properly name, Self-Assembled Multilayer (SAMT) [37]. These dielectrics exhibit very high gate capacitance (up to $2500nF/cm^2$) and, like the SAM, may be deposited from solution on flexible substrates in order to realize both n-type and p-type transistors [37]. The on/off ratio is still low (about 10^3) as often happens in the case of SAM.

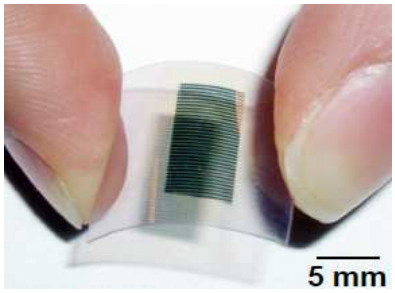


figure 31: OTFT realized by means SAMT dielectric on ITO gate and on a Mylar substrate [37]

2.7 Source and Drain electrodes in OTFTs

Strictly thinking to the materials involved in the realization, the performance of an organic transistor depend, and of course, not only from the properties of the semiconductor channel and of the gate insulator, but also from the physical-chemical properties of the source and drain contacts that are responsible for the injection of carriers modulated by the effect of the field within the channel region. In particular, it is clear those technologically attractive electrodes, in order to minimize the ohmic losses, have a high conductivity and at the same time they are characterized by a low contact resistance (R_s) which is often a critical factor in OFET operation (reduces the drain current).

In addition, the interface between the electrodes and the channel is comparable to a metal/semiconductor junction and it is necessary to pay particular attention to the electrical characteristics of the resulting device realized by the junction itself. The contact should have an ohmic characteristic and this goal is achieved depends on the barrier between the energy levels related to the contacts and the channel.

The reduction of this barrier is obtained, for a given semiconductor, by choosing the appropriate material with which realize the Source and Drain, as well as by the adoption of process improvements and interface treatments. Equally important, as regards the feasibility of a particular transistor and its integration in complex logic, are the possibility to realize a patterned structure of the

electrodes with high aspect ratio and the possibility to implement it on large areas.

Realization cost and environmental stability complete the main technical specifications associated with the electrodes in the OTFT devices.

In the following paragraphs we will analyze different kind of materials that have been already investigated in the literature in order to care about the specifications that have been discussed until now.

2.7.1 Inorganic electrodes

The inorganic conductors are good candidates to be used as electrodes for OFET transistor, because of the wide availability and their good environmental stability, and because they have been already well characterized in the past. These materials are often easy to find and the purification process is not so difficult, in addition deposition methods are already studied and established including a good patterning capability and process reproducibility. However, they are often poorly suited to be used on flexible substrates and cannot be sustainably used in optical applications where high transparency is essential.

2.7.1.1 Metallic contacts

The metal contacts are the most commonly used materials into benchmark structures realized to study the characteristics of a single transistor placed outside of a complex circuitry, and so to study the material properties of the channel or insulator in easy way. They usually have the advantage of a high conductivity and for this peculiarity they are used as good interconnection layer especially for large area microelectronic applications.

The wide number of metals available in nature and the wide range of work functions (W_F) which they exhibit, allow us to obtain quite easily ohmic contacts. In particular, it is expected that the boundary region between the semiconductor channel and the contact, behaves, as already mentioned, in the form of Schottky junction in which, obviously, the lower is the potential barrier between the two

materials, the higher is the current passing through the junction itself. Thus, for p-type transistor, the contact is much better as the W_F of the contact approaches the semiconductor HOMO level (in which we would like to inject holes).

Many p-type materials have HOMO levels that require, for the adequate holes injection, high work-function electrodes to minimize the interface barrier. For example, for p-type pentacene based transistors, it will be sufficient to use metals such as gold, nickel, platinum, etc. to realize the appropriate source and drain contacts (see table 1).

Metal	W_F(eV)
Au	5.10
Pt	5.65
Ni	5.15
Co	5.00
Cu	4.65

table 1: some metals having high work-function

The issues related to the energy bands alignment between Source/Drain and semiconductor were extensively investigated in the literature for many materials combinations.

In figure 33, it is shown a diagram about the situation of the energy levels that exists between a gold contact and the HOMO level of a pentacene film, as described by Horowitz in an interesting paper [7].

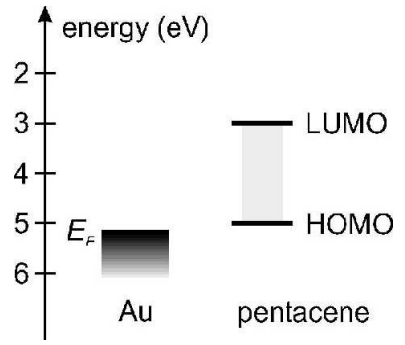


figure 32: band diagram for a Au/Pentacene junction [7]

For instance, the gold Fermi level is approximately W_F=5.10 eV and the pentacene HOMO level as estimated in [7] has to be approximately 5.2 eV, the barrier should appear extremely limited (0.1 - 0.2 eV) and the quality of the contact is theoretically optimal. However, in practice, the contact resistance is much higher than expected and exhibits a non-ohmic contact behaviour. This is also confirmed by PES (Photo-Electron Spectroscopy) measurements [38] that have shown a shift of more than 1 eV between the two materials, actually lowering the metal Fermi level as the contact has been realized (see figure 33). This was attributed to the formation of interfacial dipoles that modify the energy profile at the border of the source and drain contacts.

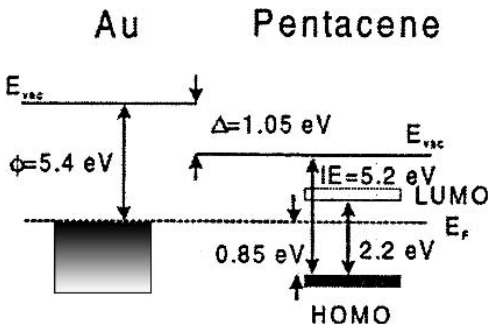


figure 33: the shift in the energy levels between gold and the HOMO and LUMO levels of the pentacene due to the formation of interface dipoles [7][38]

The effect of the barrier height at the contacts on the electrical potential profile along the pentacene channel for a gold top in-contacts (TC) OTFT has been investigated by Nakamura et al. [42] in 2005 by potentiometric measurement carried out in situ using a Atomic force microscopy technique (AFMP), see figure 34.

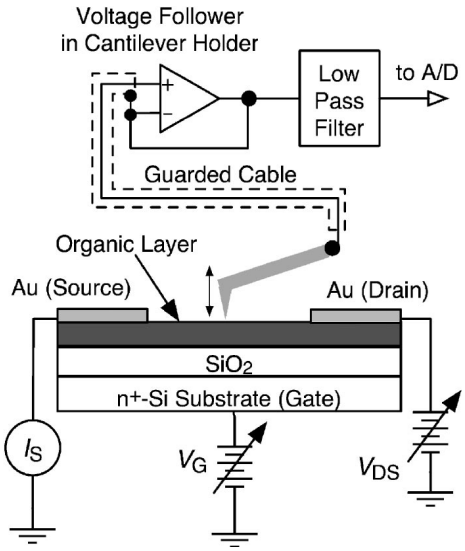


figure 34: experimental Setup during an AFMP measurements on a TC-OTFT pentacene based device as reported by Nakamura et al. [42]

In the above mentioned work [42], the surface potential of the channel for an TC-OTFT is measured by scanning with an AFM tip in both directions while the transistor is biased in active region. Close to the contacts, the sharp drop in potential V(x) confirms the presence of a Schottky barrier diode at the interface, and a consequent non-negligible contact resistance, that can be placed in the areas in which the profile shows the greater slope (see figure 35), in fact, a comparison with 2D simulations reported by Nakamura in [43], it is possible to quantify the contribution of non-ideal behaviour due to the mismatch energy and the lowering of mobility due to thermal deposition of metal through a shadow mask and to the consequent metal diffusion in the semiconductor layer.

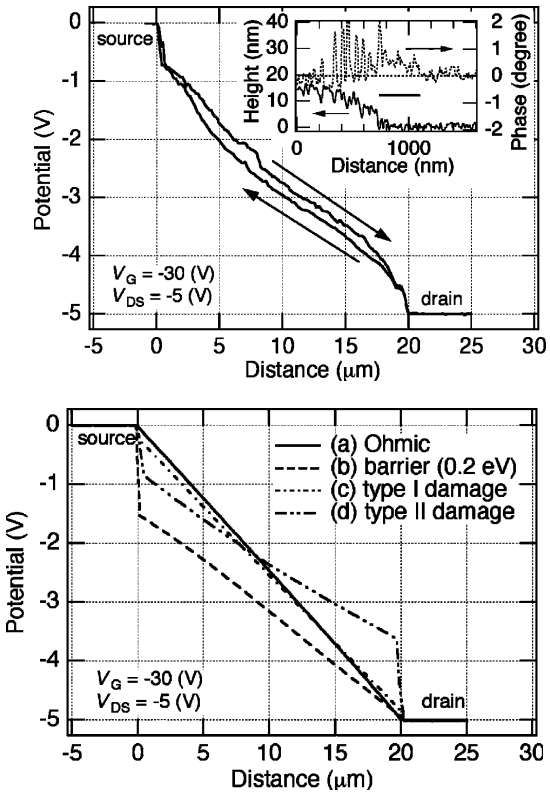


figure 35: AFMP measure on a TC-OTFT pentacene based device [42]; close to the contacts it is evident the effect of the Schottky barrier and the damage caused by the deposition of the metal contacts.

As already mentioned, it 'also important to note the reasons that cause a drastically different behaviors for the metal contacts depending on whether they are used in BC or TC topologies.

From the physical point of view, an analysis similar to the one already seen, the KFM (Kelvin Probe Force Microscopy), is also useful in this direction as shown by Puntambekar, Pesavento and Frisbie [44] in a comparison of potential profiles expressed by structures bottom-contacts and top-contacts-contacts respectively (figure 36).

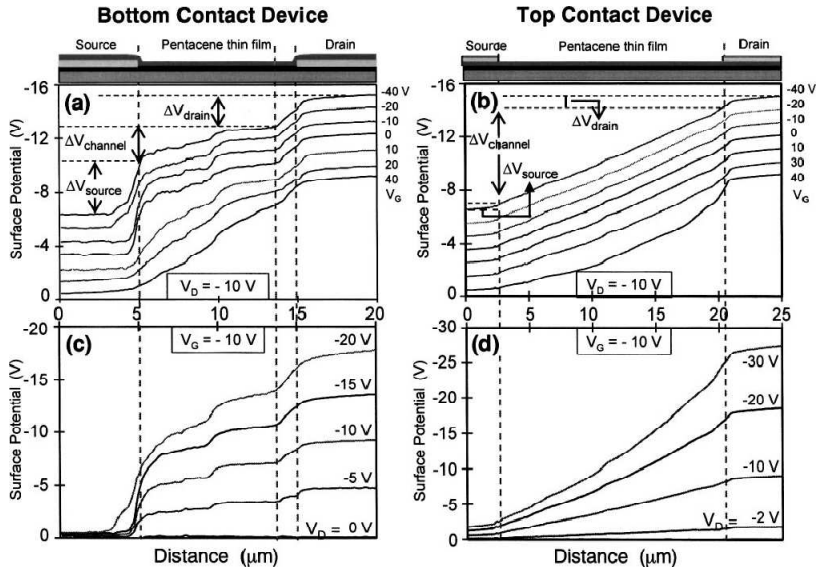


figure 36: potential profile – comparison between top-contacts and bottom-contacts architectures [44]

This helps to explain why the bottom-contacts structures (BC), if not properly optimized at the interface, typically have much lower performance in comparison with TC structure. These kinds of studies show, another time, the importance of surface treatments at contact/channel interface.

2.7.1.2 Surface treatments of metal-semiconductor interfaces

To functionalize the semiconductor/contact interface follows what already seen for surface's treatments of gate insulator. For example, in [39], the surface of Gold electrodes in an OTFT is functionalized through different treatments: thiophenol, 2-mercaptoethanesulfonic acid and thioketone (see the structure in figure 37). In table 2, these treatments are referred with numbers (1), (2) and (3).

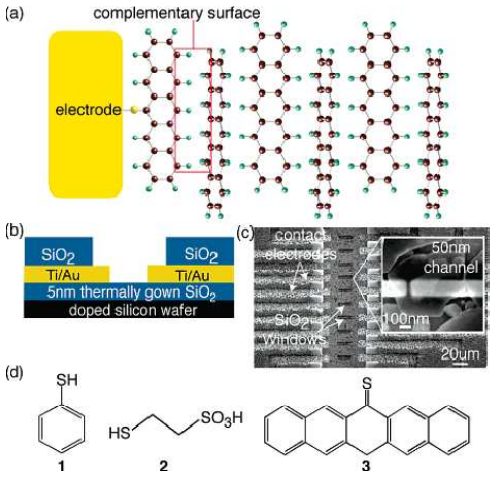


figure 37: functionalization of Ti/Au electrodes for OTFT as reported in [39]

modification	I_{ON}/I_{OFF}	μ (cm^2/Vs)	g_m (nA/V)
none	100	$1.4 \pm 0.3 \times 10^{-4}$	0.5 ± 0.1
1	50	$5.1 \pm 0.9 \times 10^{-4}$	1.3 ± 0.3
2	35	$7.6 \pm 1.1 \times 10^{-4}$	1.8 ± 0.2
3	8000	$2.2 \pm 0.7 \times 10^{-2}$	12.2 ± 1.4

[a] Values are an average of many devices (>10) with channel lengths ranging from 40 to 100 nm.

table 2: comparison of performances for OTFT with treated contacts:

1: thiophenol; 2: 2-mercaptoethanesulfonic acid; 3: thioketone [39]

From table 2, it is easy to observe that a single molecular layer (from here "monolayer") of thioketone is the best process between the three ones, improving the pentacene channel mobility of about two orders of magnitude, and giving some benefits also for I_{on}/I_{off} ratio.

Another example of surface treatment with monolayer deposition is shown in [40]: the transistor contacts are first immersed in a solution of 4-nitrobenzenethiol and then the semiconductor is deposited over them (see figure 38).

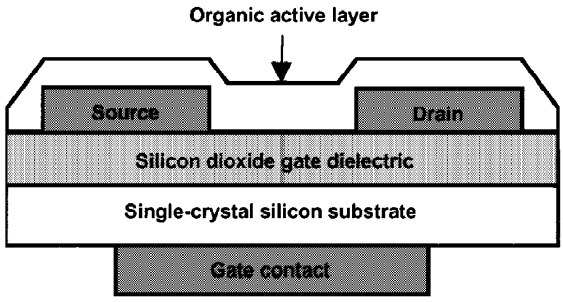


figure 38: "bottom contacts" test structure of transistor fabricated in [40]

In [40], two identical substrates with insulator and Source and Drain contacts are exposed to OTS (octadecyltrichlorosilane) in vacuum at 100°C, to improve mobility in saturation region. Just one of the two substrates follows the said treatment (see figure 39 and figure 40), giving an improvement of performances for pentacene transistor in linear region. In particular, the improvement is clear at low Drain voltages and for mobility in linear regime (0.55 $cm^2/V*s$). (Note: considering that transistor mobility is dependent from Gate voltage, the evaluation of mobility in linear regime often gives lower values than ones in saturation regime; is generally true that $\mu_{LIN} < \mu_{SAT}$).

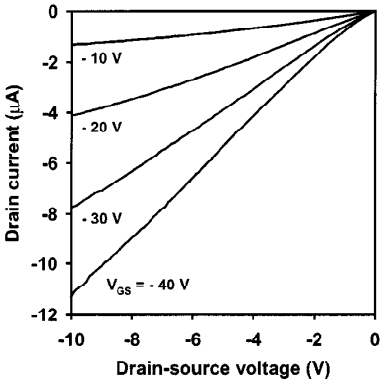


figure 39: output characteristics of transistor in [40] without contacts treatment

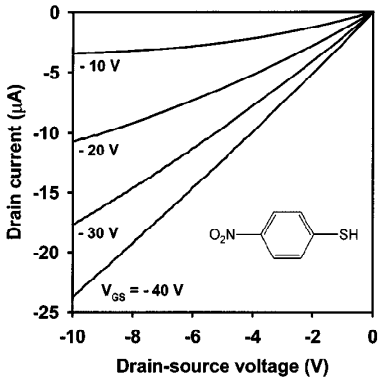


figure 40: output characteristics of transistor in [40] whose contacts are treated with 4-nitrobenzenethiol

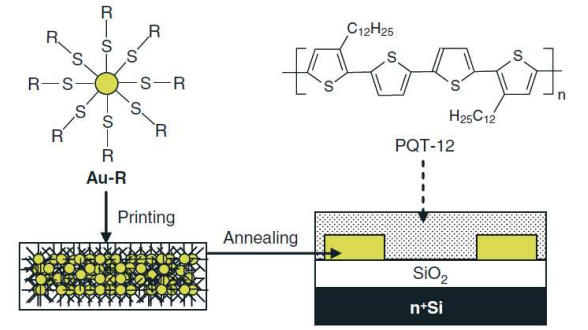
2.7.1.3 Patterning methods for metallic contacts

Given the particular topologies of devices, often organic materials (insulators and semiconductors), over which metallic contacts are deposited, could not resist a conventional photolithography process. Because using evaporation shadow-masks, without particular approaches, doesn't permit precise structures, little enough and aligned with Gate contact, literature is rich of many different methods for depositing and defining metallic contacts applying innovative processes.

In [41], Gold contacts Source and Drain for OTFT are deposited from liquid phase, applying a printing process. Technologically viewing, this solution is quite interesting, because it seems less expensive than vacuum deposition techniques or than lamination and, at the same time, more electrically efficient than polymeric conductors deposited from solution, like PEDOT:PSS and doped Polyaniline, which intrinsically show lower conductivity than metallic contacts [46][47].

An ink is made of a suspension of Gold nanoparticles functionalized with n-Buthanethiol (Au-C_4), dimensions from 1 to 4 nm. The ink is printed on a test structure of Si/SiO_2 to create Source and Drain contacts for a BC-OTFT (see figure 41). A relative low-

thermal-budget treatment turns the solution into a compact solid film (see figure 42).



Schematic depiction of printing gold source and drain electrodes using gold nanoparticle ink for a bottom-contact OTFT device with PQT-12 semiconductor layer.

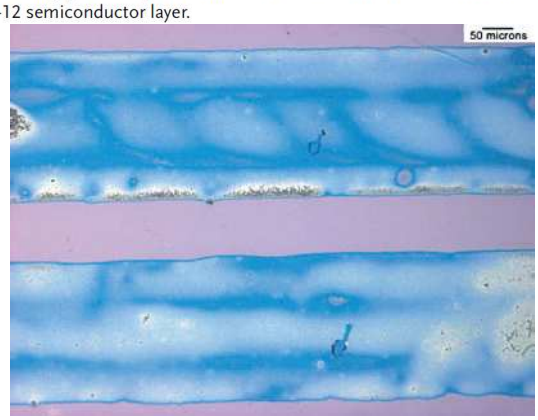


figure 41: deposition process for an ink of Gold nanoparticles, as reported by Wu et al. [41]; on the right, an optical image of an OTFT fabricated using this technique.

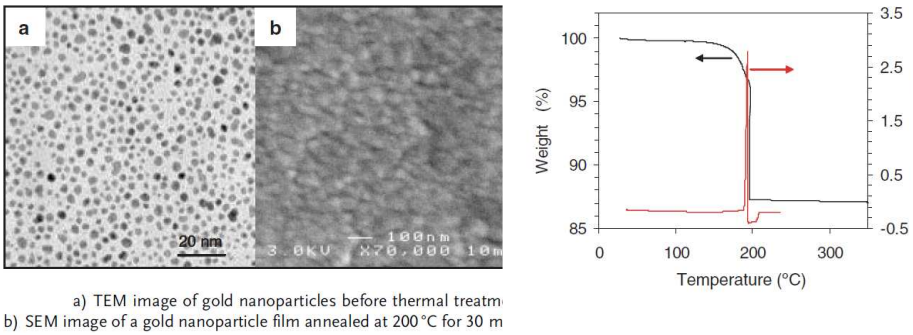


figure 42: effect of annealing process on a conductive ink of Au-NP [41].

2.7.2 Polymeric electrodes

A big limit for flexibility and transparency of organic circuits is the presence of metallic contacts and inorganic oxides. Thus, materials like PEDOT:PSS and doped Polyaniline are tested to fabricate logic circuits with OTFTs, to obtain devices with both organic semiconductor and Source and Drain organic/polymeric contacts, also because in this way printing[1] and spin-coating deposition techniques can be applied. However, these materials show high resistivity and contact resistance, and tend to create non-ohmic contacts.

2.7.2.1 PSS:PEDOT

Poly(3,4-ethylenedioxythiophene):poly(4-styrenesulfonate) (PEDOT:PSS), is a material widely employed in Organic Electronics,

[1] Printing techniques:
- Digital
  - IJP
  - Thermal
- Gravure printing (a cylindrical metallic surface presents pits which can contain very small quantities of ink to release on the substrate to print)
- Offset lithography
- Flexography

in particular in OLEDs [50][51][52] as a Hole Injection Layer (HIL), thanks its high work-function.

One of its advantages is a rather high conductivity (about 1 S/cm, as shown in [53]) and low sheet resistance. Another important characteristic is that it is water soluble, which gives the direct opportunity to use it as an ink for IJP systems, as done in [54].

Moreover, recent technological advancements have succeeded in using it for OTFTs with self-aligned contacts [55]. In this paper, published in *Nature* on 2007, authors report on an OTFT with polymeric Gate of PEDOT:PSS, applying a process called SAP (Self-Aligned Printing), already shown in [56], obtaining scalable sub-micron structures. Source and Drain contacts are produced in the following way: a first structure (for example, Source) of PEDOT:PSS is deposited through IJP and then its surface energy is reduced using a suitable process; in this way, a second structure (Drain) deposited to partially cover the previous one, doesn't wet the surface and moves at the side, forming automatically a gap to create the device channel (see figure 43).

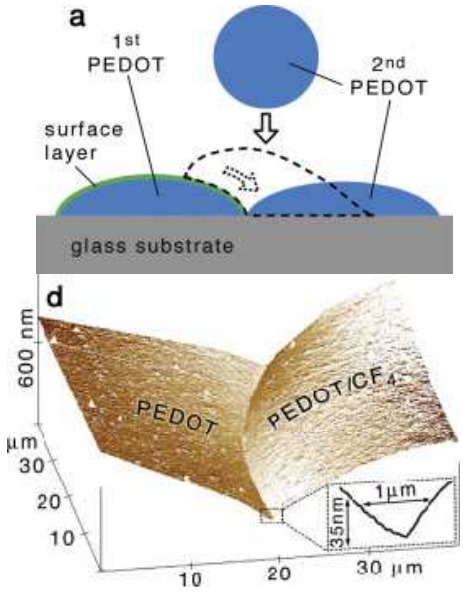


figure 43: self-aligned structures for OTFTs, with Gate of sub-micron length, are obtained modifying the wettability of a drop of PEDOT:PSS.

2.7.2.2 Polyaniline

Among the polymeric materials, Polyaniline (PANI) always had large attention, for the possibility to pattern it at photolithography quality without needing to etch material. In particular, in Gelink on APL, completely polymeric OTFTs integrated circuits are shown.

The interconnection lines and OTFTs' Sources and Drains have been produced through photopatterning of a PANI film 200 nm thick: PANI is exposed to deep UV radiation, to turn it into the much less conductive leucoemeraldine (see figure 44).

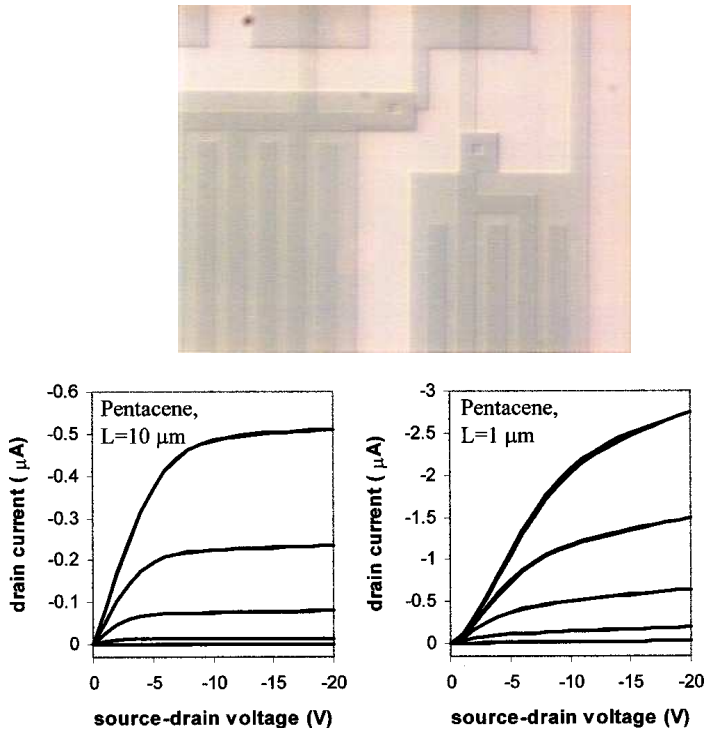


figure 44: photopatterning of PANI to fabricate a logic of p-type transistors, with nominal feature size of 1 μm, and OTFTs characteristics.

One interesting character of PANI is its qualitatively different behaviour respect to Gold when employed for contacts. In fact, as reported by Blanchet et al. in [49], the output characteristics in linear regime of a BC-OTFT using PANI contacts show ohmic trend, while the corresponding TC-OTFT acts differently (see figure 45).

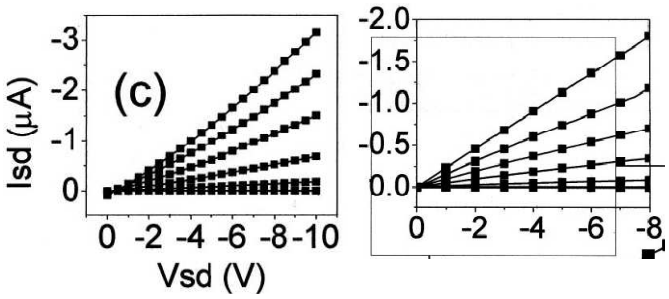


figure 45: left, output characteristics in linear regime of a BC-OTFT with PANI S and D; right, the corresponding TC-OTFT. Both devices use pentacene semiconductor [49]

2.7.3 Composite materials for Source and Drain electrodes

Composite materials, as Gate insulator and as electrodes, are one of the approaches employed to improve the OTFT performances. In paragraph 2.7.1.3, we have already seen that a dispersion of Gold nanoparticles can be applied to fabricate patterned electrodes.

Also Carbon nanotubes are quite often applied. For example, in [57], a dispersion of Single-Walled NanoTubes (SWNT) is deposited using spin-coating technique. To have contacts conductive enough to be employed in OTFTs, but not increasing the SWNT concentration beyond the percolation limit (and other important effects), authors apply the self-assembling of a matrix of poly(styrene-block-4vinylpyridine) (PS-b-P4VP) doped with $HAuCl_4.3H_2O$ and with SWNT dispersed into, to increase electrical conductivity and not reduce film transparency.

In figure 46, clear field TEM images are shown for a stabilized film (a) and at the highest possible concentration of doping (b). In (c),

an AFM tapping-mode image is presented at very low scale, to show the presence and uniformity of SWNT.

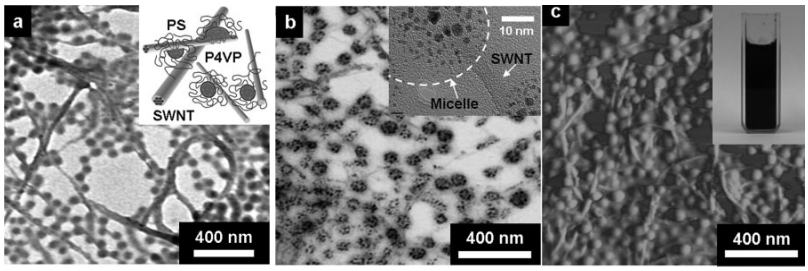


figure 46: film of stabilized PS-b-P4VP (a); the same material with the highest doping concentration (b); AFM image (c) [57]

Observing also the transmittance measurements (figure 47), these results state this kind of material is very good for fabrication of completely transparent OTFTs. Devices have been produced, with these contacts and pentacene semiconductor, through spin-coating deposition and micro-imprinting patterning.

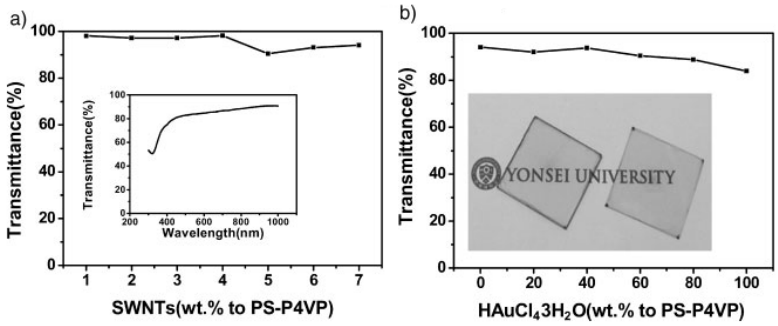


figure 47: transmittance measurements of the composite film obtained by Sung in [57]. Sheet resistance can be varied by doping; the value here applied is 6000 Ω/sq [57].

The estimated performances are: mobility of 0.05 cm^2/Vs and on/off ratio of 10^5, as can be seen from figure 48.

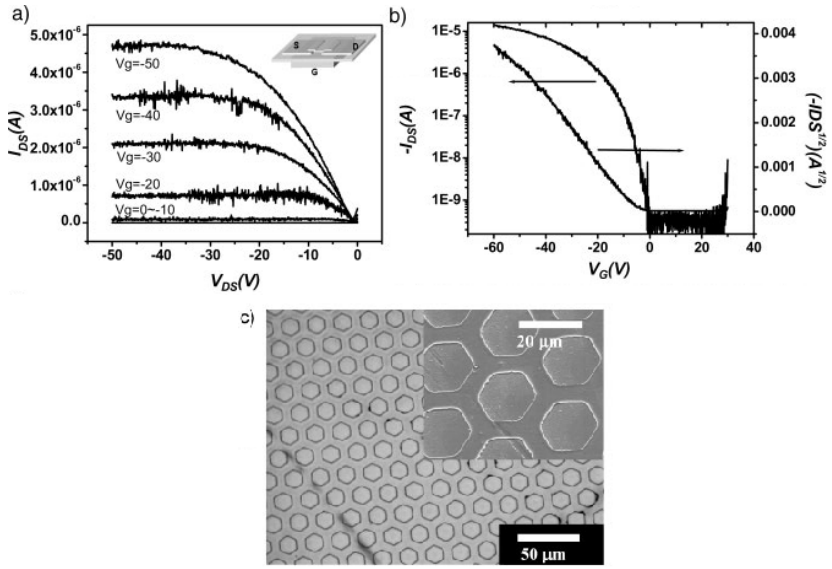


figure 48: electrical characteristics of OTFTs presented in [57], and patterning of conductive transparent film obtained using micro-imprinting

2.8 Conclusions

The development of the organic thin film transistors is evolving quickly and most of the efforts are being focused on the overcoming of the technological limits which make the employment of these devices in integrated circuits complex, in particular in large area applications (typical characteristic of flexible display).

Further efforts are invested whereas it is possible to glimpse the possibility of improvement concerning:

- Development of n-type channel materials
- Issues of structure patterning
- Issues of scaling
- Research of self-aligned processing (consequent reduction of gate overlaps)
- Static and dynamic electrical modeling
- Low-cost and high-productivity deposition methods
    - Vacuum-free deposition techniques
    - Advanced gravure printing techniques and innovative roll-to-roll systems
- Implementation of high-efficiency complementary logics
- Realization of OTFT based sensors
- Research of high environment and thermal stability materials
    - Development of passivation and encapsulation techniques
- Development of surface treatments for
    - Reducing S and D contact resistances
    - Reducing the potential barriers at contact interfaces
    - Increasing of channel mobility
    - Optimizing of the performances in linear region characteristics
    - Passivation of the gate insulators
    - Defining of the solution-deposited contacts

The research on the OE field has to face all these challenges, and more other ones, so that this new technology can assert itself and become competitive covering the market sectors left still partially unexplored by the inorganic electronic technology.

Relying on the literature information reported in the State of the Art of the present doctoral thesis and on the just exposed Conclusions, future technological guidelines have to be defined for the development of this research activity.

The guidelines are defined setting the target of integrating organic and/or polymeric and inorganic commercial materials in optimized structures in terms of electrical performances and fabrication processing.

In particular, the topological factor is a fundamental component of the future organic transistor development: as disclosed, bottom-gate (BG) architectures are particularly advisable for optimizing the channel-semiconductor interface. Moreover, at the aim of obtaining the highest profit from the patterning techniques developed in inorganic electronic and from emerging, not conventional methods, structures with source and drain contacts placed under the channel will be realized for reducing the issues related to gate-overlap, loss currents and parasitic effects due to the diffusion of the vapour-phase deposited metals towards organic polycrystalline or amorphous semiconductor.

In conclusion, the BGBC architecture appears particularly suitable for the future improvements of the presented activity. The drawback for using of this structure lies in the formation of interfacial dipoles between source/drain and channel thus increasing the contact resistance, producing potential barriers and reducing the device saturation current. At this aim, new processes will be experimented to optimize the contact-semiconductor interface putting down undesirable phenomena (injection barrier and parasitic resistances).

As the choice of commercial materials to be employed in OTFT is wide and the electrical performances in static and dynamic regimes are often correlated to technological factors, such as processing, architectural and interface physics factors, the future research will consist in using of available materials and in optimizing the structure through the study and the modeling.

Organic semiconductors, such as Pentacene ($C_{22}H_{14}$), il P_3HT (Poly (3-Hexylthiophene)) and modified PPV, such as MDMO-PPV (poly[2-methoxy-5-(3,7-dimethyloctyloxy)]-1,4-phenylenevinylene), will be inserted in planar OTFT structures. Polystyrene (PS), Polyimide (PI) and conventional photoresist (PR) films will be deposited by solution with different thicknesses and will be characterized as dielectric layers. High-work-function metals, such as gold, nickel, etc., and also organic conductors, such as doped polyaniline (for optical patterning) and PEDOT:PSS (Poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate)) based materials, will be employed for realizing ohmic contacts on p-type semiconductors.

Since the losses due to the dielectric gate are considered the main causes of the damage of the performances of MIS field-effect transistors, the static and dynamic characterizations of these structures will be performed taking into account the above-mentioned non-idealities. Analysis on the injection physics and the carrier transport of the materials employed as insulators or semiconductors will be necessary in order to study the specific issues related to different device architectures in quantitative manner. In particular, at the aim of studying and potentially improve the dielectric behavior inside FET structure, high- and low-temperature characterizations will be carried out for analyzing the modifications in desired (horizontal) and undesired (vertical) transport physics of electrical charge.

The investigation of the mechanisms correlated to these phenomena will be performed evaluating the channel carrier mobility with relation to the transverse and longitudinal electric field, to the interface microstructure analyzed by means of electronic scanning microscopy - SEM - and atomic force microscopy -AFM, to the material crystalline lattice modifications examined by X-ray diffraction -XRD, etc.

The modifications of the trap states and the free-carrier density are the crucial factors which influence the OFET electrical characteristics and they are usually correlated to UV/Visible/IR radiation effects in reversible or irreversible manner. As concerning this point of view, an analysis of the physical parameters linked to transient or permanent effects induced by the interaction of semiconductor channel layer with the light radiation and external environment as consequence of the same radiation effect (oxidation,

photolysis). In this perspective the chosen topology clearly has got a fundamental rule in the treatments of the dielectric-channel and contact-channel interfaces.

Preliminary tests will be aimed to understand the physics and the properties of the interfaces and of the employed materials in order to optimize the transport characteristics for obtaining a carrier mobility enhancement and channel region decreasing whereas parasitic effects take place.

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Chapter 3

Gate-leakages in polymeric dielectrics and layout optimization

The purpose of this chapter is to highlight the importance of the analysis of non-idealities in the static electrical characteristics of organic p-type thin film transistors (OTFTs). Such studies can improve the interpretations of the performance parameters as carrier mobility and device threshold voltage. Our investigation includes the characterization of Pentacene-OTFTs fabricated with different gate dielectrics to study the impact of gate leakage currents in the modeling of static characteristics of the device, and the effects of thermal annealing on such device non-idealities.

3.1 Introduction

Pentacene ($C_{22}H_{14}$) thin films for organic electronic applications have been widely exploited for research purposes, because of their good field-effect mobility enhanced by past advances in vacuum-based deposition techniques[1]. For these reasons such organic semiconductor is considered a benchmark material in OTFT studies and surface's optimization. Therefore, our analysis will take advantage of the literature knowledge about this material to investigate gate-dielectric static dissipations.

The gate leakage current is one of the most important non-idealities in field-effect transistors operation, in particular for applications in digital logic circuits and in pixel-drivers of active matrix organic displays backplanes. The presence of such leakage is evident in I_D/V_{DS} output characteristics, which fail zero-crossing at V_{DS} = 0 V in the linear region. Thus, the operation in this regime becomes difficult and performances decrease, also in terms of on-off currents ratio [3]. In some works, a thermal annealing has been proved

to reduce gate currents by de-doping the insulating films from undesired contaminants such as oxygen and moisture contents [3][5][6]. The aim of this study is to obtain an electrical model describing the effects of the analyzed non-idealities.

3.2 Samples preparation

For the gate contact, we have used commercial glass substrates coated with Indium Tin Oxide (ITO) film (thickness 130 nm) purchased from Delta Technologies, Ltd and processed after standard cleaning procedures. Three kinds of polymeric materials have been used to obtain the gate dielectric layers: Polyimide PI2556 from HD Microsystems (PI), Polystyrene (PS) Poly(1-phenylethane-1,2-diyl)) and AZ5214E photoresist (PR) from Clariant. Gate dielectrics were solution-processed by spin-coating technique, to obtain 1 µm-thick films for each material. PI was cured as specified by the Manufacturer [4] and PR was processed and hard-baked for 30' at 115°C without UV-light exposure to obtain a stable film. Pentacene was purchased by Sigma-Aldrich and processed under class-100 clean room environment and deposited without further purification.

Pentacene thermal evaporation was carried out at a base pressure of $2 \cdot 10^{-7}$ mbar from an alumina-coated crucible. Pentacene layers were deposited on the three samples in the same evaporation run, obtaining 65 nm-thick films at the average growth rate of 0.7 Å/s. The deposition process was performed at room temperature, to obtain polycrystalline thin film phase according to [9]. Source and drain gold contacts were deposited, after vacuum breaking, by thermal evaporation through a shadow mask, at a base pressure of 10^{-6} mbar. The 50 nm-thick electrodes, on the top of pentacene film, were deposited at the rate of 0.5 Å/s to fabricate a bottom-gate top-contacts OTFT structure (figure 1). Devices geometries were: channel length L = 500 µm, channel width W = 1200 µm, Drain (and Source) length $L_D = L_S = 1000$ µm.

The Pentacene films were characterized by means of UV-vis and near-infrared (NIR) optical absorbance, using films deposited on quartz with a Perkin-Elmer Lambda 900 spectro-photometer in the wavelength range of 200 ÷ 800 nm. The crystalline film structure was

determined by XRD measurements in Bragg-Brentano θ-2θ configuration with an MPD-XPERT (Philips) diffractometer, using a Cu Kα radiation source. Device's static electrical characterizations were performed by HP 4140B pA meter/DC source, in dark conditions at room temperature in ambient atmosphere.

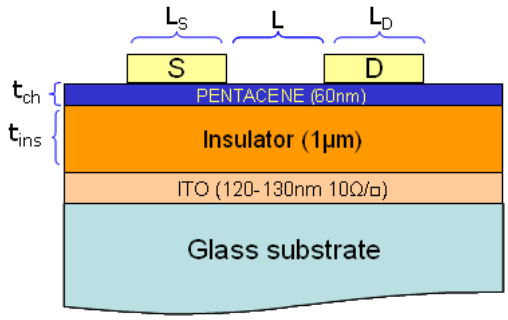

figure 1: analyzed OTFT structure.

Post-fabrication annealing was performed under clean room environment for 5' in oven at 115°C (for PI and PR samples) and at a lower temperature (90°C) for PS samples, to avoid polymers glass transition.

3.3 Results and discussion

3.3.1 UV-vis and XRD characterizations

The absorbance spectrum shown in figure 2 is in agreement with [6] for thermally-evaporated polycrystalline pentacene films. The peaks at 630 nm and 669 nm, due to Davydov-split, points out the presence of the high mobility phase [8][12]. XRD characterizations in Figure 3 show that the highly ordered single thin-film phase has been grown on each kind of insulator, as suggested by Dimitrakopoulos [9].

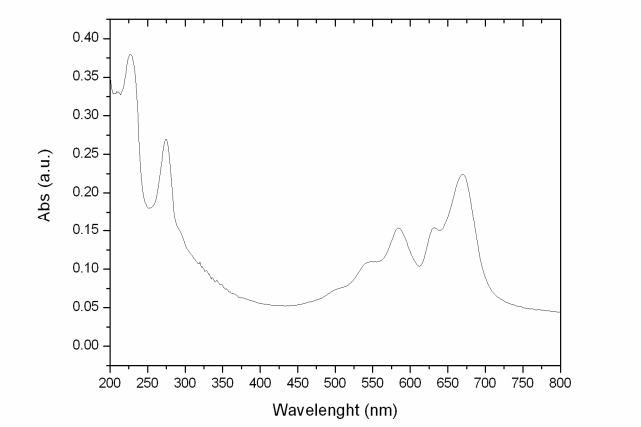

figure 2: Optical absorbance spectrum of a 65 nm thick pentacene film deposited on a quartz substrate.

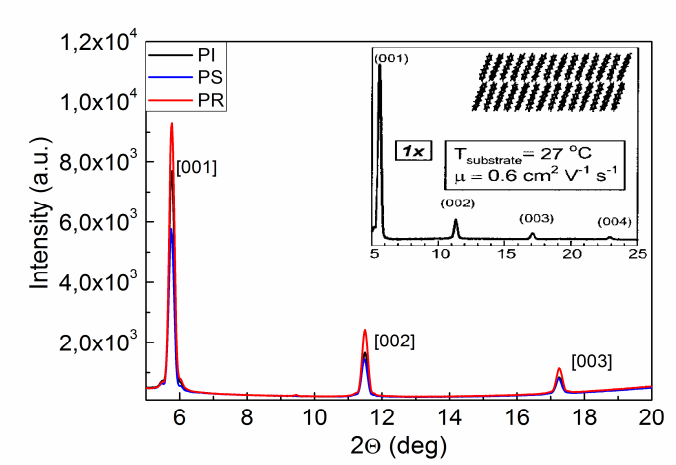

figure 3: XRD spectra of the pentacene film grown on the three insulators compared (inset) with [9].

An estimation of the average crystal domain of the three films was evaluated by applying the Scherrer formula:

$$\langle L \rangle = 0.9 \cdot \lambda / [\cos(\vartheta_0)\Delta(2\vartheta)]$$

to the (002) Bragg reflection of the films. In the formula, $\lambda = 1.54$ Å is the wavelength used for the measurements, ϑ_0 is the Bragg angle, and $\Delta(2\vartheta)$ is the FWHM.

The results are:

<L> = 35.4 nm	Polyimide
<L> = 35.1 nm	Polystyrene
<L> = 37.8 nm	Resist

These data do not show relevant differences in the films structure.

3.3.2 Electrical characterization and device modeling

figure 6 shows that the output characteristics for the PI sample, before the annealing process, fail zero-crossing at V_{DS} = 0 V. This effect can be attributed to a leaky gate insulator [10]. Moreover, since the sample revealed a symmetric Drain-Source behaviour, we can suppose the leakage current to be $I_S = I_D = I_G/2$ at V_{DS} = 0 V, as stated in [10].

Plotting $I_S(V_{DS} = 0\ V)$ vs. V_{GS} (see figure 4), a quadratic trend can be noticed. This result is common in many dielectric materials with trap-free Space-Charge Limited Current behaviour (SCLC). Thus the parasitic currents between the Drain contact and the Gate can be modeled by $I_G \sim V_{GD}^2$ obtaining:

eq. 1 $$I_S = -K\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^{\,2}\right] - \alpha V_{DG}^{\,2}$$

where α can be named *non-ideality factor*.

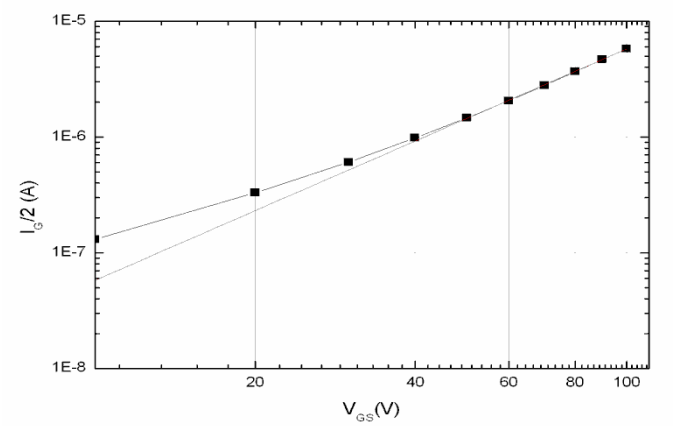

figure 4: Log-Log plot of Source current at VDS = 0 V for non annealed PI sample. Line slope=2.

If we look at figure 5, the elevated currents reported in figure 4 are not surprising. In fact the planar geometry of the device and the small thickness of films employed to obtain gate insulation, make the structure in figure 1 a topology which it can be easily argued to be affected from such leakages. In our approach, the character of gate current can be extracted from usual output and trans-characteristics by considering the zero-polarization plot of I_S (see a schematization of the leakage paths in figure 5).

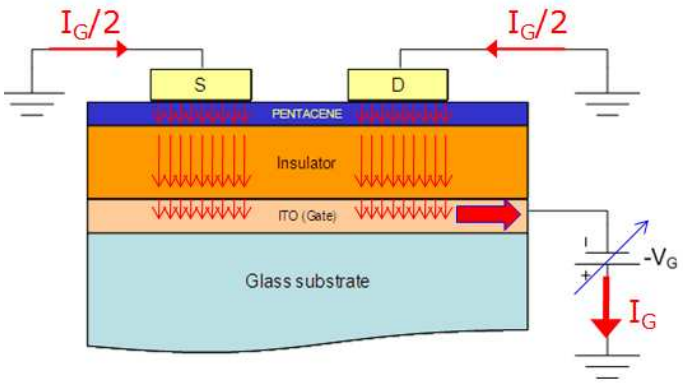

figure 5: Investigating gate leakages in manufactured devices

It has to be considered that the increase of gate current is provoked by a complete overlap between contacts and gate and a relatively small gate-source and gate-drain separation (in the figure 5 it has to be 1.000µm (insulator) + 65nm (pentacene) = 1.065 µm)

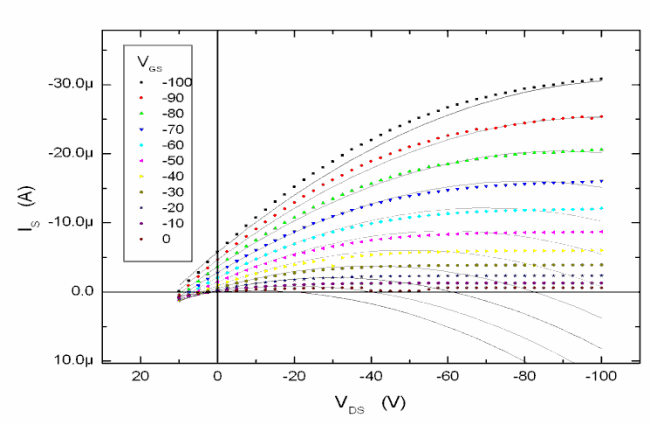

figure 6: Output characteristics of PI device before annealing (dotted: experimental; line: model fitting simulations of eq. 1).

The fitting results (figure 6 and eq. 1 with the common meaning of symbols) reveal that the gate leakage current is related to the gate-drain voltage, if drain was biased ($V_{DS} \neq 0$). After the annealing process, the output characteristics change (see figure 7), restoring the zero-crossing at $V_{DS} = 0$ V. Consequently, we can state that gate leakage-current reduces and the device approaches a quasi-ideal FET operation (i.e.: $\alpha = 0$).

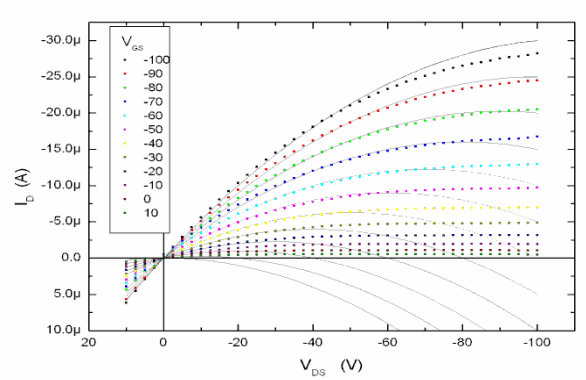

figure 7: Output characteristics of PI device after thermal annealing (dotted: experimental; line: model fitting simulations with MOS ideal model).

For PS and PR samples, the same characterization steps before and after annealing have been carried-out. For PS, the fitting results have shown in both conditions (see figure 8 and figure 9) the presence of a contact barrier voltage (V_C), as also reported in [11]. In this case, the undesired current affects the characteristics at low V_{DS} and the fittings show a dependence from the only V_{GS} bias, which can be modeled by $I_G \sim V_{GS}^4$ (as in eq. 2) due to Trap-Charge-Limited Space-Charge-Limited-Current (TCL SCLC). In this case, we detected the presence of a Source-Drain contact barrier, modeled in eq. 2 through the V_C voltage shift of the V_{DS} as suggested by Horowitz [11].

eq. 2 $$I_S = -K\left[2(V_{GS} - V_T)(V_{DS} - V_C) - (V_{DS} - V_C)^2\right] - \alpha V_{SG}^4$$

Here, the baking treatment decreases the *non-ideality factor* α but keeps the same power law exponent, as appears from fittings shown in figure 9 with the eq. 2 model.

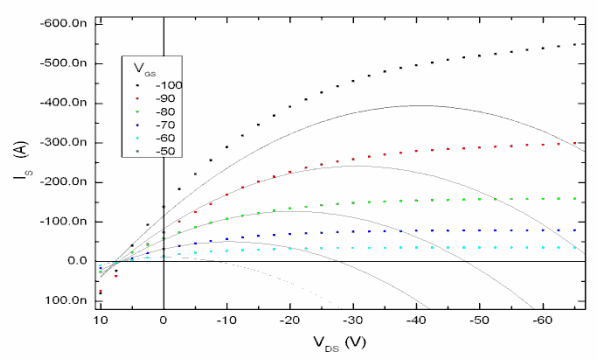

figure 8: Output characteristics of PS device before thermal annealing (dotted: experimental; line: fitting simulations of Eq. 2).

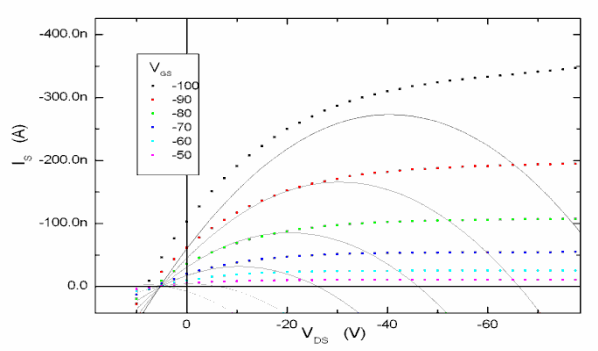

figure 9: Output characteristics of PS device after thermal annealing (dotted: experimental; line: model fitting simulations of Eq.2).

The sample fabricated with PR, before annealing, also has shown a gate leakage current (see output characteristics in figure 10), modeled by a quadratic SCLC transport, as in eq. 3

eq. 3 $$I_S = -K\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^{\,2}\right] - \alpha V_{SG}^{\,2}$$

but, differently from the not-annealed PI sample, the leakage current is related to the Source-Gate voltage.

After the annealing (figure 11), the output characteristics are null at V_{DS} = 0 V and the device fits an ideal FET model (i.e.: α = 0). The threshold voltage V_T becomes more positive, enhancing the depletion-FET behaviour.

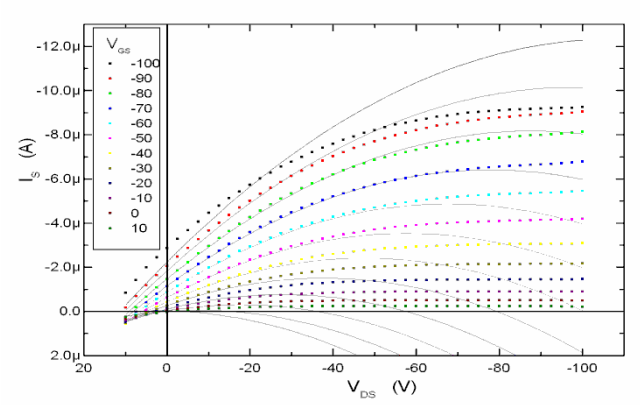

figure 10: Output characteristics of OTFT with Photoresist gate dielectric (dotted: experimental; line: model fitting simulations of eq. 3).

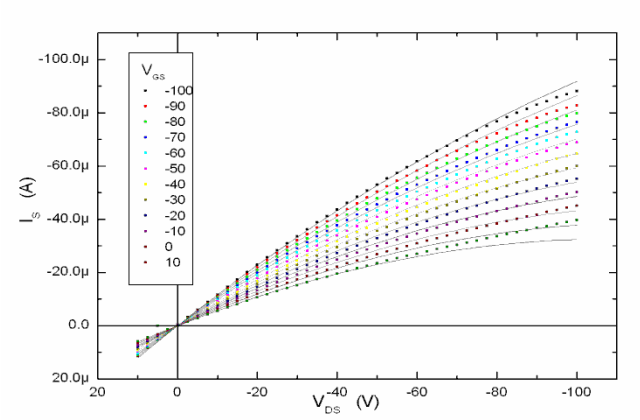

figure 11: Output characteristics of PR device after thermal annealing (dotted: experimental; line: model fitting simulations with MOS ideal model

To summarize our experimental results, we propose a generic electrical model for the OTFTs, shown in figure 12: electric model of fabricated devices. In this figure the effects of all the non-idealities that have been found, and also known results 105[11][12], are taken into account.

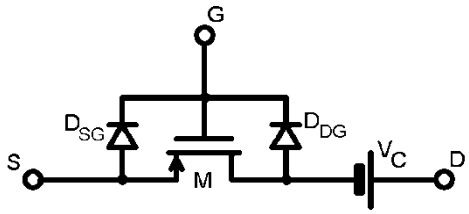

figure 12: electric model of fabricated devices.

The diodes D_{SG} and D_{DG} model the dependence of the gate leakage current components from V_{SG} and V_{DG} respectively, while the V_C voltage shift, due to the contact barrier, is described through a series voltage source.
Then, the generic electrical model can be written as:

eq. 4 $$I_S = -K\left[2(V_{GS}-V_T)(V_{DS}-V_C)-(V_{DS}-V_C)^2\right]-\alpha_S V_{SG}{}^m-\alpha_D(V_{DG}-V_C)^m$$

As explained above, the empirical coefficient *m* is related to the kind of SCLC transport in the gate insulator.

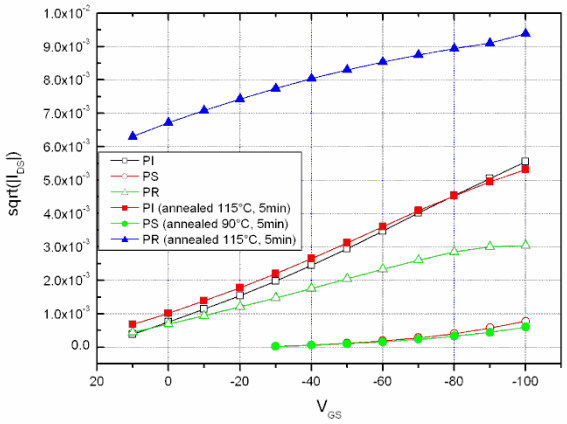

figure 13: Mobility evaluation in saturation regime by plots of sqrt(I_S)/V_{GS} without taking into account non-idealities.

Using the ideal FET model in the saturation operation (eq. 5)

eq. 5 $$\mu_{SAT} = \frac{2L}{WC_{ins}}\left(\left.\frac{\partial\sqrt{I_{Dsat}}}{\partial V_{GS}}\right|_{V_{DS}\le V_{GS}-V_T}\right)^2$$

The evaluated mobility values extracted from $\sqrt{(-I_S)}/V_{SG}$ plots (see figure 13) are smaller than the estimated ones in triode operation fitted with the unified model (eq. 4 and figure 12).

Fit parameters shown in table 1 (related to the triode operation) suggest that for the PI sample the device benefits of a better gate insulation if annealed. Furthermore, we observed in each case a slight decrease of mobility and K and a small V_T increase. About the PS sample, the same trends for μ_{TRI}, μ_{SAT} and K are confirmed, while the threshold voltage (V_T) and the contact barrier V_C seem not affected by the thermal process. For PR sample, it can be observed a huge increase in threshold voltage (positive values) approaching a deep-depletion-like operation for the OFET. Mobility and K also increase their values. From extracted mobility values, it does not appear a direct relationship between the average crystallite size <L> and OTFT performances, in according to results reported in [15].

If we suppose for the not-annealed PI and PR samples the SCLC transport in gate leakage current, according to [14], we can estimate the insulator mobility from the *non-ideality factor* α

eq. 6 $$\mu_{ins} = \frac{8}{9}\frac{\alpha \cdot t_{ins}^3}{WL_S \varepsilon_r^{ins} \varepsilon_o}$$

giving $\mu_{ins}(PI) = 1.4 \cdot 10^{-7}$ cm^2/(Vs) and $\mu_{ins}(PR) = 4.1 \cdot 10^{-8}$ cm^2/(Vs).

	ε_r (adim.)	K (A/V^2)	μ_{TRI} (cm^2/Vs)	μ_{SAT} (cm^2/Vs)	V_T (V)	V_C (V)	α_S (A/V^m)	α_D (A/V^m)	m (adim.)
PI	3.4 [15]	2.6E-9	0.73	0.71	7.6	0	0	5.7E-10	2
PI annealed		2.5E-9	0.69	0.57	10	0	0	0	n.a.
PS	2.5 [16]	1.7E-10	0.06	0.064	-55	4.5	5E-16	0	4
PS annealed		1.3E-10	0.049	0.007	-55	4.5	1E-16	0	4
PR	4.9 [17]	8.7E-10	0.167	0.144	7.7	0	2.4E-10	0	2
PR annealed		2.7E-9	0.519	n.a.	120	0	0	0	n.a

table 1: OTFT model parameters synthesis

3.4 Advanced circuital gate leakage models application in performance analysis of OTFTs

By advancing the analysis of circuital equivalent model seen in previous chapters, taking into account that contact potential V_C should not appear at the device's terminals, in further works [19], we added an ideal diode on drain electrode to prevent this (see figure 14).

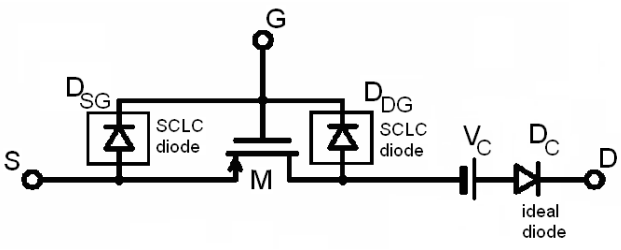

figure 14: OTFT electrical model complete of gate leakage and source/drain contact barriers non-idealities.

In other words, the total effect of the source and drain contact barriers is described from the V_C source voltage, the diode D_C underlines the asymmetrical behavior of the characteristics while the gate leakage current is related to the D_{SG} and D_{DG} diodes.

Adopting this circuital model, source current equations can be rewritten in terms of external applied voltages (eq. 7, eq. 8 and eq. 9).

For Polyimide OTFT:

eq. 7 $$I_S = -K\left(2(V_{GS} - V_T)V_{DS} - {V_{DS}}^2\right) - \alpha(V_{DS} - V_{GS})^2$$

For Polystyrene OTFT:

eq. 8 $$I_S = -K\left(2(V_{GS} - V_T)(V_{DS} - V_C) - (V_{DS} + V_C)^2\right) - \alpha {V_{GS}}^4$$

For AZ5214E OTFT:

eq. 9 $$I_S = -K\left(2(V_{GS} - V_T)V_{DS} - {V_{DS}}^2\right) - \alpha {V_{GS}}^2$$

Then, the general electrical model can be more properly expressed as follows:

eq. 10
$$I_S = -K\left(2(V_{GS} - V_T)(V_{DS} - V_C) - (V_{DS} - V_C)^2\right) - \alpha_S {V_{GS}}^m - \alpha_D (V_{DS} - V_{GS} - V_C)^m$$

3.5 Gate-leakage models in the evaluation of morphology-performance relationship

As it will be better explained in chapter 3, a correct estimation of channel current, which is different from drain or source current because of gate-leakages, can help from misleading interpretations of mobility, threshold voltages and more in general of OTFTs performances.

On the basis of SEM (Scanning Electron Microscope) imaging performed on the three (PS, PI, PR) samples, it has been possible to estimate pentacene grain dimensions and relate it to hole mobility in the channel (see figure 15, figure 16, figure 17).

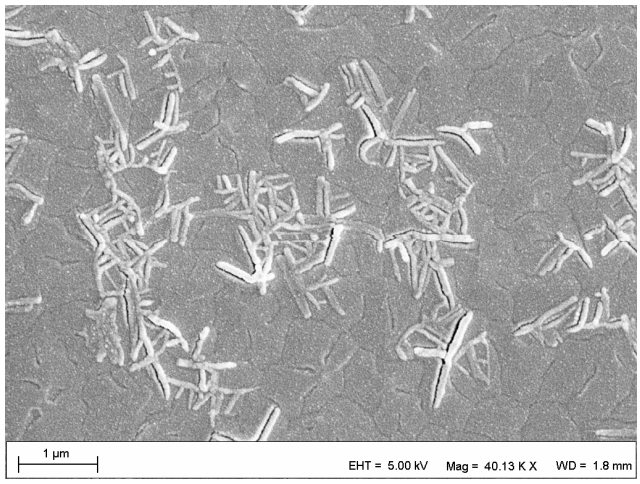

figure 15: SEM image relative to the PI sample.

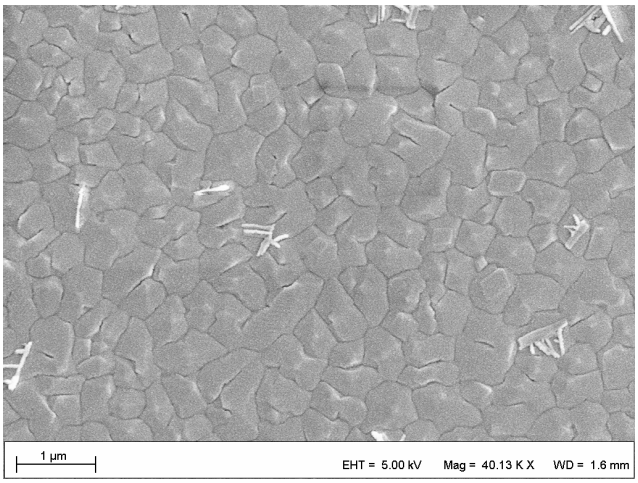

figure 16: SEM image relative to the PR sample. Grain shapes and grain boundaries are evident.

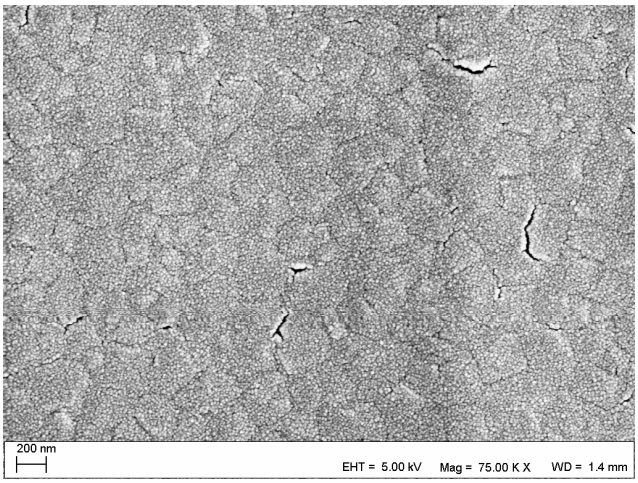

figure 17: image relative to the PS sample.

Such extracted dependence can be summarized as in figure 18 obeying the dependence noticed from Horowitz on a different class of OTFTs[20].

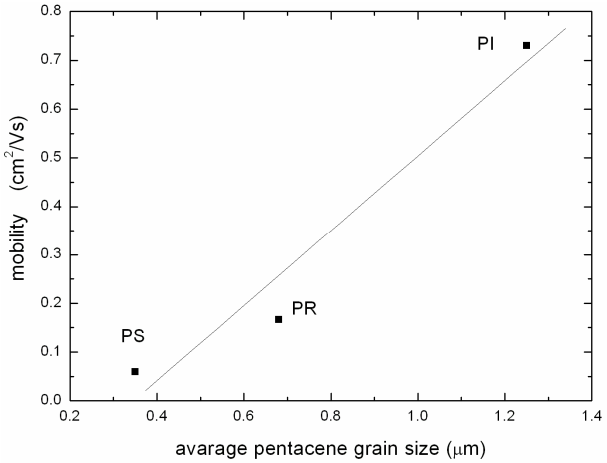

figure 18: Experimental dependence of the channel mobility from the pentacene average grain size. The line is only a guide for eyes.

3.6 Conclusions

In this chapter, we have analyzed non-idealities of pentacene OTFTs. In our samples, we studied the effect of gate leakages and contact barriers; therefore we have proposed a unified electrical model to describe these parasitic effects.

Furthermore, the origin of the gate current leakages can be attributed to the simple topology of fabricated OFETs, having unpatterned gates and channels. The model describes dielectric leakages by means of two Source-Gate and Drain-Gate SCLC-diodes.

A voltage source in series with the Drain terminal of the ideal FET describes the contact barrier.

The proposed model well fits the different behaviours of transistors fabricated with three different polymeric gate insulators and the effects of simple thermal annealing process. After this, we have observed a clear reduction of the gate-leakage current and estimated a slight mobility decrease. All the devices have shown gate leakage currents. This effect has been electrically modeled with two SCLC diodes and in Polystyrene sample the V_{DS} shift has been

modeled with a constant voltage source. The proposed model has allowed to estimate the channel mobility and the voltage threshold.

The mobility values of the devices estimated with the model agrees with the SEM analysis. Further investigations will show (chapter 3) that in the case of different topologies and dielectrics, the variation of charge mobility with gate field will make sometimes not-consistent the fits made with a model having a power-law dependence of current from voltages as in the examined case.

3.7 Layout design impact of the gate-leakage analysis

Gate leakages are often a *hidden problem* in many literature reports. They become relevant when working on very thin insulating films or leaky dielectrics like polymers or solution-processed materials and are responsible of static dissipation in OFET-based circuitry.

From observations of this chapter's data analysis we can state that the PI offers the best performances once annealed: in terms of mobility: 0.72 $cm^2V^{-1}s^{-1}$ with a negligible gate leakage I_G
The drawback of Polyimide utilization are the high operating voltages (0,-100V), the it should be necessary to fabricate thinner dielectrics to increase the insulator's capacity C_{ins}.

Unfortunately, we were not able to process PI layers under the 1µm thickness without obtaining gate short-circuits. But a way to reduce active area under contacts had to be found to optimize devices not only in terms of mobility but thresholds, gate leakages, operating voltages and so on.

Being the overlap between S/D contacts in large part responsible of such non-ideality effects, to improve performances we had to move to a process/layout with patterned gates/islands. In this line of work we can take into account three chances:

- **OSC subtraction**.

  This is usual in inorganic devices where organics are used just to make patterning and removed with solvents. Thus, inorganic technology is for its nature orthogonal to patterning technology. This method is not actable without any precaution

to organic materials which are unstable if in contact with solvents and water.

- **OSC passivation** in unused zones.

  If such passivation (mobility/conductance reduction in specific areas) could be obtained selectively by optical, hopefully lithographic, methods, it would be good to obtain the precise geometries required from performing OFETs operation. From this point of view, is known that UV irradiation can be active on organic materials provoking molecule's oxidation/degradation[21].

  We have followed this path to clarify if by using common photolithography equipment we could obtain pentacene passivation outside the channel region by irradiating a PI OTFT with the UV light coming from a Suss MA6 mask aligner equipped with quartz masks (see figure 19).

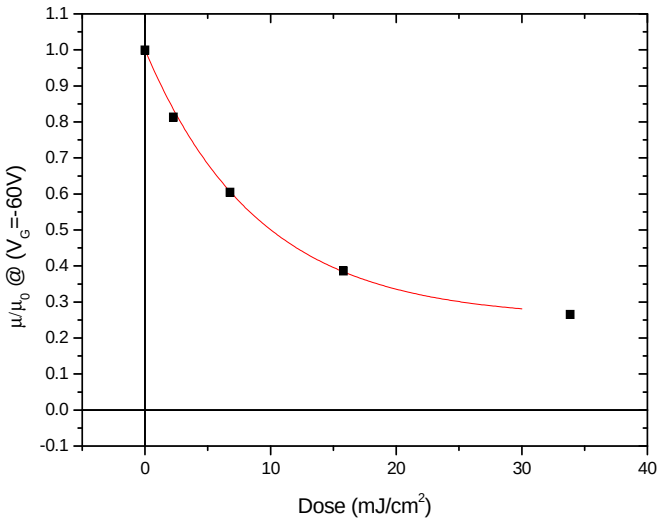

figure 19: the pentacene mobility changes of one order of magnitude by increasing the UV dose over 25/30 mJ/cm^2

As it can be seen in figure 19 and by model in , just one order of magnitude of response reduction can be obtained by i-line g-line UV optical patterning.

eq. 11 $$\mu(D) = \mu_{\infty} + Ae^{-\frac{D\,[mJ\ /\ cm^{2}]}{D^{*}}}$$

- Shadow-masks are the only way to realize easily layer's patterning for evaporated materials, thus an appropriate set of masks has been designed, realized and adopted to accomplish to this (the change in topology is summarized in figure 20).

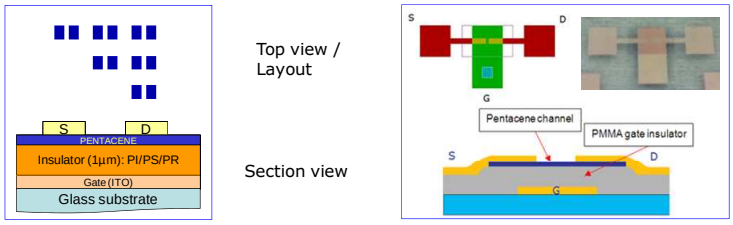

figure 20: left: unpatterned topology, right layout based on stencils

The adoption of PMMA (Poly(methyl methacrylate)) has been done to scale the insulator's thickness. In further analyses the new topology will be adopted for fabricated OTFTs.

A brief summary of performances obtained is reported in table 2.

	Old layout and PI	New layout and PMMA (115nm)	Effect
t_{ins}(µm)	1	0.115	
ε_r	3.4	3.66	
C_{ins}(F/cm²)	0.301	2.843	Operating voltage reduction
W/L	1200/500=2.4	350/70=5	I_D increase
G/S Overlap Surface (µm²)	600k	511k	reduction of I_G
V_T(V)	+10	-7.1	accumulation operation and operating voltage reduction
µ(cm²V⁻¹s⁻¹)	0.69	0.09	I_D decrease

table 2: PI and PMMA OTFT performances compared

In this reference case, by reducing the insulator thickness by factor 10, we have been able to decrease operating voltages from -100V to about -16V but surface properties of PMMA are not optimized for pentacene growth then we have to work on dielectric modification to

enhance mobility again. Furthermore, some effort will be done in reducing threshold voltages. Please see chapter 4.

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Chapter 4

Morphology-mobility relationship in dielectrics with optimized surface-energy and its exceptions studied by means of density of states

Gate-dielectric properties and dielectric-semiconductor interface physics are known to govern growth of pentacene channel films with a tremendous impact on the morphology of their polycrystalline phase [1][2][3][9]; in this context, surface wettability can be considered as a measure of interface energy properties reflecting on the growth of the first molecular layers of channel semiconductor on the top of the gate dielectric layer.

In the scope of the present work there's the development and optimization of gate-dielectrics to enhance channel properties and then device performances.

As a result of the research work, it has been developed a device based on an organic-inorganic hybrid insulator deposited from solution phase by sol-gel processing. It has been studied by using an OTFT as a characterization experiment in comparison with known results. We found such dielectric layer (named after its acronym PFTEOS:TEOS) exhibiting anomalous trends in a well-assessed morphology-mobility relationship.

The nature of this class of OTFTs has been studied by thermal activation of charge mobility characterizations which showed the innovative dielectric having a behavior in contrast with common polymeric gate insulator-based transistors. Such singularity has been related to density of states in the valence band and to microscopic disorder which cannot be evaluated by common morphological characterizations (Scanning Electron Microscope etc.).

3.1 Introduction

It's known that morphology and charge transport in polycrystalline pentacene is strongly related to gate-dielectric properties and, more in detail, to dielectric-semiconductor interface nature [1]. Thus, in OTFT's performance optimization, it's fundamental to qualify and quantify the OSC/insulator interface features and control them in device's processing phase.

Literature studies report that in a pentacene medium the charge mobility is limited by grain-boundaries (see [3][4][5] and their references) as in models derived from amorphous and polycrystalline silicon. There are, indeed, Research Teams which have obtained high performance pentacene-based OTFTs having very small grains (<<1μm) by surface treatment of a SiO_2 gate dielectric by octadecyltrichlorosilane (OTS) SAM deposition. Thus the effect of semiconductor grains dimension on OTFT mobility is still controversial and not fully understood but some well-defined trends have been identified. The correlation between processing parameters and device's performances has been proven showing that hydrophobic dielectric surfaces have the ability to enhance device's saturation current and field-effect mobility (μ_{FE}) [8] by acting on the molecular order in the growth of first layers of semiconductor.

In a fundamental reference work [9] surface energy-controllable dielectrics have been obtained and studied proving that low-wettability interfaces can induce a "Stransky-Krastanov growth" of pentacene films with grains of great dimension (>1μm) and evident dendritic off-film formations.

In the referred work and also in further papers [10], a low surface energy has been suggested to be the most favorable condition to promote high charge transfer rates between adjacent zones by increasing the degree of interconnection and avoiding the formation of incomplete molecular layers. For these reasons, in the present work it have been prepared novel hydrophobic dielectric layers for OTFTs and interfaces to increase the quality of morphology of pentacene channels and enhance charge transport in such devices.

Keeping in mind these considerations, after taking into account standard gate dielectrics, we acted on the nature and interface of

insulators to increase the hydrophobicity level and obtain a large-grain growth of pentacene.

Known techniques to account this are the utilization of highly hydrophobic compounds in gate dielectric layer fabrication, the surface treatment of usual insulating materials by chemical [14][15] and/or physical [16] processing or by the deposition of buffer layers [11][12][13], self-assembled monolayers (SAM)[17] or self-assembled multilayers (SAMT)[18].

In the preparation of the new dielectric materials, we introduced an organic-inorganic hybrid material based on a *Tetraethyl Orthosilicate / 1H,1H,2H,2H-Perfluorodecyl triethoxysilane* commonly named "PFTEOS:TEOS" solution. The abovementioned layer is characterized by perfluoroalkyl units which are responsible of the desired hydrophobic properties. It has been deposited by a spin-coating-based sol-gel technique on the metallic gate layer.

From the point of view of the physical treatments we studied the effect of CF_4 plasma treatments on common PMMA gate dielectrics as it has been already done on PVP/CeO_2 combined dielectrics [16].

Furthermore, by following the same optimization path, a thin film (<10nm) of Poly(methyl methacrylate), PMMA, has been employed to bufferize the PFTEOS:TEOS surface similarly to the treatment which has been already demonstrated to be effective on SiO_2 interfaces [11] with OSC in top contacts OTFTs [12][13] by Mariucci et Al.

The relationship between maximum field-effect mobility and average pentacene grain dimension in the channel[3] has been extracted and analyzed for fabricated OTFTs demonstrating that PFTEOS:TEOS samples have a behavior which does not obey the general trend for performances which we also have found for a wide class of polymeric insulators.

In contrast to single crystal semiconductors, in our devices, channels are disordered or partially ordered systems then the charge transport is dominated by localized states which result in temperature and gate voltage dependencies of μ_{FE}.

It has also been reported [19] that for the referred kind of disordered systems there's a dependence of the activation energy of mobility from the gate voltage bias, a thermal activation analysis has been performed showing in Arrhenius plots of μ_{FE} extracted from static characteristics the existence of a compensation rule which we modeled according to Meyer-Neldel[20] relationship (MNR).

Then, we utilized the model parameters extracted from DC characteristics to investigate the singularities correlated to PFTEOS:TEOS samples and founding the Meyer-Neldel Energy (MNE) to be one of the key factors which can explain mobility trend differences in terms of in-band DOS and microscopic disorder.

3.2 General device structure and processing

OTFTs analyzed in this chapter share the same bottom-gate/top-contact topology. They have been processed under a class-100 clean room environment on boron-silicate glass. Contact structures and semiconducting islands have been defined by means of shadow-masks utilized during evaporated films deposition process. Different kinds of insulators have been all solution process-deposited utilizing a spin-coater. For the sake of simplicity we report a cross-section and a top view schematics layout of a device (see figure 1).

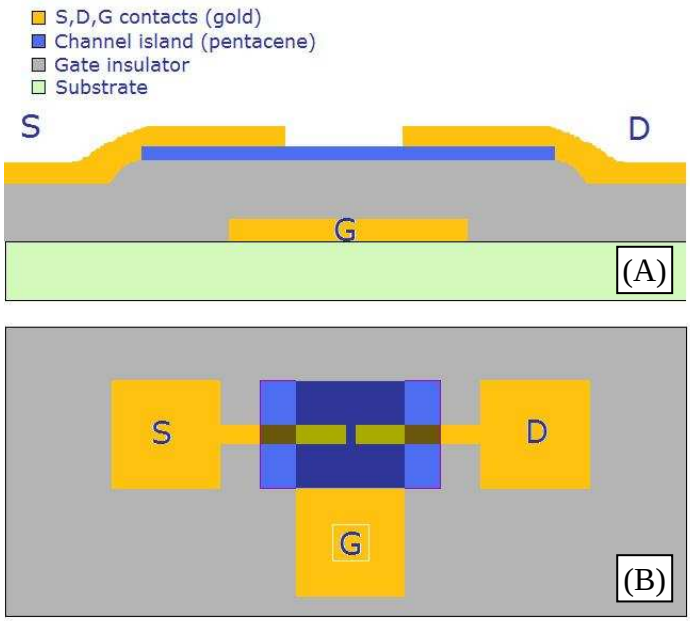


figure 1: cross-section (A) and top-view (B) schematics of an analyzed OTFT device (image B reflects real layout)

In the aim to investigate the behaviour of mobility and overall performances in the semiconductor when the gate dielectric is varied, materials and processes employed to process the substrates, contacts the organic semiconductor channel and their thicknesses have been kept unvaried. The only variations introduced in the fabrication

process are exclusively due to the nature, the thickness and the interface of the gate dielectric. Thus, being the insulator features the controlled variable; we decided to briefly identify samples by means of an acronym which reminds to the particular dielectric involved in the fabrication.

In figure 1, we report materials, thicknesses and identifying acronyms of OTFT varieties in order to make more immediate the measurement interpretation.

More in detail, three thicknesses of PMMA dielectric have been deposited by spinning to make explicit the dependence of mobility from gate electric field and the relationship between insulator thicknesses and pentacene morphology.

Structure / Role	**Material**	**Thickness**	**Sample id.**
Substrate	Boron-silicate glass	1mm	
Gate adhesion layer	Chromium	10nm	
Gate electrode	Gold	50nm	
Gate insulator	PMMA	114nm, 225nm, 420nm	PMMA114 PMMA225 PMMA420
	CF_4-treated PMMA	225nm	PMMA/CF_4
	PFTEOS:TEOS	270nm	PFTEOS:TEOS
	PFTEOS:TEOS having a 10nm-thick PMMA layer	273nm	PFTEOS:TEOS/PMMA
Channel semiconductor	Pentacene ($C_{22}H_{14}$)	65nm (avg. thickness)	
S/D electrodes	Gold	50nm	

table 1: Fabricated samples materials, thicknesses and acronym ids.

Gate contacts have been deposited in standard conditions with fixed planetary substrate holder in an evaporation chamber at the base pressure of $2 \cdot 10^{-7}$mbar from 99.99% purity metals by means of thermal evaporation. Chromium has been evaporated with 0.1Å/s rate and gold with an average rate of 0.5 Å/s.

Pentacene islands are formed by vacuum evaporation of $C_{22}H_{14}$ from a Kurt J. Lesker Al_2O_3 source provided with an additional hot-lip at the base pressure of $1.2 \cdot 10^{-7}$mbar with an average rate of 0.6Å/s.

The pentacene material employed as evaporation source has been purchased from Sigma Aldrich and processed without any other purification. Gate masks, island masks and S/D contact masks are changed by breaking the vacuum and opening the evaporator chamber.

3.2.1 PMMA gate-insulators processing

PMMA is spin-coated from 4% and 8% (in weight) solutions in toluene solvent. Thus, three different thicknesses of polymeric dielectric have been obtained by varying the spin coating recipe and polymer concentration as reported in table 2.

Sample id.	PMMA thickness	PMMA concentration (w/w)	speed (rpm)	Time (s)	Acceleration (rpsqm)	Ra (nm)	Rq (nm)
PMMA115	114nm	4%	3500	40	1500	1.2	1.9
PMMA225	225nm	4%	1500	40	1000	1.3	1.6
PMMA420	420nm	8%	3000	40	1500	1.2	1.4

table 2: PMMA thickness recipe to obtain three different film thicknesses.

Soon after deposition, toluene is drift off the film by thermal annealing on an hot-plate at 100°C for 2hr.

3.2.2 PFTEOS:TEOS gate-insulators processing

The materials used to prepare hydrophobic dielectric films are here below enumerated:

- Aqueous solution (0.24M) of hydrochloric (HCl) acid
- Poly-(methylmethacrylate) (PMMA) (M_w = 120,000Da) purchased from Sigma-Aldrich
- Tetraethyl Orthosilicate (TEOS), purchased from Sigma-Aldrich Mw = 208.33Da

- 1H,1H,2H,2H-Perfluorodecyl triethoxysilane (PFTEOS) (Mw = 610.38Da), purchased from Sigma-Aldrich
- Ethanol
- Toluene
- Fluoro-propanol

In table 3 is shown the molecular formulas of PMMA materials, TEOS and PFTEOS.

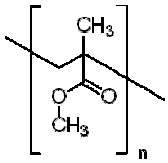
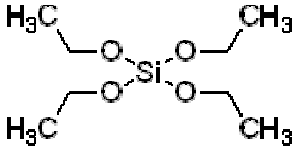
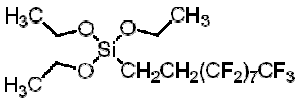
Material	Molecular formula
Poly-(methylmethacrylate) (PMMA)	
Tetraethyl Orthosilicate (TEOS)	
1H,1H,2H,2H-Perfluorodecyl triethoxysilane (PFTEOS)	

table 3: Molecular formulas of compounds utilized as gate dielectrics

Before spin-coating deposition of dielectric films on TFT devices with the structure shown in figure 1, the same films were prepared on glass substrates to be characterized by means of measures of roughness, contact angle measurements and SEM imaging of morphology.

For the preparation of PFTEOS:TEOS, 1.333g of TEOS and 0.073g of PFTEOS were diluted in 5ml of ethanol by stirring on hot-plate for 5 minutes.

A 0.25 ml HCl (0.24M) aqueous solution is diluted in 5 ml of ethanol and added drop-by-drop to the PFTEOS:TEOS solution. After the preparation, the solution is stirred for 16hr to prevent the formation of clusters. Before spin-coating, the solution is diluted with an equal volume of 3-fluoropropanol to enhance the adhesion of the solution on glass. After this preparation phase, the solution is filtered and deposited by spinning on the substrates at 1000rpm for 30s with an acceleration of 800 rpsqm. Soon after spinning, the film has been cured on an hot plate under laminar flow in a class-100 environment for 30 minutes to evaporate the solvent and then gradually heated in an oven from 110°C to 150°C and kept at 150°C for 16hr before pentacene deposition. For the preparation of the PMMA films on PFTEOS:TEOS, a 4% solution of PMMA in toluene has been prepared. A 10nm-thick layer of PMMA has been deposited by spin-coating of that solution at 6000rpm for 1 min with an acceleration of 5000rpsqm on the top of the PFTEOS:TEOS cured film. Toluene is removed by keeping the sample on an hot plate at 100°C for 2 hr to promote solvent evaporation.

In table 4, films thicknesses and obtained roughness are reported.

Film	Thickness (nm)	Roughness (nm)
Glass substrate		Ra=2.1
		Rq=2.8
PFTEOS/TEOS	273	Ra=2.7
		Rq=3.4
(PFTEOS/TEOS)/PMMA	273/10	Ra=2.9
		Rq=3.8

table 4: morphological characterization of PFTEOS:TEOS films.

Surface roughness is a key factor in OTFT performances. A rough dielectric-to-channel interface causes charge trapping and scattering because of interface traps thus a higher gate voltage is

necessary to modulate the channel current[21]. As we can state by observing table 4, film roughness increases of few Angstroms when film is deposited on the glass substrate. For the sake of our investigation similar values of mean roughness have been obtained, therefore a comparison can be considered consistent from this point of view.

3.2.3 Sol-gel PFTEOS:TEOS processing

When PFTEOS and TEOS are put in solution, the silicic derivatives hydrolyze giving Si-OH groups which are able to undergo to condensation. Such condensation process happens when the material is in its thin-film phase (after spin-coating) by means of thermal curing at 150°C. During this process the material forms networks of chemical bindings between functionalized Si-O-Si and perfluoroalkyl groups which tend to migrate to the film surface giving rise to enhanced hydrophobic interface properties[22] (see figure 2).

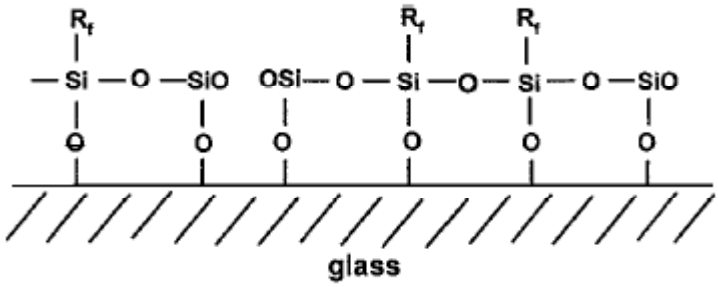


figure 2: schematization of perfluoroalkyl groups localization on PFTEOS:TEOS film surface

The described sol-gel process is summarized in figure 3

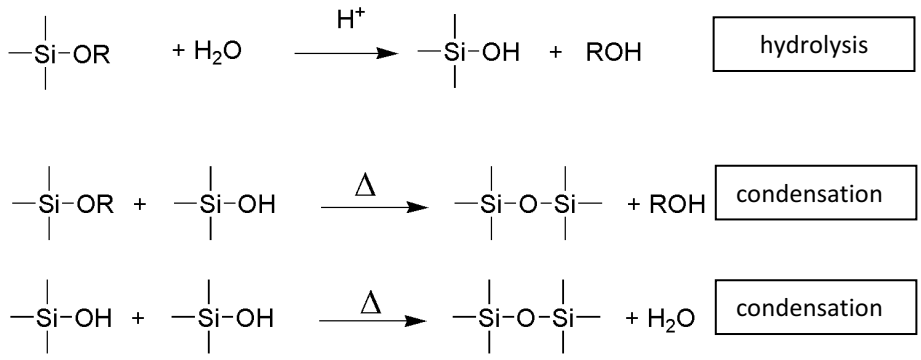
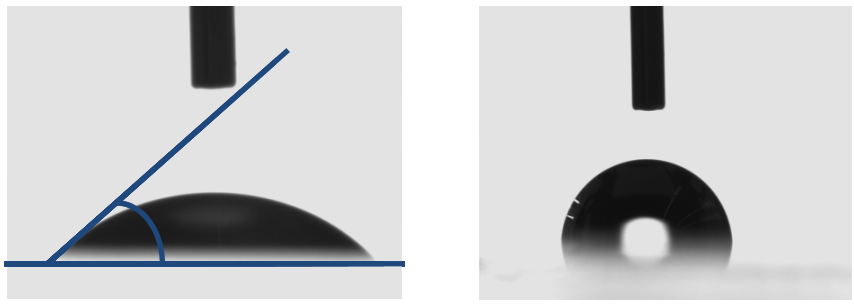


figure 3: PFTEOS:TEOS sol-gel process schematization

3.3 Materials and interface characterization

3.3.1 Contact angle measurements on PFTEOS:TEOS-based thin films

To measure surface wettability of prepared films contact angle measurements have been performed by dispensing deionized (DI) water on deposited test substrates either on glass surfaces than Cr/Au gate structures to establish the effect of the thin film processing on each portion of the gate-level substrate.



(a): α(Glass) = 48° (b): α(Cr/Au) = 87.2°

figure 4: Initial condition: contact angle measurement process of DI water on (a): glass substrate, (b): Cr/Au gate

After PFTEOS:TEOS deposition and curing, contact angle is verified repeating measurements that show differences between films coated on the glass portion of the substrate surface and the metallic area (see figure 5).

(a): α(PFTEOS:TEOS on Glass) = 111.5°

(b): α(PFTEOS:TEOS on Glass) = 111.5°

figure 5: contact angle measurements on PFTEOS:TEOS deposited (a): on Glass, (b): on Cr/Au surface

As a reference, the contact angle of DI water on a simple PMMA (thickness 200nm) surface deposited on glass is reported to validate the 10nm buffer layer processing (see figure 6). Taking into account this information about a plain PMMA surface, we measured wettability on PMMA buffer layers (10nm) on PFTEOS:TEOS showing a contact angle of 70° which is really near the one we obtained for the initial case of PMMA (figure 6) proving the effectiveness of the buffer layer deposition.

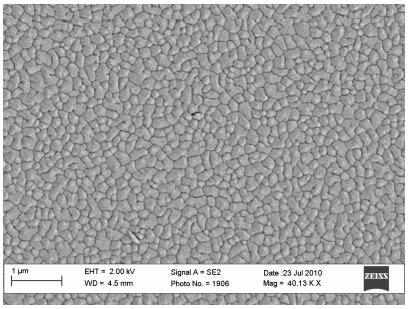
figure 6: Contact angle on a 200nm-thick cured film surface of PMMA (67.2°).

3.3.2 Scanning Electron Microscopy (SEM) imaging of channel morphology

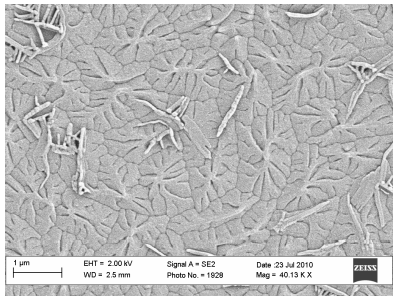
The knowledge of surface morphology of the charge transport medium is fundamental because it is one of the ways to predict device's performances without making a complete device. The use of

a scanning electron microscope (SEM) allows for rapid surveying of in-plane geometric features of grown semiconductor films on different dielectrics once the sample is conveniently prepared.

To make imaging possible, a 10nm-thick gold layer has been sputtered on the top of pentacene films. Imaging has been performed by using a Leo 1530 Scanning electron microscope revealing fundamental difference between PFTEOS:TEOS and PFTEOS:TEOS/PMMA samples (see figure 7).



(a): pentacene grown on PFTEOS:TEOS surface



(b): pentacene grown on PFTEOS:TEOS/PMMA surface

figure 7: SEM imaging of pentacene channels grown on top of (a): PFTEOS:TEOS surface, (b): PFTEOS:TEOS/PMMA surface. Images are taken at the same 40.13X magnification

Surprisingly, differently from we expected for polymeric dielectrics, an higher contact angle does not result in a greater pentacene average grain size. The explanation of this effect is still unclear and in contrast with other literature results. In table 5 a summary of grain dimensions we found for different OTFT insulator surfaces has been reported.

Sample	Grain width (µm)	Std. Deviation (µm)
PMMA115	0.346	0.087
PMMA225	0.344	0.094
PMMA420	0.258	0.072
PFTEOS:TEOS	0.191	0.048
PFTEOS:TEOS/PMMA	1.26	0.478

table 5: statistics on pentacene grain dimensions evacuate by SEM surface imaging.

3.4 Device's characterization

3.4.1 Experimental

Electrical characterizations and have been performed by means of a Cascade SUMMIT 11000M probe station equipped with a N_2 atmosphere chamber (micro-chamber) and a thermal chuck connected to an ESPEC ETC 200L EMO thermo-chuck controller. The probe station is set-up with three DC probes kept in nitrogen flow.

To measure static output and trans-characteristics we adopted a Keithley SCS4200 semiconductor parameter analyzer having two pre-amplified SMU and one ground unit. The apparatus is able to measure simultaneously the drain current and the gate leakage making possible to evaluate static dielectric non-idealities in electrical and thermal analyses.

The knowledge of the gate leakage current $I_G = I_G(V_{GS}, V_{DS})$ is useful to heal from misleading interpretations deriving from the confusion of the drain current I_D (measured by the characterization apparatus) and the channel current I_{ch} modeled by triode and saturation equations in standard FETs.

Such gate-dielectric leakages have already been reported (and in some cases modeled) by literature works at different degrees of approximation by circuital models, distributed parameter analyses and MIM (Metal Insulator Metal) or MIS (Metal Insulator Semiconductor) structures characterizations [24][25][26][27].

Threshold voltages of OTFTs are estimated from $\sqrt{I_{DS}}/V_{GS}$ plots by means of the intercept method, mobilities have been extracted from the slope of the same curve in saturation regime at the same V_{DS} polarization. In considered cases, the trans-characteristics plot at V_{DS} =-16V with a varying V_{GS}, represents the saturation condition for all the examined OFETs. This has been verified by comparison with output characteristics at the same drain voltage. In these hypotheses, once known the drain current in saturation regime versus gate-voltage I_{DSSat}/V_{GS} characteristic, the mobility has been estimated from the ideal MOSFET model (see eq. 1).

eq. 1 $$\mu_p(V_{GS}) = \frac{2L}{WC_{ins}}\left(\frac{\partial\sqrt{I_{DSsat}}}{\partial V_{GS}}\right)^2$$

Where C_{ins} is the insulator surface-specific capacitance as calculated from the knowledge of the dielectric thickness (t_{ins} and the relative permittivity) in eq. 2.

eq. 2 $$C_{ins} = \frac{\varepsilon_0\varepsilon_r}{t_{ins}}$$

Channel microstructure-related properties (see [4],[25] and their references) involve charge transport and trapping, in our case by using the previous relationship and the subtended model in the case of amorphous or polycrystalline semiconductors, we expect a gate-voltage dependence of the mobility ($\mu_{FET}=\mu\ (V_{GS})$). The behavior of μ_{FET} versus the gate electrical field, has the ability to reveal the electrical, thermodynamic and material-related features of OSC/dielectric interface in the channel area. Then, a correct estimation of channel mobility can be performed only if we have knowledge of dielectric constants of adopted insulators. For these reasons, an HP4192A impedance analyzer has been employed to make capacitance voltage measurements (C/V) to extract the dielectric permittivity at low frequencies (10^2-10^3Hz). If this step could be overcome for commercial insulators like Polyimides etc., particular attention should be kept for in house made materials like PFTEOS:TEOS which, as far as we know, has still not be investigated as a dielectric for OTFTs. As a result of our measurements, we found PFTEOS:TEOS showing an elevated value if compared with polymeric low-k dielectrics (see table 6).

PMMA	ε_r=3.6
PFTEOS:TEOS	ε_r=5.1

table 6: measured dielectrics relative permittivities at f=100Hz

3.4.2 Morphology-mobility relationship

Starting from SEM imaging results on the pentacene layers grown on the top of selected dielectrics it has been possible to relate the

mobility with the dimension of grains and thus of grain boundaries as Horowitz et Al. [3] have shown for thiophenes and also in previous works. The analysis of mobility curves versus gate bias (*gate voltage-dependent mobility*) has been performed for PMMA samples and extended for a 225nm PMMA insulator treated in CF_4 plasma and subsequently in PFTEOS:TEOS and a bufferized PFTEOS:TEOS/PMMA sample.

In the case of PMMA/CF_4 treated sample the gate voltage dependent μ_{FE} has showed a typical behavior of dielectrics when surface treatments are performed. A maximum in the μ_{FE} and a value higher than the equivalent untreated sample can be observed in figure 8.

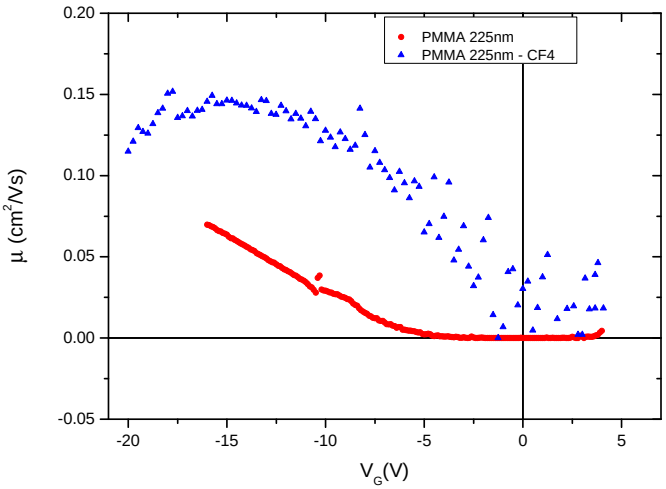


figure 8: the effect of CF4 plasma surface treatment on PMMA dielectric. The mobility exhibits a maximum point and values greater than a plain PMMA OTFT. (PMMA thickness: 225nm)

As it can be seen in figure 8, the untreated PMMA dielectric exhibits a behavior almost linear for higher gate fields, obeying to the Necliudov's empirical model[28] reported in eq. 3 which was already known for amorphous silicon (a-Si)[30] and its subsequent developments for PMMA-based OTFTs[29].

eq. 3 $$\mu = \mu_0 \left(\frac{V_{GS}-V_T}{V_{AA}}\right)^{\gamma}$$

However, in the lower neighbors of -10V gate voltages, at V_{DS} = -16V drain bias, a sign of superlinear behavior and the existence of a local maximum value which overlaps the linear behaviour. This can be attributed to the nature of the PMMA surface which for these insulator thicknesses can make behave the TFT in a way similar to treated ones.

If compared with a "plain" (*non-treated*) one, the PMMA/CF_4 sample exhibits a drastic reduction of turn-on voltage of the OTFT (which shifts from -6.17V to -1.9V as it can be observed in figure 9 and figure 10).

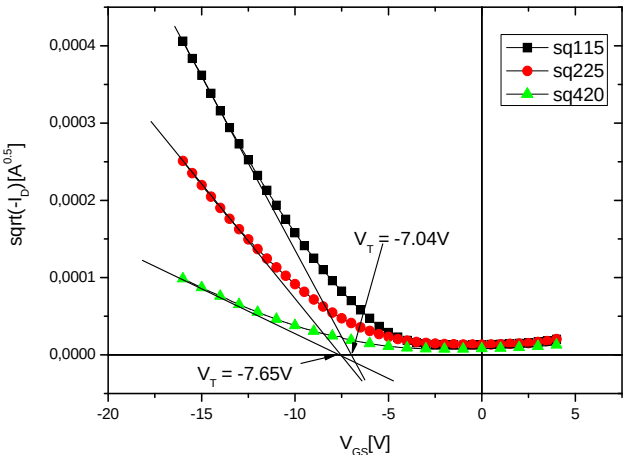


figure 9: threshold voltage extraction for PMMA samples at ambient temperature from trans-characteristics with the intercept method.

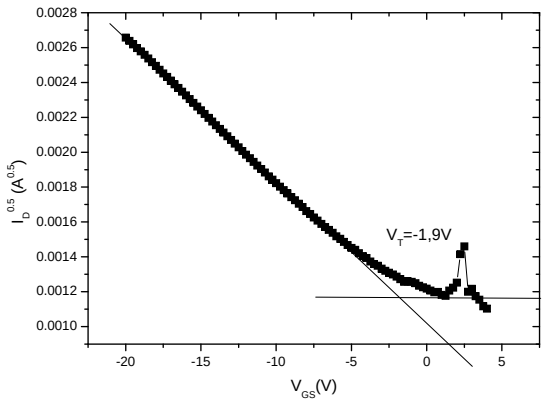


figure 10: threshold voltage extraction for the PMMA/CF_4 sample at ambient temperature

As it can be observed in figure 10, we must say that CF_4–treated OTFTs have shown very high gate-leakages when compared to untreated ones failing zero-crossing in output characteristics and trans-characteristics making them not suitable in an effective utilization for driving or switching circuitry for display or OLAE applications.

For these reasons we have decided to perform surface optimization by switching to PFTEOS:TEOS PMMA-buffering and CF_4 samples will not be taken into account. It's therefore evident that, in the case of CF_4, the nature of the treatment and its magnitude (which has already been reduced to the minimum necessary for our purposes in process optimization steps) damages from the electrical point of view the insulating film provoking the formation of preferential current shortcuts and low-resistivity paths which are responsible of the high gate-leakages obtained.

In a similar way to what we've done with PMMA225 and PMMA225/CF_4 samples, we compare the PFTEOS:TEOS sample with its bufferized version (PFTEOS:TEOS/PMMA10) in terms of gate voltage-dependent mobility (see figure 11).

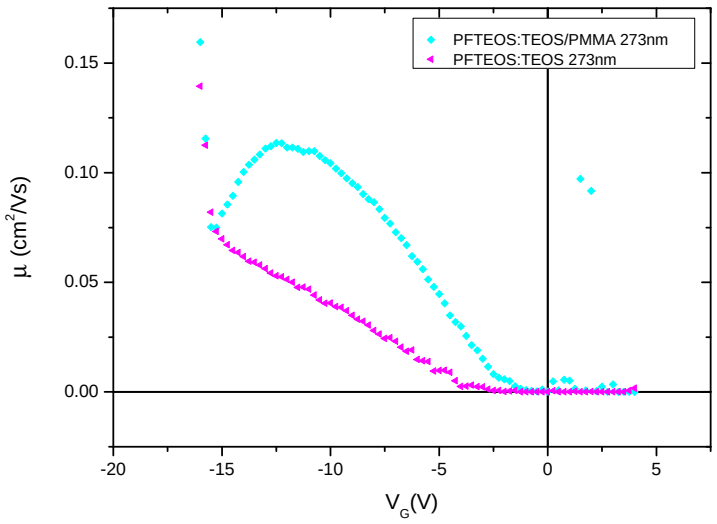


figure 11: the effect of the PMMA (10nm) buffer layer interface on PFTEOS:TEOS transistors. The gate voltage dependent mobilities are extracted from saturation trans-characteristics and compared with a reference sample.

Also in this case the enhanced structural order of the first pentacene monolayers in comparison to the plain sample evidences a general increase of the charge transport and mobility and a peak value at V_{GS}=-11V as it has already been shown for CF_4 in figure 8 and references [31].

Finally, if we compare mobility results obtained for treated and untreated dielectrics as in figure 12, and extract grain dimensions statistics from channel's SEM images, a relationship between maximum mobility and channel morphology can be graphically shown taking also into account values extracted in previous works [24][23] in figure 13.

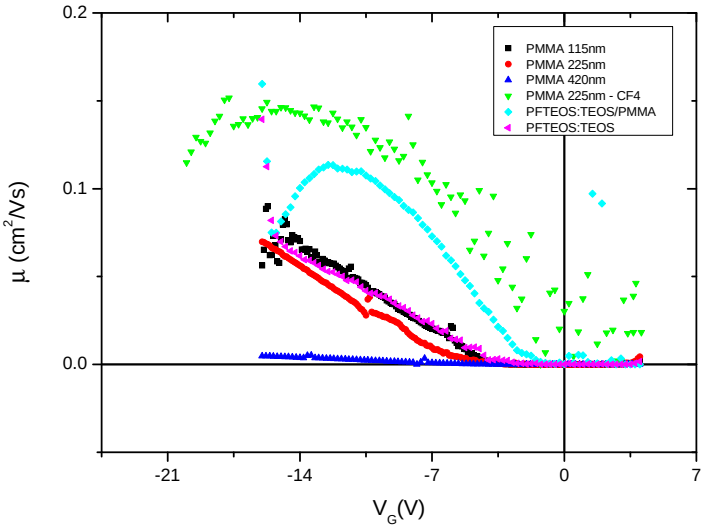


figure 12: gate voltage dependent mobility comparison for PMMA, PMMA/CF_4, PFTEOS:TEOS and PFTEOS:TEOS/PMMA devices

If we observe the figure 13 (black square symbols), it's possible to notice a generally increasing trend of charge mobility versus pentacene lateral grain dimension. This behavior is common in large grains semiconductors[3] and the limiting factor is not the grain mobility but, according to the back-to-back Schottky schematization of the grain-to-grain interface, the current flowing through a grain boundary at room temperature is limited by thermionic emission. (eq. 4).

eq. 4 $$\mu = \frac{q\bar{v}l}{8kT} e^{-\frac{E_b}{kT}}$$

Where $\bar{v}$ represents the electron mean velocity, l the grain length and E_b the activation energy.

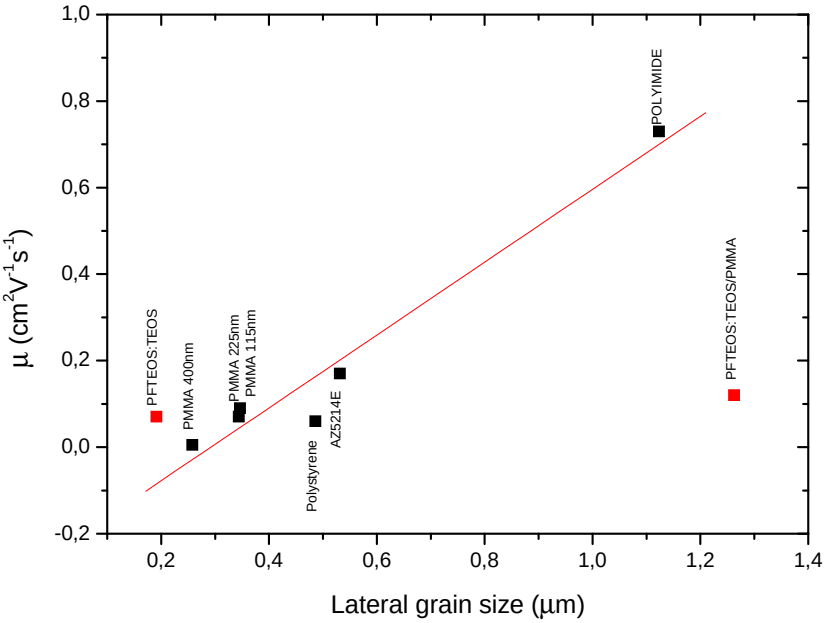


figure 13: pentacene grain dimension-mobility graph for pentacene OTFTs having the same channel thickness (65nm).

If we look at red square symbols (tagged as: "PFTEOS:TEOS" and "PFTEOS:TEOS/PMMA" names) in figure 13, it comes out that PFTEOS:TEOS and PFTEOS:TEOS/PMMA samples do not follow the same trend we noticed for polymeric dielectrics.

In more detail, the extremely hydrophobic surface of PFTEOS:TEOS film, interestingly, does not result in great grain dimensions (Wg < 0.2µm); as a second consideration we can state that the application of the buffer layer, similarly to OTFTs known from previously published papers [31] should benefit of high mobilities deriving from very large pentacene grains.

For the PFTEOS:TEOS/PMMA sample even if we obtained grains of average dimension 1.3 µm (with peak dimensions of 2µm),

we did not observed a mobility increase it should approach the unit as required by our extrapolation for polymeric materials.

To better understand this anomaly, we utilized thermal measurements to stimulate the release of trapped carriers in semiconductor film and then studying this anomaly from the point of view of interface charge traps.

3.4.3 Thermal characterizations

In thermal measurements, the disorder level of dielectric/OSC interface is probed by an indirect method to take into account the level of interconnection between pentacene grains and not only their lateral dimension. In fact, the inter-grain material portions is characterized by an amorphous phase which is strongly subjected to thermal activation, then, by acting on the temperature parameter, we go to investigate such material's regions.

In order to perform the analysis of the thermal activation process of charge transport at interface, we repeated trans-characteristics measurements and output characteristics measurements at the following temperatures: 270K, 280K, 290K, 300K, 310K, 320K, 330K, 340K.

By considering the trans-characteristic in the saturation regime, we extracted the mobility/V_{GS} curve for each temperature by using the derivative method as we already seen (eq. 1) then, we plotted the logarithm of a normalized value of μ_{FE} as a function of the reciprocal of temperature: 1000/T obtaining the so-called *Arrhenius plot*.

The curve family generated by the thermal scan of OTFT's mobility (as an example, see figure 14) has been considered for all the PMMA and PFTEOS:TEOS samples and has evidenced the presence of an isokinetic temperature (T_{MN}) [20][19] in each case and a Meyer-Neldel behavior.

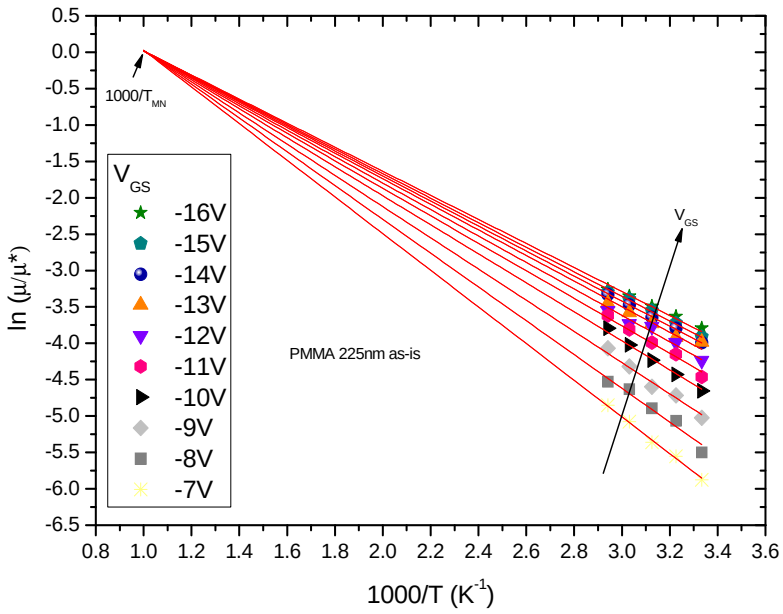


figure 14: Arrhenius plots of mobility of PMMA 225nm device at different V_{GS} voltages and their Meyer-Neldel fit necessary to extract the activation energy and the mobility prefactor.

Furthermore, from the slope of the fitting lines in Arrhenius plots, it has been possible to extract the *activation energy* (E_a) of the carrier trapping/release process, $Ea(V_{GS})$, which has been compared in figure 15.

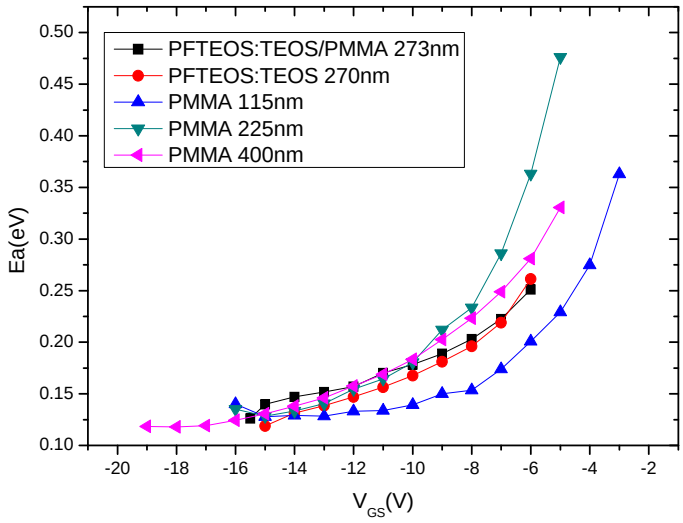


figure 15: Activation Energy (Ea(V_{GS})) graph for charge mobility in considered samples versus V_{GS} gate bias.

As it can be seen in figure 15, in every sample, activation energy decreases with gate bias but the relationship between sample's physical features and activation energy appears unclear and all the curves tend to collapse, at high gate fields to a common value of 0.12eV of activation energy and a precise trend of T_{MN} is not identified.

Our hypothesis is that a thermally-activated non-ideality phenomenon is hiding the real thermal behavior of charge mobility from our analysis. Between the main causes of device's drift from the nominal behavior there are the gate leakages as we seen in chapter 3.

Nevertheless it cannot easily be eliminated by means of the circuital equivalent we proposed in previous works [24] because the wide variation of mobility with gate field cannot be addressed in the model without losing the physical meaning of the extracted parameters. This is due to the introduction of an additional variable in the fitting of output curves in the triode region.

Thus, it appears clear that we have to extract the channel current I_{ch} from the measured drain current I_D and gate leakage I_G by following an alternative path. For these reasons we decided to change the approach and to apply the Esseni's [26] method to clear the

measured drain current from the gate leakage contribution and then performing thermal analyses for our OTFTs.

3.4.4 Gate leakage-free results and thermal analysis

As an example, if we consider the output characteristics of a PMMA 114nm gate insulator OTFT, by applying the Esseni method[26][27] at the first order (eq. 5) an estimation of the channel current can be extracted by algebraic means once measured directly I_G and I_D.

eq. 5 $$I_{ch}^{est} = \frac{I_S + I_D}{2} - \frac{I_{G0} - I_G}{6}$$

Where the meaning of symbols has already been cleared in chapter 1. This approximation is physically consistent with the expected behavior because has the ability to restore in experimental curves the zero-crossing as required from the gate leakage-free condition. Thus, the fitting of output characteristics with the ideal MOSFET model becomes easier and simulated curves are very close to estimated I_{ch} ones (compare the square symbols, the blue stars and red continuos line in figure 16 for V_G=-16V).

By applying the extraction method to all the trans-characteristics of considered transistors, we can repeat the mobility analysis which for the sake of simplicity we reported in figure 17.

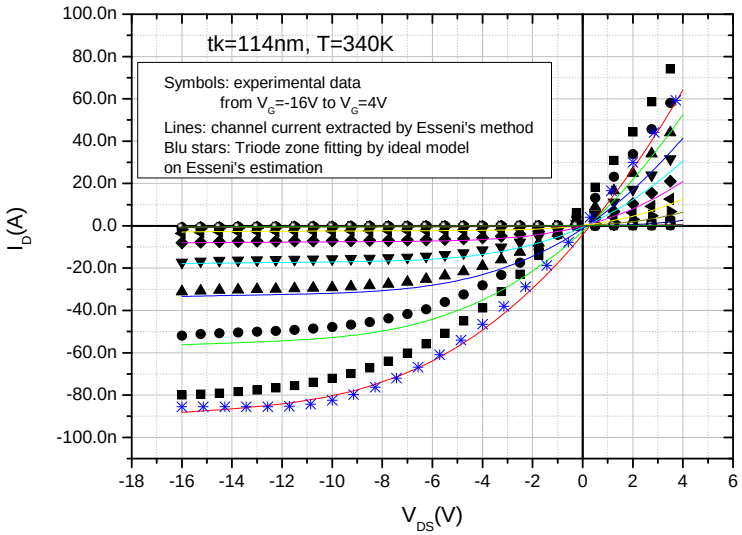


figure 16: comparison between output characteristics measured for a PMMA114 OTFT (square symbols), the Esseni's estimation of channel current (lines) and the ideal model of MOSFET.

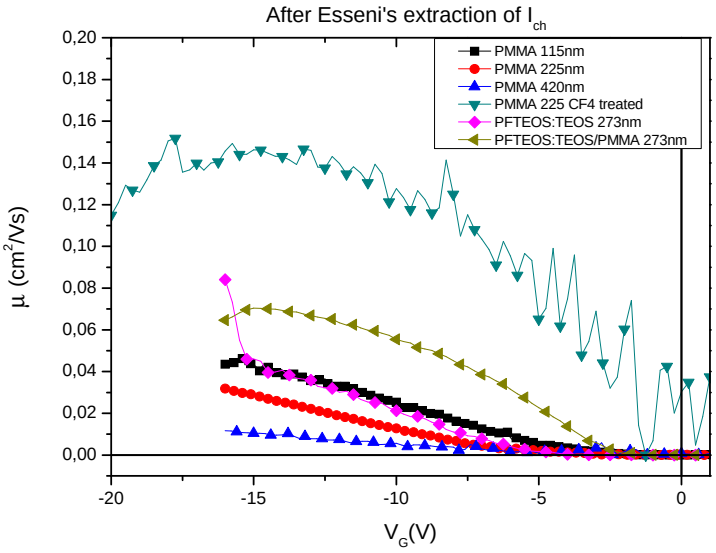


figure 17: comparison between μ_{FE}/V_{GS} channel current curves at T_{amb} after the gate leakage extraction.

It's interesting to notice in figure 17 that for surface-optimized samples the non-monotonic behaviours are preserved

(PFTEOS:TEOS/PMMA and PMMA-CF_4) and also the trend of growth of μ_{FE} as the thickness approaches to its lower limit is still obeyed (black squares, red circles and blue triangles - curves for PMMA plain samples).

The evident thing is, perhaps, that the mobility-thickness relationship in samples having the same dielectric materials has become more linear with the t_{ins} as it can be easily observed in the comparison of figure 18.

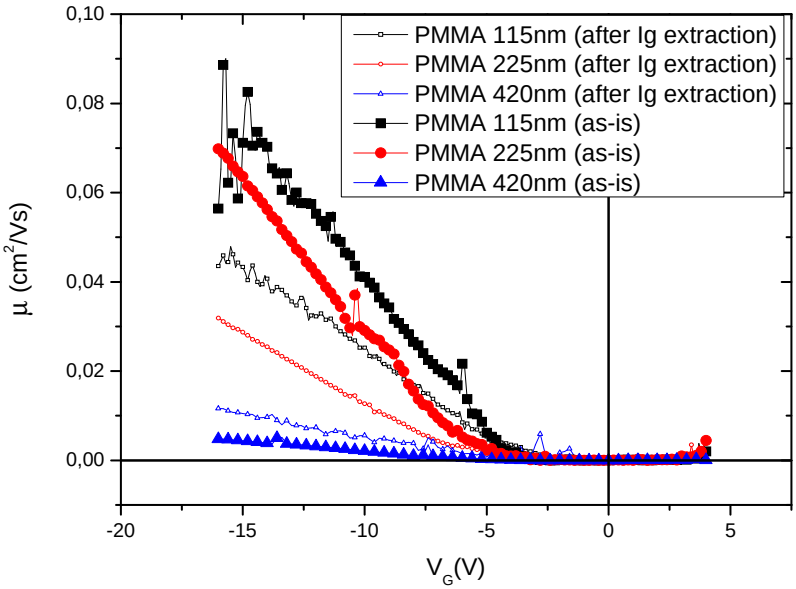


figure 18: μ/V_{GS} characteristics are compared for PMMA before (symbols) and after (lines) I_G extraction.

On this basis, it is possible to reconstruct the graph in figure 13 by using the mobility values computed on the Esseni's gate leakage-free channel current at the first order and considering the highest μ_{FE} reported in the plot in figure 19 for each sample type.

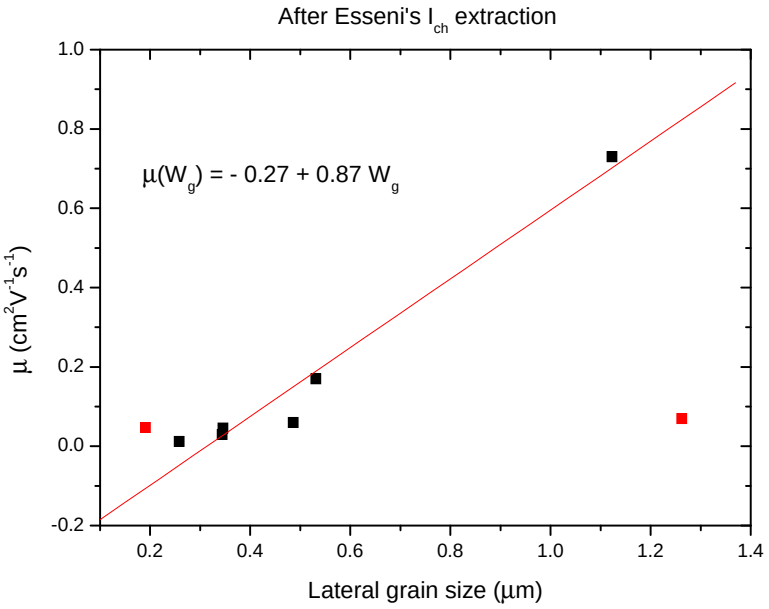


figure 19: extrapolation of a linear trend from the field-effect mobilities versus mean pentacene grain dimensions for polymeric dielectrics-based OTFTs (black symbols). Red squares are PFTEOS:TEOS samples mobilities.

As we can observe in figure 19, the mobility trend in samples having polymeric dielectric is strongly dependent from channel's morphology but also the anomaly of PFTEOS:TEOS samples is still evident if we remind figure 13.

By interpolating all the symbols but the red ones (the first on the left and the last on the right in the plot), we obtained an estimation line for transistor's performances as the channel film morphology changes.

The major differences introduced by I_{ch} estimation are, instead, evident in thermal analyses that allow now to distinguish some important features of PFTEOS:TEOS samples in comparison with PMMA samples.

Looking at figure 20, we see that the activation energy curves are now more separated and denote the dependence of the thermal activation from thickness and nature of gate dielectric in OTFTs. They still keep the usual decreasing behavior with the gate field intensity

but now it appears evident that samples having PFTEOS:TEOS as a dielectric have higher activation energies respect to the polymeric ones.

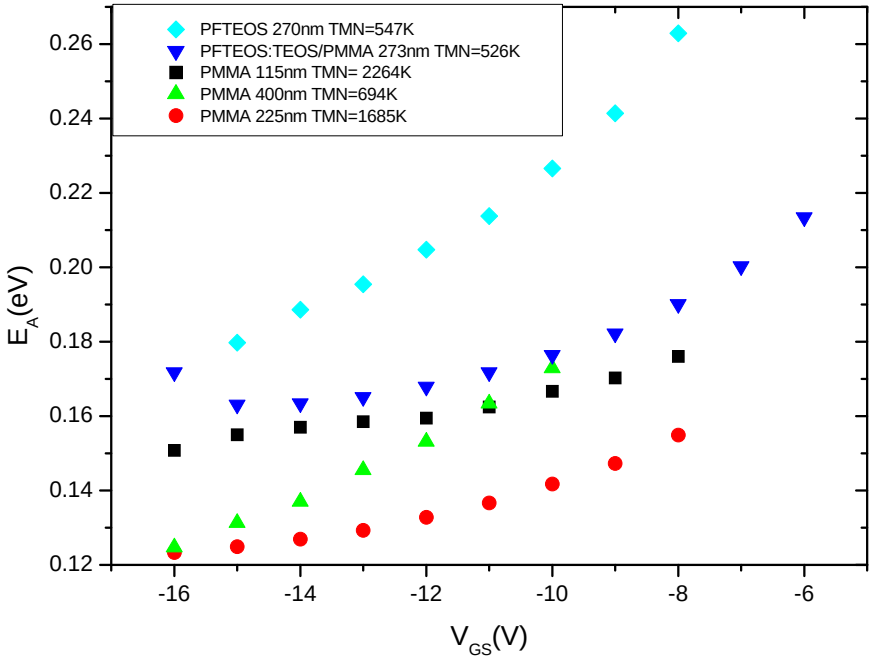


figure 20: after I_{ch} extraction, activation energies of the charge transport in PMMA and PFTEOS:TEOS samples are compared in the same plot.

Meyer-Neldel temperature (T_{MN}) analysis is another task that benefits of channel current extraction.

As we know, this factor is bound to the variance of the Gaussian DOS at OSC/dielectric interface [32][33] and then to the structural disorder in the microstructure of the conducting media. The benefit of Esseni's elaboration is clear if we compare the E_{MN}/t_{ins} plots for PMMA samples (figure 21) where it appears that for a given dielectric the Meyer-Neldel energy decreases as film becomes thicker.

In other words, the MNE seems to be for PMMA an index of the degree of control on charge channel modulation that the gate electrode effectively has.

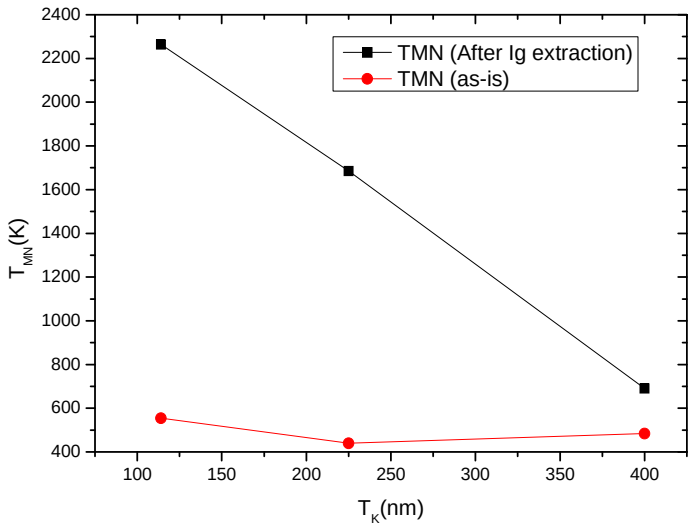


figure 21: dependence of T_{MN} and E_{MN} from pentacene grain dimension in PMMA dielectrics

From T_{MN} observation we can deduce that there's a sharp separation from the behavior of PMMA samples, having a linearly increasing trend of mobility with Meyer-Neldel energy ($E_{MN}=k_B*T_{MN}$) and the PFTEOS:TEOS ones which exhibit the opposite trend (figure 22) but also lower energetic disorder and, consequently, higher absolute values of charge mobility (figure 19).

In fact, as reported by Ullah, Fishchuk et Al. [32], in the case of disordered organic semiconductors, the charge transport can be described in terms of incoherent charge hopping. This process is thermally activated giving rise to a MNR-like dependence of charge mobility from temperature.

In the cited paper, the Density Of States in the HOMO level band is modeled by Gaussian disorder having amplitude σ which, at elevated temperatures can be estimated approximately from eq. 6 once T_{MN} is extracted and known.

eq. 6 $$T_{MN} = \frac{2\sigma}{5k_B}$$

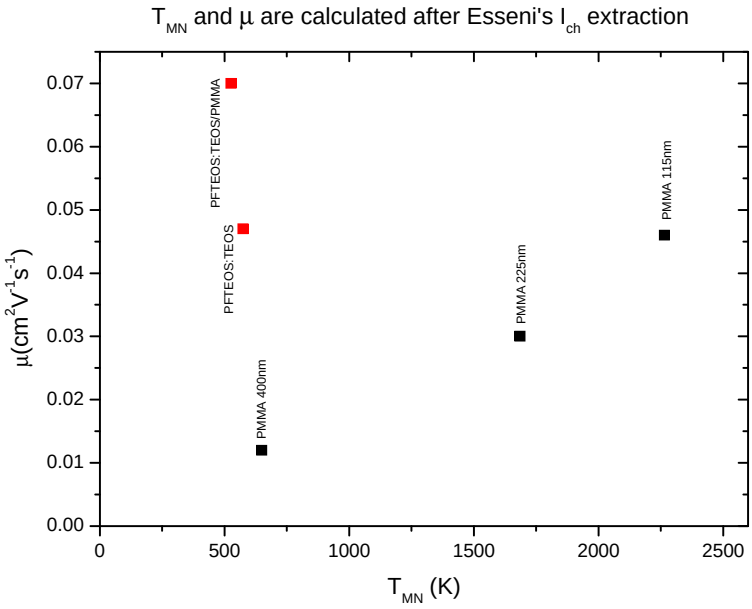


figure 22: trend inversion in mobility/EMN dependance shown by the comparison between PMMA (black squares) and PFTEOS:TEOS samples.

Then, if we refer to estimated T_{MN} for PMMA and PFTEOS:TEOS samples extracted after Esseni's modeling of Ich, we can summarize this results in the table 7.

Sample	T_{MN}(K)	σ
PMMA 115nm	2264	0.49
PMMA 225nm	1685	0.36
PMMA 420nm	649	0.14
PFTEOS:TEOS 270nm	574	0.12
PFTEOS:TEOS/PMMA 270nm	526	0.11

table 7: Gaussian DOS variance estimation by means of MNR application in PMMA and PFTEOS:TEOS samples

Such results, supply an indirect estimation of the energy disorder in the electronic states induced by dielectric interface properties by means of DC measurements at different temperatures.

We can conclude that samples having a PFTEOS:TEOS dielectric have a lower spread of states density and then a lower interface disorder and a higher charge mobility if compared with PMMA OTFTs.

For PMMA samples the T_{MN}-μ_{FE} trend seems to be inverted denoting that the thermally activated process of charge trapping and release, bound to the pre-factor of MN rule (eq. 7), overcompensates the effect of the increase of activation energy and then the behavior is dominated by grains more than by island-interconnections.

eq. 7 $$\mu_0 = e^{-\frac{Ea(V_{GS})}{k_B T}}$$

3.5 Conclusions

In the present chapter we studied the OTFT performances when varying the dielectric material. In an optimization approach, we utilized the surface wettability as a key factor to be decreased to obtain performing channels.

By following this path, a sol-gel processed organic-inorganic hybrid dielectric (PFTEOS:TEOS) has been developed and compared with plain polymeric dielectrics. A surface treatment and a bufferization process have been studied and analyzed and results utilized to relate pentacene grain dimension to charge transport. This relationship has been analyzed showing the anomaly in the behavior of PFTEOS:TEOS innovative insulators if compared to a wide class of polymeric dielectrics.

Thermal analyses of charge transport activation for the considered samples have been performed showing a general validity of the MNR also for hybrid dielectrics but the extraction of energetic parameters in Arrhenius plots applied to static electrical characterizations, has

revealed differences of maximum mobility trends versus E_{MN} between polymer dielectric-based OTFTs and PFTEOS:TEOS-based OTFTs.

The differences in dielectric/OSC interface have shown to be correlated to the isokinetic temperature and activation energy and then to the disorder parameter σ of the DOS in the HOMO band tail. Thus, instead of considering the contribution of band density of states, the amplitude of the distribution of energetic states has been exploited in the investigation of surface properties and dielectric-specific features remarked.

The activation energy analysis shows a trend inversion in the T_{MN}/mobility relationship between PMMA samples and PFTEOS:TEOS samples revealing an effect induced by the very nature of insulator rather than the OSC/dielectric interface on thermally activated processes. The dielectric is then responsible of a wide range of thermal behaviours in the thermal response of disordered OSC used in OTFTs.

Given the original use of PFTEOS:TEOS in organic electronics applications and more in detail in OTFTs, once we considered the anomalies that it has shown respect polymer dielectric-based transistors in terms of energetic order/disorder effects on pentacene channels, further investigations have to be done on this class of materials in OE together with non-conventional gate/channel interface materials.

In this line of work, thermal analyses have proven to be a key discriminant factor to address non-conventional dielectrics surface-features characterizations in electronic devices.

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Conclusions

In this PhD dissertation the role played by the gate dielectric in the electrical performances of organic transistors is presented.

The key aspects which have been investigated about dielectrics are the gate leakages and the models to extract the channel current, the relationship between wettability of dielectric surfaces and the growth of pentacene and then, the channel morphology and charge transport.

Another important factor is the optimization of the device when keeping in mind that optimum performances are reached not just with an OTFT having high values of charge mobility but also low threshold voltages, low operation voltages, high saturation currents and low gate dissipations. In order to obtain an optimized device, a process layout and flowchart has been designed and stencils utilized to make pattering of evaporated contacts and OSC islands.

This manufacturing method has been chosen because other potentially more precise techniques have been evaluated and not taken into account because they did not guarantee a working device and good performances.

One of the caveats of analyzed OTFTs was the gate-leakage. This non-ideal component has been studied by means of a specific circuital model which has been developed from experimental data to explicit the dependence between gate-to-contact currents from polarization voltages in the OTFT.

Annealing effects have been analyzed by means of the developed circuital model on fabricated devices in the aim to reduce, in some cases, gate dissipations. As a result of this analysis, we found Polyimide to be from the point of view of mobility an optimum gate dielectric after a simple low-temperature rapid annealing. But considering this device performances, thinking about applications such device has to carry on, it was mandatory to obtain lower working voltages by reducing the insulator thickness. But we found Polyimides to be not easy to dilute and spin in continuous defect-free film thicknesses under 1 microns. Thus, polyimide had to be abandoned in favor of more processable materials like PMMA. In order to reduce

gate leakages in case of thin dielectrics, the security mechanism had to be hardwired into the process flowchart without relying on the effects of annealing.

For these reasons, the optimized layout designed and adopted to build OTFTs had patterned gates and reduced the overlap area between contacts and OSC.

The utilization of gate leakage model also enabled us to estimate mobility-pentacene grain size trend relationship. In the case of PMMA devices and other thin dielectrics, the dependence of field-effect mobility from gate field made the performance analysis not affordable if faced with a simple circuital model. In these cases a model used in inorganic electronics for leaky dielectrics has been adopted after Palestri, Esseni et Al. Such distributed-parameter model proved to be effective also with OTFTs and was employed to investigate grain size-mobility trend for an extended class of devices.

The utilization of PMMA as thin gate dielectric evidenced a low mobility value, thus we worked on this parameter by changing the nature and surface state of the insulator. From this point of view, we developed a novel gate insulator material PFTEOS:TEOS which is and organic-inorganic material processable by sol-gel technique from a solution. Devices based on this kind of material exhibited improved performances respect to the plain dielectrics but break the relationship between grain dimensions and mobility.

Anomalies which have been noticed for PFTEOS:TEOS and its optimized version PFTEOS:TEOS/PMMA obtained from buffer layer deposition have been investigated and compared to other polymeric dielectrics with their varying nature and thickness. In order to do this, thermal analyses have been performed. A Meyer-Neldel rule general observation was found to be obeyed in every analyzed case, thus activation energy and Meyer Neldel temperature were exploited to characterize energetic disorder at OSC/insulator interface by Gaussian disorder model for Density of Band states.

In conclusion the behavior of a novel sol-gel gate insulator has been characterized and analyzed comparing it to plain cases and finding an original behavior of E_{MN}/mobility/Activation energy which exhibits an inverse (decreasing) trend between energetic disorder and charge transport. This has been completely opposite to trends found for PMMA devices encouraging studying, exploiting and

characterizing more in depth this material for Organic Electronics purposes.

The development of the organic thin film transistors is evolving quickly and most of the efforts are being focused on the overcoming of the technological limits which make the employment of these devices in integrated circuits complex, in particular in large area applications (typical characteristic of flexible display).

Further efforts are to be invested whereas it is possible to glimpse the possibility of improvement concerning the development of n-type channel materials, the addressing of the structures patterning issues, problems related to surface upscaling and device downscaling. Also further researches have to be done in self-aligned processing (consequent reduction of gate overlaps). Low-cost and high-productivity deposition methods should be developed by vacuum-free deposition techniques and finally the implementation of high-efficiency complementary logics should be reached.

The research on the OE field has to face all these challenges and even more, other ones, so that this new technology can assert itself and become competitive covering the market sectors left still partially unexplored by the inorganic electronic technology.

Table of acronyms and symbols

Symbol	***Description***	***units***
AC	Alternate Current	
a-Si	Amorphous silicon	
BGBC	Bottom-Gate/ Bottom-Contacts	
BGTC	Bottom-Gate/Top-Contacts	
C/V	Capacitance/Voltage measurements	
C_{ins}	Gate Specific Capacitance	F/cm^2
Da, u	Mass Atomic Unit	
DC	Direct Current	
DI	DeIonized (water)	
DUV	Deep-UV radiation	
$\underline{\mathcal{E}}$	Electric field (its components have the subscript – i.e.: $\mathcal{E}_x$)	V/cm
E_a, E_A	Activation Energy	eV
E_G	Semiconductor's Bandgap (E_C-E_V)	eV
FET	Field-Effect Transistor	
GCA	Gradual Channel Approximation	
HMDS	Hexamethyldisilazane	

HOMO	Highest Occupied Molecular Orbital	
hr	Hour	
IJP	Ink-Jet Printing	
LUMO	Lowest Unoccupied Molecular Orbital	
MNE	Meyer-Neldel Energy	eV
MNR	Meyer-Neldel Rule	
MISFET	Metal-Insulator Semiconductor Field-Effect Transistor	
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor	
NP	NanoParticles	
OFET	Organic Field-Effect Transistor	
OLAE	Organic Large-Area Electronics	
OLED	Organic Light-Emitting Diode	
OSC	Organic SemiConductor	
OTFT	Organic Thin-Film Transistor	
OTS	Octadecyltrichlorosilane (chemical compound)	
P5	Pentacene, $C_{22}H_{14}$	
PANI	Polyaniline	
PC	PhtaloCyanine	
PECVD	Plasma-Enhanced Chemical Vapour Deposition	

PFTEOS	1H,1H,2H,2H-Perfluorodecyl triethoxysilane	
PMMA	Poly(methyl methacrylate)	
PVP	Polyvinyl phenol	
Ra	Mean Roughness	nm
Rq	Root Mean Square Roughness	nm
RPM	Revolutions per minute	
RPSQM	Revolutions per squared minute	
SAM	Self-Assembled Monolayer	
SAMT	Self-Assembled MulTilayer	
SCS	Semiconductor Characterization System	
SEM	Scanning Electron Microscope	
SiN_x	Silicon Nitride	
TEOS	Tetraethyl Orthosilicate	
TGBC	Top-Gate/Bottom-Contacts	
TGTC	Top-Gate/Top-Contacts	
T_{MN}	Meyer-Neldel Temperature	K
UV	Ultra-Violet (radiation)	
VLSI	Very Large Scale Integration	
W_F	Workfunction	eV
μ_{FE}	Field-effect mobility	$cm^2/V^{-1}s^{-1}$
µc-Si	Micro-crystalline silicon	