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TESI DI DOTTORATO

Models and methods for the design of isolated power converters in high-frequency high-efficiency applications

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I dedicate this achievement
to my sister Alessia

Thank you for your support, encouragement and love.

Also to my parents

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Giulia

Contents

Introduction

Power supply technology is an enabling technology that allows us to build and operate electronic circuits and systems [1].

Today, many electronic systems require several dc supply voltages, which are usually derived from a battery or an ac utility line using a transformer, rectifier and filter. The resultant dc voltage is not constant enough and may contain a high ac ripple that is not appropriate for most applications. Voltage regulators are used to make the dc voltage more constant and to attenuate the ac ripple. A Power Supply (PS) is a constant voltage source with a maximum current capability.

PSs are used in telecommunications, instrumentation equipments, computers, aerospace, automotive, motor control, renewable energy, medical, lighting, defense electronics; in other words, wherever efficient energy processing is needed. Designers needs to properly select the technology of each PS, according to system finality in which it is going to work [2][3]. Important issues influencing this choice are:

- cost;
- efficiency;
- weight and volume;
- heat dissipation;
- reliability;
- number of required output voltages;
- EMI;
- time-to-market.

There are two general classes of PS: *regulated* and *unregulated*. The output voltage of a regulated PS is automatically maintained within a narrow range, *1÷2%* of the desired nominal value, in spite of line voltage, load current, and temperature variations. A regulated dc PS is also called dc voltage regulator.

Two major power supply technologies can be recognized in the development of regulated power supplies system: *linear* regulators and *switching-mode* power supplies [1]-[3].

In linear voltage regulators, transistors are operated in active region as dependent current sources, with relatively high voltage drops at high currents, dissipating a large amount of power and resulting in low efficiency (around *35-50*%). Because their losses are dissipated as heat, linear regulators are commonly used in equipments where heat generation and low efficiency are not of major concern. However, they exhibit low noise level, resulting suitable for audio applications, data converters and wherever low cost and quick design are desired.

In switching-mode converters, transistors are operated as switches, which inherently dissipate much less power than transistors operating as dependent current sources. The voltage drop across the transistors is very low when they conduct high current and the transistors conduct a nearly zero current when the voltage drop across them is high. Therefore, the conduction losses are low and the efficiency of switching-mode converters is high, usually above *85–95*%.

In switching-mode converters two main PS technologies can be found: *PWM* regulators and *resonant* regulators. Both can be used at high power and voltage levels, are small in size, light in weight, and may achieve high conversion efficiency. PWM regulators are more efficient and flexible in their use than linear regulators [4][5]. Their weight is much less that linear regulators, since they require less heatsinking for the same output ratings. However, because of switching losses increase proportionally to switching frequency, losses reduce the efficiency at high frequencies. Resonant converters are commonly used in applications where still lighter weight and smaller size are desired and, above all, a reduced amount of noise is acceptable [5].

Both PWM and resonant switching-mode converters are more expensive and require more engineering development, and are adopted as in *non-isolated* as in *isolated* conversion [5]. In a large number of applications, dc isolation between the input and output of the converter is desired: for example, in all off-line applications, where the input of the converter is directly connected to the ac utility system. In such a case, transformer is introduced into the switching converter

because of isolation requirements. Moreover, when a large step-up or step-down conversion ratio is required by the application specifications, the use of a power transformer can allow to achieve better converter optimization due to the distribution of stresses among power components, compared with non isolated topologies. In fact, by proper combined choice of transformer and silicon devices, voltage and current stresses on transistors and total power losses can be minimized, improving both efficiency and cost of the switching-mode isolated converter. Isolated converters are also very effective solutions in multi-output power supplies, thanks to the use of multiple secondary windings transformers. The counterpart of benefits offered by transformers lies in the need of a careful design at system level in order to achieve a good trade-off among overall performances, size, cost and reliability.

PWM converters usually work under *hard switching* conditions, with semiconductor devices voltages and currents changing abruptly from high values to zero and vice-versa at turn-on and turn-off, thus causing switching losses and a great amount of electromagnetic interference noise (EMI) [4]. In PWM dc–dc converters, higher power density and faster transition response can be obtained mostly by increasing the switching frequency. Nevertheless, as the switching frequency increases, efficiency decreases and EMI increase as, when MOSFETs are used as switching device in power converters, the losses occurring due to the charge/discharge of their parasitic capacitances increase with frequency [6]. In order to reduce losses and improve PWM converters efficiency, improved semiconductor devices and magnetic materials have been developed over the last decades [7]. For example, NexFET™ technology is a new generation of silicon-based power MOSFETs with an inherently low-charge structure and very low on resistance and parasitic capacitances [8]. NexFET™ technology delivers high performance for both N and P channel power MOSFET devices, increasing efficiency in existing switching converters, as well as enabling the next generation of switching power converters operating at switching frequency of several *MHz*. In high voltage MOSFETs panorama, CoolMOS™ is an interesting technology of power MOSFETs, characterized by reduced gate charge, optimized gate threshold voltage for soft-switching, good body-diode

ruggedness, improved *dv*/*dt* [8]. All these features permit to achieve improved efficiency.

In isolated converters, the transformer leakage inductance forms resonant circuits with the silicon devices parasitic capacitances, causing ringing phenomena, which can lead to efficiency degradation, unless they are adequately exploited to realize some form of *soft-switching*. Indeed, switching losses and EMI level in PWM converters can be both reduced by *soft switching* techniques. Numerous *soft-switching* circuit techniques have been proposed and discussed in the literature for reducing the voltage-current product during the switching transitions [10]-[14].

The soft-switching techniques can be divided into two categories: zero-voltage switching (ZVS) and zero-current switching (ZCS). In the ZVS technique [11]-[13], the voltage across the transistor is zero when the transistor is turned on. Therefore, the energy stored in the transistor output capacitance is zero at turn-on. Hence, the turn-on switching loss is also zero, yielding high efficiency. While in ZVS technique a semiconductor device turns on at zero voltage, in ZCS technique [14] a semiconductor device turns off at zero current. When semiconductor devices turn-on or turn-off at zero voltage or zero current, the product of the device voltage and current during the transitions is dramatically reduced, thus eliminating switching losses problem, thus allowing high switching frequencies and then smaller size and weight of power converters. The harmonic content of the current and voltage waveforms is also reduced, yielding a lower level of EMI. Unfortunately, soft-switching techniques are accompanied by an increase of conduction losses, unless more sophisticated configurations are used, involving the use of additional silicon devices and precise drive synchronization, which make the true achievement of soft-switching more critical and the global cost of the converter much higher.

Resonant and quasi-resonant converters are switching power supplies that “tune” the ac power waveform to reduce or also eliminate the switching losses within power supplies, by placing resonant tank circuits within the ac current paths, in order to create pseudo-sinusoidal voltage or current waveforms. Smaller size and also typically higher efficiency can be achieved in resonant regulators

[15][16], even if switching losses are not the only frequency-dependent losses (e.g. in magnetic devices, where frequency influences both core losses and copper losses, through skin and proximity effects). Indeed, the trend toward high power density, high efficiency, and low profile in power supplies has exposed a number of limitations in the use of magnetic component structures too [17][18].

There are many resonant converter topologies, and they all operate in essentially the same way: a square pulse of voltage or current generated by the power switches is applied to a resonant circuit. Energy circulates in the resonant circuit, and some or all of it is then tapped off to supply the output. More detailed descriptions and discussions can be found in [19]-[22]. Resonant converters, especially those with an LLC half-bridge configuration (two inductors, *LL*, and a capacitor, *C*, also known as *LLC* configuration) are well suited for magnetic integration, permitting combination of inductors and transformer into a single magnetic device, with consequent higher achieved power density [23]. However, as a main disadvantage, these converters work with a variable switching frequency to control the dc output voltage. Indeed, because the tank circuits have only one resonant frequency, a variable frequency control is required, which can vary the converter period, keeping fixed the resonant period. Moreover, in these power converters voltage and current stress and conduction losses are usually higher: peak voltages and current values can be two or also three times higher than in PWM converters. As a consequence, higher rated power switches and rectifiers are needed, which however may not have very good conduction characteristics.

High-efficiency high power density with PMW converters are achievable by lowering voltage and current cross-over point during turn-on and turn-off transitions, minimizing effects of reverse recovery in rectifiers, reducing spikes created by parasitic elements, recovering as much of loss energy as possible and returning it to the power flow of the power supply. In order to achieve these objectives, some modifications to the standard PWM topologies can be adopted, like for example including active clamp reset of transformer in isolated converter [24]-[26], and even using new enhanced hybrid hard-switching/soft-switching techniques [27].

Today growing popularity of the LLC resonant converter in bridge and half-bridge implementation is due to its high efficiency, low level of EMI emissions, and its ability to achieve high power density. Such features perfectly fit the power supply demand of many modern applications. In particular, several innovative techniques have been proposed for increasing the power conversion efficiency of such converters at high frequencies and many frequency-controlled resonant converters equipped with synchronous output rectifiers have been proposed in the literature for high efficiency operation at high input and low output voltage applications. However, a real difficulty is encountered by engineers working with this topology: the lack of information concerning the way the converter really operates in wide input or output range applications, for example, and, therefore, the way to design it in order to optimize its features.

On the contrary, new interesting features in semiconductor devices together with higher efficiency technologies, like active clamp transformer reset and secondary side synchronous rectification in isolated converter, are becoming even more attractive issues. As a result, the new trend in power technology is towards combining the simplicity of PWM converters with the soft-switching characteristics of resonant converters. ZVS/ZVC switching commutations of power devices are achievable while the power transfer is realized by using simpler PMW techniques, with evident efficiency improvement especially in isolated converters (e.g. Forward and Flyback).

In this regard, the impact of transformer leakage inductance and other circuit parasitic parameters (stray inductances and MOSFET capacitances) on isolated converter efficiency is an almost attractive topic. The influence of transformer leakage and magnetizing inductances on Active-Clamp-based converters can be properly considered, in order to find optimal compromise between the devices size and amplitude of the load range where soft-switching is guaranteed. Moreover, magnetizing and leakage inductance values should be explicitly taken into account in the efficiency evaluation of the design solutions, in order to avoid excessive magnetizing current, nevertheless permitting to store enough energy enabling active clamping reset. The jointly transformer and silicon devices selection can be investigated too, in order to guarantee overall high-efficiency high-power-density design solutions.

Considerations

The scenario depicted above makes the design of power supplies a decision matter: which is the most appropriate arrangement of topology, operation mode and power devices for a given application?

What is very important is that the answer to this question is customized to real world, the world of power designers who need to achieve a good solution for a real product which must comply with technical specifications but also with material and economical needs and market requirements, such as size, weight, cost, time to market, competitiveness. Such constraints become as much stressing as the application context moves from the very high-power, such as in railway traction systems, where the system development can take a long time and the panel of possible design solutions is sometimes very limited, to low powers, such as in telecom, consumer electronics and portable electronics, where few cents make a difference in projects going from hundred thousand to hundred million pieces. In such contexts, it is not uncommon the demand to power designers to deliver a working prototype of a low-power supply within few weeks, and sometimes in few days. In that time, a number of decisions have to be fixed (topology, operation mode, control type, silicon and passive power devices), based on a synoptic quantitative evaluation of the overall elements characterizing the performances of each design solution.

WEB based power design tool such as the WEBENCH® from former National Semiconductor Corporation, now Texas Instruments, fit the demand for quick and reliable search of feasible power supplies design solutions. Most of the silicon and passive power devices manufacturers are now providing WEB based design tools helping designers to quickly evaluate parts given the context application.

Sound models, numerical methods, design techniques and decision criteria are needed to setup effective algorithms allowing a quick and reliable investigation of power supplies design solution. To this aim, it is of paramount importance to achieve an adequate trade-off among:

- the depth of physical models of devices and their coherence with the realistic knowledge of the final board characteristics (e.g. printed circuit board layout parasitic);
- the practical outcome of design methods (using the available parameters of existing real parts as base for the calculations);
- the time sustainability and the reliability of numerical algorithms (intended as the summa of convergence of the algorithms plus repetitiveness and correctness of the results).

In the modern context of low-power supplies design, what a good computer aided design tool has to guarantee is to provide a fair comparison among manifold differentiated design solutions and options, starting from which, a design choice can be done to quickly pass to the second step of the in-depth system analysis and board engineering.

The aim of this PhD dissertation is to discuss the fundamental issues regarding the design of high-efficiency high-power-density isolated power converters, related to the transformers design and to the system-level analysis of functional and parametric correlations existing among transformers and silicon devices in the achievement of high efficiency.

The research results presented in this PhD dissertation consist in models, methods and algorithms for the design of high-frequency and high efficiency in isolated switching-type converters. Achieving this goals has required an interdisciplinary study, which involved modeling problems of both magnetic devices and solid-state devices, with critical aspects on numerical and experimental issues.

The dissertation is organized as follows.

In Chapter 1, a brief review on isolated power converters topologies is firstly given.

In Chapter 2, a novel design approach for custom transformer design is proposed, highlighting challenging correlations among the magnetic core geometrical characteristics and the application in which each type of core might guarantee major advantages in terms of minimizing losses and/or sizing.

Thermal properties of magnetic devices, needed for a complete magneto-electro-thermal modeling of the transformer, are discussed in Chapter 3.

In Chapter 4, a novel versatile numerical method for the analysis of MOSFETs commutations and the evaluation of related losses in synchronous rectification switching cells has been proposed and investigated.

Finally, in Chapter 5, the mutual constraint conditions between magnetic devices and solid state devices in isolated converters have been investigated.

Chapter 6 is the summary of this work and illustrates future work.

This dissertation contains four chapters presenting results published in journals and conference proceedings. The complete citations for these papers and the chapters in which they appear are provided in the following:

Chapter 2 – Transformer Design Methods for Isolated Converters

- A. De Nardo, G. Di Capua, N. Femia, "*Transformer Design for Isolated Switching Converters Based on Geometric Form Factors of Magnetic Cores*", IEEE Transactions on Industrial Electronics, vol. 60, no. 6, pp. 2158-2166, June 2013.
- A. De Nardo, G. Di Capua, N. Femia, G. Petrone, G. Spagnuolo, "*Geometric-constants-based design of transformers for isolated switching converters*", Proceedings of 2010 IEEE International Symposium on Industrial Electronics (ISIE 2010), pp.844-849, Bari, Italy, 4-7 July 2010.

Chapter 3 – Temperature Effects on Transformers Design Constraints

- G. Di Capua, N. Femia, "*A novel approach to transformers design based on acceptability boundary curves of magnetic cores*", Proceedings of 2010 IEEE 12th Workshop on Control and Modeling for Power Electronics (COMPEL 2010), pp.1-8, Boulder, Colorado (USA), 28-30 June 2010.

Chapter 4 – MOSFETs Commutations Analysis

- G. Di Capua, N. Femia, "*A Versatile Method for MOSFETs Commutations Analysis in Switching Power Converters Design*", accepted for publication in IEEE Transaction on Power Electronics (TPEL-Reg-2012-12-1764).
- G. Di Capua, N. Femia, "*Modeling Switching Losses in MOSFETs Half-Bridges*", Proceedings of 2012 IEEE International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD 2012), pp. 93-96, Seville, Spain, 19-21 September 2012.

Chapter 5 – System Level Analysis of an Active Clamp based Forward Converter

- G. Di Capua, N. Femia, "*Minimizing Power Components of Isolated DC-DC Converters*", Proceedings of 2012 European Power Conversion Intelligent Motion Conference (PCIM 2012), pp. 1108- 1115, Nuremberg, Germany, 8-10 May 2012.

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Chapter 1

Switching Mode Power Supplies Isolated Converter

1.1 Isolated Converters Overview

Isolated converters are required to provide electrical isolation between a high voltage source and a low voltage load. Galvanic isolation is required between the power source and the load both in off-line ac-dc applications and in high-voltage dc–dc power supplies in order to meet safety specifications, ensuring that there will be no shock hazard in using the equipment. Many safety requirements and standards have been established over last decades by different all over the world agencies (e.g. IEC in Europe or UL in the United States): all these isolation related specifications involved both electrical and mechanical issues, which may finally result as limiting factors in the design of Isolated Switch-Mode Power Supplies.

Isolation must be provided and guaranteed between all the input and output stages of the power converter and in the control loop too. In the power stage galvanic isolation is typically achieved through use of a transformer, which provides good dielectric barrier between involved parts; in the feedback/control loop isolation is often provided through an opto-isolator [1] or digital couplers [2].

In particular, the transformer inclusion in the converter power stage ensures that:

- secondary side circuits are protected from potentially dangerous transient voltages and currents present on the primary side of isolation;
- ground loops between primary and secondary side are removed, increasing noise immunity of the secondary supply;
- possible multiple outputs are achievable;

- input voltage stepping up or stepping down is allowed;
- a negative supply from a positive supply and vice-versa is possible.

1.2 Isolated Converters Topologies

In this section the principal isolated converters topologies are briefly discussed.

Flyback Converter

The flyback converter [3] is a buck-boost derived topology (Figure 1.1). Its isolation is ensured by means of a *flyback transformer*, where the current does not simultaneously flow in the primary and secondary side. The converter uses a single FET to energize the transformer, utilizes a single-output diode, and does not need an output inductor, as this is embedded into the transformer. As a result, the current to the output winding is discontinuous and the output voltage ripple will be greater. The transformer is automatically reset by the output voltage during the off period and therefore does not require a reset winding.

A flyback topology is typically the favorite topology for an isolated power supply when a simple low-cost solution is required. Flyback topologies are also very useful for generating multiple voltages: usually, only a single output is regulated, but it is straightforward to add windings to the transformer for additional voltage rails. A flyback converter is generally acceptable up to an output level no greater than 150W. Above this power level, other topologies should be considered. In comparison to all of the other isolated topologies, the flyback topology uses the least components and therefore typically has the smallest footprint, particularly at low power levels.

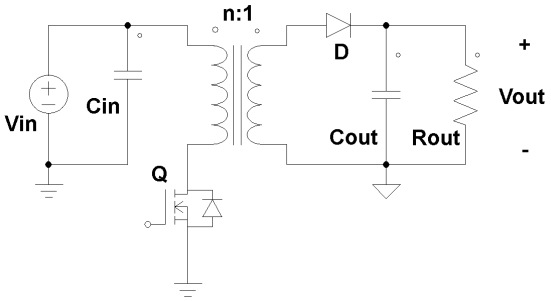


Figure 1.1. Flyback Converter Circuit.

Forward Converter

The forward converter [3] is a buck derived topology (Figure 1.2). This topology uses a reset winding on the transformer to reset it. In particular, the maximum duty cycle is set to less than 50%, if the turns number of the reset winding is the same of the turns number of the primary winding. The forward converter is relatively simple compared to the bridge topologies, making it a popular choice for isolated supplies up to about 200W of output power. Like the flyback converter, it uses a single MOSFET to magnetize the primary of the transformer. However, because a forward is buck derived, the output inductor ensures continuous current flow to the output capacitor, which reduces the RMS ripple currents in it.

Active Clamp Forward Converter

The active clamp transformer reset technique offers many well-documented advantages over traditional single-ended reset techniques [4]-[6]. This reset technique might be implemented through nor an High-Side (Figure 1.3(a)) nor a Low-Side (Figure 1.3(b)) active clamp circuit. In particular, the addition of the active clamp to the forward converter allows the realization of greater efficiencies through the use of synchronous MOSFETs, the reduction of switching losses and EMI in the primary MOSFET due to zero voltage switching, and the non-dissipative reset of the transformer, recycling the leakage inductive energy back to the input. Traditional diodes rectification at the secondary side is possibly replaced by synchronous rectification (see Figure 1.3), especially in high current applications, ensuring higher efficiency.

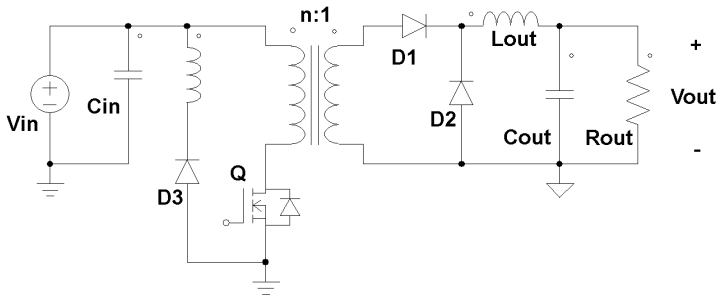
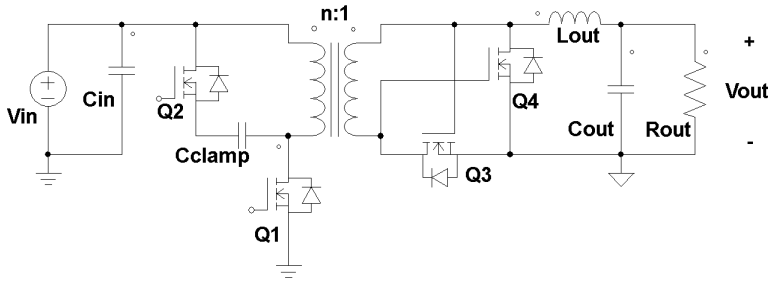
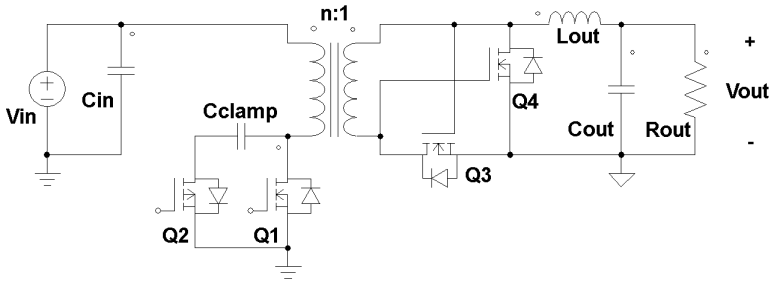


Figure 1.2. Forward Converter Circuit.



(a)



(b)

Figure 1.3 Active Clamp Forward Converter Circuit, with High Side reset (a) and Low Side reset (b).

Push-Pull Converter

The push-pull converter [3] is an interleaved forward converter, whose primary winding is made up of a center-tapped transformer (Figure 1.4). This converter uses a transformer with center-tapped both at primary and at secondary side. Ideal for higher power designs above 200W, the push-pull converter has all the benefits of a forward converter, while exhibiting lower input and output ripple currents compared to the forward, thus having smaller filter components. However, the MOSFETs of a push-pull converter need to be rated at twice the input voltage. Moreover, the push-pull converter typically has flux imbalances in the transformer and, as a result, magnetizing current is not reset to zero. Over consecutive cycles, the flux density in the core accumulates to higher and higher levels, eventually driving the core into saturation. Therefore, current-mode control should be used to ensure proper and complete reset of the transformer.

Half-Bridge and Full-Bridge Converter

The half-bridge and the full-bridge converter [3] are buck derived topologies (Figure 1.5 and 1.6, respectively). These converters use a transformer with center-tapped at the secondary side and are typically used in switching power supplies at power levels of approximately 250W and 750W, respectively. The utilization of the transformer is quite good, because its magnetizing current can be both positive and negative and the total core *B-H* loop can thus be used.

The half-bridge configuration requires only two transistors, which however must handle currents that are twice as large as those of the full-bridge converter. As a consequence, half-bridge is usually adopted for lower power levels, where transistors with sufficient current rating are readily available and where low parts count is important. Due to the differences in capacitances C_1 and C_2, the voltage across them will not be identical and current-mode control will worsen the voltage imbalance, causing the half-bridge to stop working. The full-bridge is usually used at higher power levels, because of its high parts count, which include four transistors and their associated driver circuits.

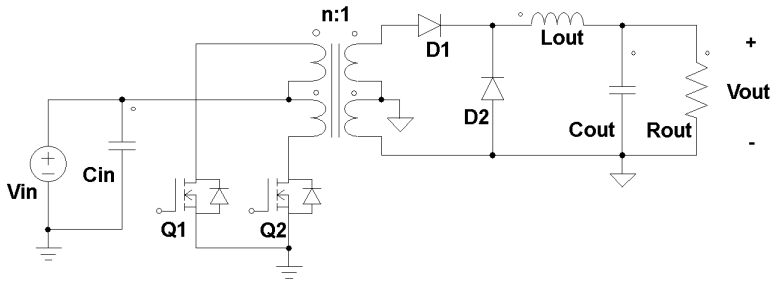


Figure 1.4. Push-Pull Converter Circuit.

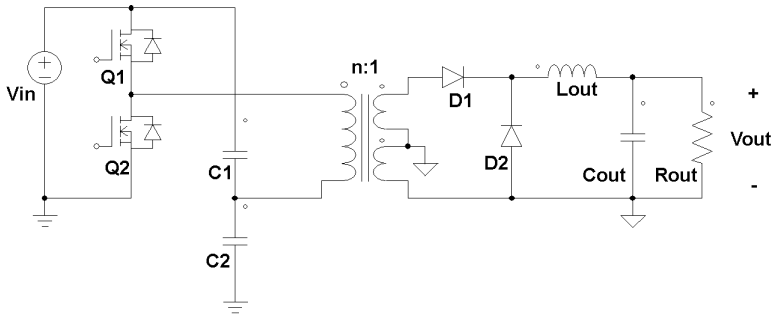


Figure 1.5 Half-Bridge Converter Circuit.

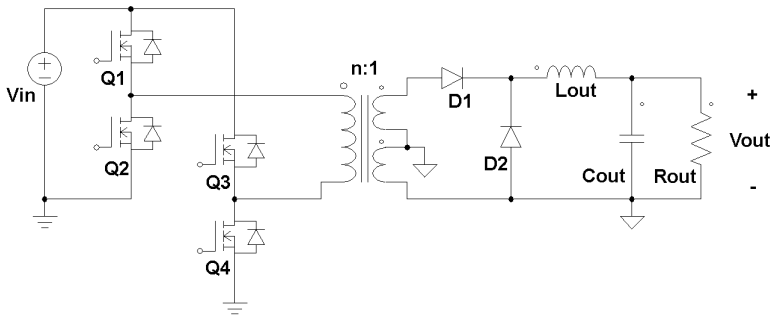


Figure 1.6 Full-Bridge Converter Circuit.

Comments

Several aspects have to be considered when comparing isolated power supplies topologies for a certain application. The most popular rules of thumb are based simply on the output power rating to switch from one topology to another, from flyback to full-bridge. More opportunely, the evaluation of a certain topology must take into account that:

- for a given power output rating, it makes a big difference to work with higher current and lower voltage or with lower current and higher voltage, as the voltage and current ratings greatly influence the stresses and losses (and then the size and cost) of transformer and silicon devices;
- the way the transformer is reset and the number of windings has a big impact on transformer size and current rating capability;
- for any given topology, there can be different variants (e.g. diode rectification vs synchronous rectification, hard-switching vs soft-switching, low-side vs high-side active clamp reset, etc., different combination of duty-cycle and transformer turns ratio, continuous conduction mode vs discontinuous conduction mode, self gate driving vs independent gate driving);
- a transformer can be designed in many different ways (magnetic core shape and material, windings allocation and interleaving, gapping, planar *vs* wounded, etc), thus determining much different effects on size, losses and ringing;
- core temperature rise must be properly limited to avoid material operation in conditions of unpredictable temperature and losses levels;
- in power distribution architectures used in applications such as telecom, several multi-stage combinations of isolated and non-isolated, regulated and unregulated, topologies can be adopted, with different bus voltage levels, enabling the achievement of better stresses distribution among the power devices and higher-efficiency with respect to single-stage architectures.

As a result, a model allowing to include all these elements and to determine a reasonably reliable estimation of the transformer operation, starting from physically realizable core and windings arrangement, is needed to correctly decide whether, for any given specifications set, a certain topology is suitable or not.

Next Chapter discusses the fundamental issues of transformers design, focusing on the key point regarding the selection of the most appropriate magnetic core which allows to minimize the transformer size.

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Chapter 2

Transformer Design for Isolated Converters

Transformer design is the central issue in isolated switching power supplies design. The great interest for this topic is witnessed by the huge literature. Mostly discussed issues are: losses calculation and reduction [1]-[3], thermal modeling [4], benefits of planar *vs* conventional transformers [5]-[7]. References [8]-[10] can be assume for a quite complete survey about general modeling, design and optimization issues.

2.1 Introduction

Even though many commercial transformers are available today, many special situations occur such that the design of a custom transformer is required. Several types of non-standard multi-output dc-dc switching power supplies are used, for example, in aerospace applications, where many unconventional dc regulated outputs must be fed by a single dc input rail. Low profile, high efficiency, thermal stability, reliability specifications and high-power density requirements increase the transformer design complexity. Many design solutions can be allowed using different possible conversion topologies and considering the wide variety of magnetic cores available today and designers have often to fix whether feasible design is allowed or not by given set of design specifications. Providing a sound design solution is challenging and requires effective handling capability of several issues:

- data of magnetic cores provided by manufacturers;
- electromagnetic and thermal models of magnetic cores;
- overall design equations of transformers;
- numerical techniques to solve the design equations;

- make a search of a good physically realizable candidate in the space of design solutions;
- matching analytical results with restrictions imposed by the available core sizes, by the integer windings turn numbers and by the physical properties of magnetic materials.

Figure 2.1 shows a typical transformer setup, where main measures are highlighted. The preliminary design steps consist in selecting a magnetic core and determining the turns number and bar area of each winding, such that:

- the ratios between secondary and primary winding voltages are as close as possible to the desired ones;
- the magnetic core does not saturate;
- the total core and copper losses do not exceed the allowed loss budget;
- the core temperature is limited to avoid thermal runaway and to make core loss predictable;
- skin and proximity effects into windings are prevented.

Other design issues, like isolation, multi-layer arrangement and consequent estimation of high-frequency losses increase, leakage inductances, interleaving, shielding, have also to be faced in different ways depending on the voltage levels. All these elements are heavily conditioned by the selected core.

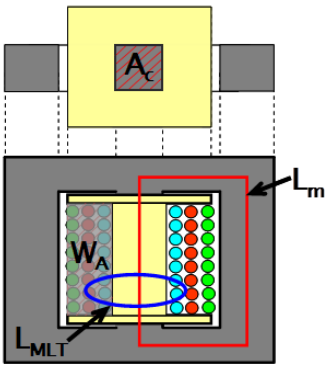


Figure 2.1 Basic transformer setup.

The primary winding turns number n_0 and the secondary windings turns numbers n_1,.., n_m must fulfill the conditions (1):

$$\frac{n_j}{n_0} = \frac{V_{oj}}{M(D)V_i}, \quad j = 1,..,m \tag{1.a}$$

$$n_0 = \frac{\lambda_T}{2A_c B_{ac}}, \quad \lambda_T = \int_0^{DT_s} V_T dt \tag{1.b}$$

where $M(D)$ is the conversion ratio of the converter, λ_T is the transformer primary magnetic flux, V_T is the voltage across the magnetizing inductance, V_i and V_{oj} are the input voltage and the j-th output voltage of the power supply. The selection of core and windings is heavily conditioned by the duty-cycle D and the switching frequency f_s. Higher switching frequency f_s allows reducing the size of passive components. The duty-cycle D may greatly affect the power supply efficiency and cost: it jointly influences the losses and stresses of both semiconductor and passive power components. Therefore, a global design optimization of isolated switching power supplies should necessarily involve the consideration of the joined global effects of f_s and D. Some guidelines regarding the duty-cycle D can be adopted to avoid useless exploration of design solutions which are not convenient. A first one is the use of Utilization Factor [11] to identify the range of values of D such that the overall stress on silicon devices is kept at minimum level, thus allowing the use of devices with smaller die. Other elements to be accounted for are:

- the minimum and maximum on-time and off-time imposed by the switcher IC adopted to control the isolated converter;
- the effect of the PWM current waveforms on the high-frequency windings loss increase effect [12]-[17];
- the width of input voltage range.

All these elements together often bring to the choice reference values for the duty-cycle D around D=0.5. Nevertheless, the discussion presented in this Chapter shows that there can be reasons connected to the minimization of transformer core size suggesting to fix the duty-cycle D at different reference levels.

Affording a preliminary investigation of possible feasible transformer designs can be of great help in reducing the *time-to-test* of transformers prototypes and final design. The easiest practical method for transformer design is based on the concept of Area Product (A_p) [18]-[20]. Such method is founded on a basic and intuitive concept: the size of the magnetic core increases with the power to be handled by the transformer and decreases with allowed losses.

The method based on the concept of geometric constant K_{gfe} of the magnetic core [11] is an extension of the A_p method. It is aimed at achieving the transformer design by searching the conditions allowing to minimize the total losses and the size of the device. However, both A_p and the K_{gfe} method has some intrinsic limitations and hide some underhand misconceptions which do not guarantee to realize a straightforward and reliable achievement of these goals in any condition.

The foundations of the novel method discussed in this section derive from a critical re-examination of the A_p and K_{gfe} methods, which are very popular both in technical literature and in many application notes widespread by devices manufactures. The novel approach to transformer design presented and discussed in the following section, based on two Geometric Form Factors (GFFs) of magnetic cores, is aimed at overcoming such limitations. The new method can be applied to any global power supply design and helps in easily identifying possible transformer solutions in critical custom designs complying with given losses and size constraints. Some examples will be finally discussed, referring to the transformer design for forward converters, using both wounded and planar transformers, respectively for multi and single output case.

2.2 Design methods for magnetic devices

In this section the A_p and K_{gfe} methods are discussed.

2.2.1 The A_p Design Method

The A_p design method was firstly introduced by Colonel Wm. T. McLyman[1] and it is still now widely used for designing inductors and transformers for dc-dc power converters. The A_p approach aims to select the size core for a magnetic device with a given operating frequency and output power.

The power handling capability of a magnetic core can be determined by the product of the core cross section area A_c and its window area W_A. The relationship between the product A_cW_A and the power output of the magnetic device can be derived starting from the Faraday's law. In particular, the required cross section area A_c of the core can be obtained as in (2):

$$V_{in,rms} = \chi_f f_s N \Delta B_{ac} A_c \tag{2}$$

where $V_{in,rms}$ is the applied voltage, χ_f is the waveform factor ($\chi_f = 4.44$ for a sinusoidal waveform and $\chi_f = 4$ for a square waveform), N is the number of turns and ΔB_{ac} is the maximum magnitude of the ac component of magnetic flux density. Solving (2) for the product ($N \cdot A_c$), yields equation (3):

$$NA_c = \frac{V_{in,rms}}{\chi_f f_s \Delta B_{ac}} \tag{3}$$

[1] Colonel Wm. T. McLyman has fifty seven years of experience in the field of Magnetics, and holds fourteen United States Patents on Magnetics-related concepts. He is the author of four popular textbooks: "Magnetic Core Selection for Transformers and Inductors", "Designing Magnetic Components for High-Frequency DC-DC Converters", "High Reliability Magnetic Devices: Design and Fabrication", "Transformer and Inductor Design Handbook". He is known as a recognized authority in Magnetic design. He is the President of his company called Kg Magnetics, Inc., which specializes in power magnetic design, which was formed and incorporated in 1985.

The window utilization factor K_u, which depends on the wire type, wire size, insulation requirements and winding technique, is defined in (4).

$$K_u = \frac{NA_w}{W_A} \tag{4}$$

where A_w is the wire bar area. Solving (4) for N and multiplying for A_c, yields equation (5):

$$NA_c = \frac{K_u W_A A_c}{A_w} \tag{5}$$

Thus, combining (3) and (5) and solving by $W_A A_c$, leads to:

$$W_A A_c = \frac{A_w V_{in,rms}}{\chi_f K_u f_s \Delta B_{ac}} \tag{6}$$

Finally, let us introduce the following quantities:

$$C = \frac{A_w}{I_{in,rms}} \tag{7}$$

$$\eta_T = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{V_{in,rms} I_{in,rms}} \tag{8}$$

where C [m^2/A] is the current density into conductors and η_T is the transformer efficiency. From (7) and (8), the relation (6) can be re-written as follow:

$$W_A A_c = k \frac{P_{out}}{f_s \Delta B_{ac}} \tag{9}$$

where

$$k = \frac{C}{\eta_T \chi_f K_u} \tag{10}$$

According to the A_p concept, since the window area is orthogonal to the core cross section area, the volume and weight of a transformer are uniquely determined once the area product is known [19][20]. However, as it can be seen from the previous relations, there are many variables involved in the evaluation of an appropriate size of magnetic cores. Thus, the power handling of the core does not grow simply in a

linear way according to the product $W_A A_c$, or with his volume. A larger transformer can work with lower power density, if the heat dissipated through its surface area grows less than the heat produced within the volume of the core. In fact, the A_p method does not consider any thermal issues for the magnetic devices design. Moreover, if we look at the different instances of (9) referred to the different isolated topologies, we get different formulas [21][22], like (11):

$$W_A A_c = \frac{J_{\max}}{k_T} \frac{P_{out}}{f_s \Delta B_{ac}} \tag{11}$$

where J_{max} [m^2/A] is the maximum current density, k_T is a topology constant (given for primary area allocation factor α_p=0.4), which corresponds to:

- 0.00033 for single-output flyback converter;
- 0.00025 for multiple-output flyback converter;
- 0.00050 for forward converter;
- 0.001 for push-pull converter;
- 0.0014 for half-bridge converter;
- 0.0014 for full bridge converter.

For specific topologies, like flyback converter, different versions of the A_p formula are suggested in literature. For saturation conditioned design, (12) is given:

$$W_A A_c = \left[\frac{L_m I_{Lmk} I_{p,rms}}{k_1 B_{pk}} \right]^{\frac{4}{3}} \tag{12}$$

while, for loss conditioned design, (13) is given:

$$W_A A_c > \left[\frac{L_m \Delta I_{pp} I_{p,rms}}{k_2 \Delta B_{pp}} \right]^{\frac{4}{3}} \tag{13}$$

where $I_{p,rms}$ is the *rms* primary current, B_{pk} is the peak flux density, ΔI_{pp} is the peak-to-peak primary current, ΔB_{pp} is the peak-to-peak flux density, k_1=k_2=10^{-4}(J_{max} k_{pri}) and k_{pri} (primary copper area/window area) = 0.2. Both the coefficients k_T, k_1, k_2, and the primary winding area allocation factor α_p have standardized values, which are based on heuristic assumptions, often not explained in the literature [21][22].

As a consequence, the transformers designed by using the A_p design formulas might be as well as badly performing, depending on the operating conditions, which are completely hidden in the design equations.

2.2.2 The K_{gfe} Design Method

The core and windings losses P_{Fe} and P_{Cu} are given by expressions (14) and (15):

$$P_{Fe} = A_c L_m K_{fe} B_{ac}^{\beta} = A_c L_m \left(a f_s^{c} \right) B_{ac}^{\beta} \tag{14}$$

$$P_{Cu} = \frac{\rho L_{MLT}}{K_u W_A} n_0^2 I_{tot}^2 \tag{15}$$

where the coefficients a and c depend on the material and the switching frequency f_s. The equivalent current I_{tot} assumes different formal expressions, depending on transformer type, whether wounded or planar. In wounded transformers, an optimal allocation of the net window area W_{Au} can be achieved, so that the total copper loss P_{Cu} is minimized. According to [11], the cross-sectional area of the wire A_{wj} of each winding should be selected as proportional to its apparent power:

$$\alpha_j = \frac{n_j A_{wj}}{W_{Au}} = \frac{V_j I_{jrms}}{\sum_{j=0}^{M} V_j I_{jrms}} = \frac{n_j I_{jrms}}{\sum_{j=0}^{M} n_j I_{jrms}} \tag{16}$$

so that:

$$I_{tot} = \sum_{j=0}^{M} \frac{n_j}{n_0} I_{jrms} \tag{17}$$

In planar transformers the windings are usually flat copper traces, either stamps or Printed Circuit Boards (PCB). Because of the industry standards for core sizes and geometries, pre-designed windings are used to fit the shapes of the cores. Thereafter, also cross-sectional areas of each windings turn are quite all pre-fixed, according to low height of window areas and required insulation layer between turns. In this regard, a practical design problem lies in ensuring that the cross sections are large enough to conduct full load currents.

Therefore, the fraction α_j of the net window area W_{Au} allocated to the j-th winding is pre-determined based on the maximum current density accepted for windings. As a consequence:

$$I_{tot} = \sqrt{\sum_{j=0}^{M} \left(\frac{n_j}{n_0} \right)^2 \frac{I_{jrms}^2}{\alpha_j}} \tag{18}$$

where α_j are given. Hereinafter, for whatever transformer practical realization, the relevant expression of I_{tot} is implicitly considered, with no loss of generality.

Given a magnetic core, in [11] it is shown that the ac component of flux density B_{ac} ensuring minimum total losses in the transformer, obtained by solving the equality $\partial P_{Fe}/\partial B_{ac} = - \partial P_{Cu}/\partial B_{ac}$, is given by (19):

$$B_{ac,opt} = \left[\frac{\rho \lambda_T^2 I_{tot}^2}{2K_u} \frac{L_{MLT}}{W_A A_c^3 L_m} \frac{1}{\beta K_{fe}} \right]^{\frac{1}{\beta'}} \tag{19}$$

where $\beta' = \beta + 2$.

In the hypothesis that $B_{ac} = B_{ac,opt}$, the following formula (20) provides the total transformer losses $P_{tot} = P_{Fe} + P_{Cu}$:

$$P_{tot,opt} = \Gamma_\beta \left[\left(A_c L_m K_{fe} \right)^2 \left(\frac{\rho \lambda_T^2 I_{tot}^2}{4K_u} \frac{L_{MLT}}{W_A A_c^2} \right)^\beta \right]^{\frac{1}{\beta'}} \tag{20}$$

where

$$\Gamma_\beta = \left(\frac{\beta}{2} \right)^{-\frac{\beta}{\beta'}} + \left(\frac{\beta}{2} \right)^{\frac{2}{\beta'}} \tag{21}$$

The way formulas (19) and (20) should be interpreted is:

- given a core characterized by a certain set of values of parameters W_A, A_C, L_m, L_{MLT}, K_{fe} and β,
- given the values of parameters D, f_s, λ_T and I_{tot} coming from power supply specifications,
- given the value of the utilization factor K_u,

if the operating conditions are such that the ac component of flux density B_{ac} equals exactly the value given by (19), ***then*** the transformer realized by means of that core will dissipate its minimum

power, given by (20). Reference [11] shows that the geometric constant K_{gfe} given by (22) can be defined for any magnetic core:

$$K_{gfe} = \frac{1}{\Gamma_{\beta}^{\beta'/\beta}} \frac{W_A}{L_{MLT}} \left[\frac{A_c^{2(\beta-1)}}{L_m^2} \right]^{1/\beta} \tag{22}$$

Accordingly, the formula (20) can be rewritten as in (23):

$$P_{tot,opt} = \left[\frac{K_{fe}^{2/\beta}}{K_{gfe}} \left(\frac{\rho \lambda_T^2 I_{tot}^2}{4K_u} \right) \right]^{\beta/\beta'} \tag{23}$$

whose meaning is: ***if*** the condition (22) is fulfilled, ***then*** the higher the geometric constant K_{gfe} the lower the value of minimum transformer loss in the given operating conditions. Based on (22)(23), given the maximum allowed total transformer losses $P_{tot,max}$, if one wants that such loss equal the minimum total power losses of the transformer realized by means of the selected core, the equality (24) is expected to be fulfilled:

$$K_{gfe} \le \left(\frac{\rho \lambda_T^2 I_{tot}^2}{4K_u} \right) \left(\frac{K_{fe}^2}{P_{tot,\max}^{\beta'}} \right)^{1/\beta} = K_{gfe,ref} \tag{24}$$

whose meaning is: ***if*** there is a core whose parameters fulfill equality (24) ***then*** the transformer realized by means of that core will dissipate the power $P_{tot,max}$. Equality (24) cannot be exactly fulfilled, because the core parameters values are discretized and the windings turns numbers are integers. From (23) it is expected that a core fulfilling inequality (25):

$$K_{gfe} \ge K_{gfe,ref} \tag{25}$$

guarantees the transformer will have a power dissipation lower than the allowed $P_{tot,max}$. Inequality (25) is based on the assumption that a core with a bigger geometric constant K_{gfe} dissipates less power as bigger core volume is associated by default to bigger K_{gfe}. Then some overall loss reduction is expected to occur with cores having bigger K_{gfe}, because either the ac component of flux density B_{ac} decreases (bigger area A_c) or/and the windings bare areas increase (bigger area W_A).

The K_{gfe}-based transformer design flow to comply with loss budget $P_{tot,max}$ works as follows:

step #1 take the core having the smallest K_{gfe} fulfilling (25);
step #2 verify that $B_{ac,opt}$ does not cause core saturation;
step #3 calculate the winding turns numbers using (1) and assuming $B_{ac} = B_{ac,opt}$
step #4 round windings turns numbers;
step #5 verify that losses are lower than $P_{tot,max}$;
step #6 if the core saturates, or losses exceed $P_{tot,max}$, then take a core having bigger K_{gfe} and go back to step#2.

Several trials might be needed to exit the K_{gfe} based design flow, because inequality (25) is not a sufficient condition for transformer loss compliance. Indeed, two main limits affect the core search based on inequality (25). The first one comes from the windings turn numbers. The optimal value of $B_{ac,opt}$ given by (19) may require turns numbers of winding n_j are non integer and smaller than unity. Accordingly, all turn numbers must be rounded and scaled up or down in order that they all are integer and the smallest one is at least equal to unity. As a result, windings losses can increase and the total loss budget could be exceeded. In addition, the assumption underlying (25) is that we need to increase the core size in order to reduce the losses. This is not necessarily true. Transformer losses are conditioned by the entire core geometry, rather than just by its volume. A transformer might dissipate less power if it is realized using a smaller core but characterized by particular GFFs. Formula (23) shows an inverse relation between the transformer losses and the geometric constant K_{gfe}, but it neglects the physical feasibility of the winding turns numbers allowing to fix the operating conditions given by (19). The turns numbers resulting from (1.a) can be non integer, and even smaller than unity, for $B_{ac}=B_{ac,opt}$. In conclusion, inequality (25) is not even a necessary condition for $P_{tot} \leq P_{tot,max}$. This makes the K_{gfe} method unable to guarantee a straightforward and reliable core selection. Moreover, even though the objective of minimizing the total losses in the transformer might be shareable in principle, if the goal is to limit the transformer losses below the given budget $P_{tot,max}$, it is not important if that value is the minimum achievable with the selected core: rather, it is more important to pick up the smallest core, and the proper winding turn numbers, allowing to comply with the loss budget

$P_{tot,max}$. Putting together the windings physical feasibility constraint with the loss budget constraint can provide a true straightforward and reliable design criterion, as shown in next section.

2.3 The K_c and K_f Geometric Form Factors

The design method introduced in this section is aimed at the identification of possible transformer design solutions matching available magnetic cores, operating conditions and design constraints. The method is based on a new mathematical formulation of intuitive concepts underlying transformer design, not previously disclosed in the same formal mathematical way. This new formulation, beyond the interpretative benefit, provides the basis for a new design procedure ensuring faster and easier preliminary physical feasibility of the transformer design. Indeed, the goal is to achieve a straightforward and reliable design of the transformer, such that its total losses are smaller than the given budget $P_{tot,max}$ *and* the volume of its magnetic core V_{core} is minimized. As a further constraint, the numerical value of all the quantities involved in the description of the transformer must guarantee physical realization. In particular, all the turns numbers n_j, $j=0,..,M$, must be integer and bigger than unity.

Given any single/multi-output power supply, it is always possible to sort the output(s) for decreasing voltage. For example, given a step-down topology, it can be assumed that the M-th winding of the transformer is terminated on the minimum voltage output. Given n_M as integer number ≥ 1, the integer turns numbers n_j given by (26) will all be ≥ 1:

$$n_j = round\left(\frac{V_{oj}}{V_{oM}} n_M\right), \quad j = 1,..,M-1 \tag{26}$$

wherein the operator "*round*(x)" yields the integer number closest to the argument x. Accordingly, the number of turns of primary winding n_0 is given by (27):

$$n_0 = round\left(\frac{n_M V_i D}{V_{oM}}\right) \tag{27}$$

Putting the value n_0 given by (27) into (28) yields the resulting magnitude of the ac component B_{ac} of flux density:

$$B_{ac} = \frac{\lambda_T}{2A_c n_0} \tag{28}$$

Merging (14),(15),(27) and (28) allows to explicit the constraint on total losses of the transformer as shown in (29):

$$P_{tot} = K_f \Gamma_f n_M^{-\beta} + K_c \Gamma_c n_M^2 \le P_{tot,\max} \tag{29}$$

where

$$K_f = \frac{L_m}{A_c^{\beta-1}} \ , \ K_c = \frac{L_{MLT}}{W_A} \tag{30}$$

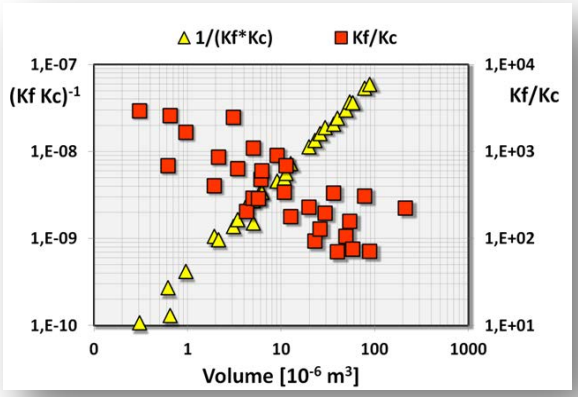
$$\Gamma_f = K_{fe}\left[\frac{V_{oM}}{2f_s}\right]^{\beta} , \Gamma_c = \frac{\rho}{K_u}\left[\frac{V_T DI_{tot}}{V_{oM}}\right]^2 \tag{31}$$

K_f and K_c are characteristic Geometric Form Factors of each magnetic core, whereas Γ_f and Γ_c are determined by the magnetic core material (β and K_{fe}), the application operating parameters (V_{oj}, I_{oj}, $j=0,..,M$, D, λ_T) and the utilization factor K_u. For any given set of values {f_s, D, β, K_u}, the selected turns number n_M determines whether a core allows or not the design of a transformer complying with loss budget constraint (29). Given n_M, a magnetic core will allow the realization of the transformer complying with (29) provided that its GFFs K_f and K_c satisfy the inequality (32), obtained from (29):

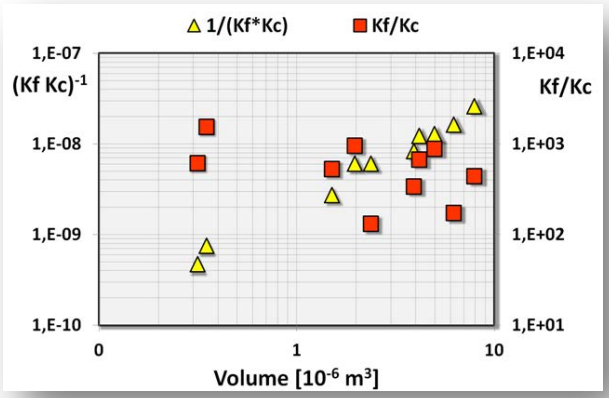
$$K_f \le K_{f,\max}(n_M, K_c) = \frac{P_{tot,\max} n_M^{\beta} - \Gamma_c n_M^{\beta'} K_c}{\Gamma_f} \tag{32}$$

The two GFFs K_f and K_c provide useful insight into the core characteristics. The product $K_f K_c$ is inversely proportional to the volume of the core, while the ratio K_f/K_c is a measure of the "*stockiness*" (large A_c area and/or small W_A area) of the core. Figure 2.2 show the plots of $1/(K_f K_c)$ and K_f/K_c *vs* the volume, respectively for a set of F material MAGNETICs EE cores (a) [23] and 3C94 material FERROXCUBE EE/EI planar cores (b) [24]. Each core is identified by a couple of vertically aligned square and triangle

markers. In Figures 2.2(a)(b), bigger cores correspond to markers located towards the bottom-left corner of the plot area while stockier cores correspond to markers located towards the bottom-right corner of the plot area. The plot shows that cores having quite different form factor K_f/K_c may have the same volume, while cores having quite different volume may have the same form factor K_f/K_c. Given a certain value of the K_fK_c product, a core with higher K_f and lower K_c may involve higher core losses and lower copper losses than a core having the same K_fK_c product (same volume) with lower K_f and higher K_c.



(a)



(b)

Figure 2.2 Geometric form factors of: (a) EE MAGNETICs cores, (b) EE/EI planar FERROXCUBE cores.

Given n_M, if the geometric constant K_f of a core is lower than the value $K_{f,max}$ given by (32), then the total losses of the transformer designed with that core will *certainly* be lower than $P_{tot,max}$. Therefore, minimizing the transformer size means to find the value of n_M allowing to make equation (32) fulfilled by the core having the biggest possible K_fK_c product. The minimum value of n_M, required to prevent core saturation is obtained by solving (33):

$$B_{dc} + B_{ac} = B_{dc} + \frac{\lambda_T V_{oM}}{2A_c n_M V_i D} < B_{sat} \tag{33}$$

which provides:

$$n_{M,\min sat} = round\left[\frac{\lambda_T V_{oM}}{2A_c V_i D\left(B_{sat} - B_{dc}\right)}\right] \tag{34}$$

The K_f-K_c-based transformer design flow works as follows:

step #1 take cores of the preferred manufacturer, material and shape;
step #2 calculate GFFs K_f and K_c;
step #3 calculate $K_{f,max}$ for each core, with $n_M \geq max\{1, n_{M,\min sat}\}$;
step #4 take the core having $K_f \leq K_{f,max}$ and maximum K_fK_c product.

Thus, no iterations and no verifications of physical reliability, loss budget compliance and core saturation are required. It should be noted that, although the previous design flow has been put in form of a sequence of steps, no code programming at all is required to apply the K_f-K_c-based method. All data, formulas and plots can be easily implemented using well known popular spreadsheets, as done for the dc-dc forward converter examples, illustrated in next paragraph.

2.4 Design Examples

A first example considered to illustrate the application of the K_f-K_c-based transformer design method is related to a dc-dc multi-output active-clamp forward converter with *48V* input voltage and seven outputs (case *a*), whose voltage and current specifications are given in Table I.

Table 2.1 Case *a*: Specifications for the Application Example

V_{out1}	V_{out2}	V_{out3}	V_{out4}	V_{out5}	V_{out6}	V_{out7}
10V	7V	5V	3,3V	10V	7V	5V
I_{out1}	I_{out2}	I_{out3}	I_{out4}	I_{out5}	I_{out6}	I_{out7}
6A	9A	9A	9A	3A	3A	9A

For such application, the following specifications have been assumed too: η=92%, f_s=*230kHz*, *D=0.42*, $P_{tot,max}$=*1280mW* (corresponding to 5% of the maximum power dissipation).

According to the multi-output topology, to the power converter handling and to the considered switching frequency, *F* material EE MAGNETICs cores have been taken into account, assuming K_u=*0.6* and β=*2.68*. The K_f-K_c-based transformer design flow has been described in previous section referring to the numerical computations it involves. Nevertheless, it should be noted that right side of inequality (32) describes a curve in the K_c-K_f plane parameterized by n_M. The graphic representation of this curve allows an effective synoptic comparative view of feasible design solutions realizable using a set of selected magnetic cores of interest. Indeed, Figure 2.3 shows a family of curves, each one associated to a value of n_M, for n_M=*2,..,4*. Each curve is classifiable as an *Acceptability Boundary Curve* (ABC). The concept of ABC has been recently introduced as a basis for methods of selection of power components for switching power supplies design [25]. That concept is now applied to transformer design. Square markers in Figure 2.3 label MAGNETICs EE cores. The cores whose markers are located below the ABC corresponding to a certain n_M, allow the design of a transformer complying with the assigned loss budget $P_{tot,max}$. Changing n_M modifies the set of cores allowing feasible design. When the turn number n_M increases, the right portion of the ABC folds downside while its left portion folds upside. The way the ABCs move through the K_c-K_f plane, while n_M goes from 2 to 4, highlights that there are different values of n_M enabling loss-compliant transformer design with different cores. For certain values of n_M it will be possible that some core having smaller volume (bigger K_fK_c product) allow the design of the transformer. Those values of n_M depend on the values of GFFs K_f and K_c of the family of cores analyzed.

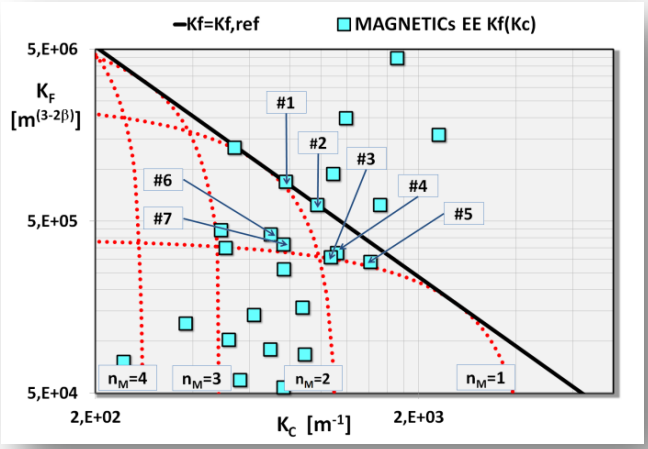


Figure 2.3 ABCs of magnetic cores for loss compliant transformer.

The envelop of the ABCs, represented by the continuous thick black line in Figure 2.3, is associated to the geometric constant K_{gfe}. In fact, merging (22) and (30) yields:

$$K_{gfe} = \left[\Gamma_{\beta}^{\beta'/\beta} K_c K_f^{2/\beta} \right]^{-1} \tag{35}$$

Putting (35) in (25) provides condition (36):

$$K_f \le K_{f,ref} = \left[K_c^{\beta} K_{gfe,ref}^{\beta} \Gamma_{\beta}^{\beta'} \right]^{-1/2} \tag{36}$$

Fulfilling (36) means fulfilling (25). The plot of right side of (36) is the mentioned envelop of the ABCs in Figure 2.3. The ABCs and their envelop allows a clear understanding of the misleading results that K_{gfe}-based design method can produce. For example, according to K_{gfe}-based design method, cores #3, #4 and #5 in Figure 2.3 should comply with maximum loss constraint. This is true only for some *non integer* value of n_M, namely $1<n_M<2$. As this solution is not physically realizable, that core is not suitable for the project. In fact, for both $n_M=1$ and $n_M=2$ the values of K_f of this core is bigger than $K_{f,max}$ given by (32): then, the transformer losses exceed $P_{tot,max}$. This example highlights that the K_{gfe}-based design method neglects the *unfeasibility*

niches in the K_f-K_c plane which correspond to the portions of plane bounded by the envelop (36) and the couples of ABCs corresponding to two successive integers values of n_M. The smallest cores ensuring loss-compliant transformer design with integer n_M are #6 and #7, both for $n_M = 2$.

Figure 2.4 shows the geometric constant K_{gfe} and minimum total transformer losses vs the volume for the cores #1 to #7. The plot highlights that:

- core #1 and core #2 have a too small K_{gfe} and total transformer losses exceed $P_{tot,max}$;
- core #3, #4 and #5 have $K_{gfe} > K_{gfe,ref}$, nevertheless the transformer losses exceed $P_{tot,max}$;
- core #6 and #7 have bigger K_{gfe} and quite larger volume and the resulting transformer losses are lower than $P_{tot,max}$;
- core #6 has lower K_{gfe} and larger volume than core #7, but its resulting transformer losses are lower.

Thus, it is not correct to assume that higher geometric constant K_{gfe} (or larger volume) correspond to lower total transformer power losses.
The second example (*case b*) considered to illustrate the application of the K_f-K_c-based transformer design method is related to a single-output dc-dc active-clamp forward converter with the following specifications: $V_{in}=48V$, $V_{out}=3.3V$, $I_{out}=15A$, η=92.5%, $f_s=230kHz$, $D=0.42$ and $P_{tot,max}=201mW$ (corresponding to 5% of the maximum power dissipation). According to the power converter handling and to the considered switching frequency, *3C94* material FERROXCUBE EE/EI planar cores have been taken into account ($K_u=0.15$ and $\beta=2.75$) and represented as square markers in Figure 2.5.

In Figure 2.5, core #2 complies with K_{gfe}-based design method maximum loss constraint. Nevertheless, the transformer losses exceed $P_{tot,max}$ because of the non integer value of n_M. The smallest cores ensuring loss-compliant transformer design with integer n_M are core #3, #4 and #5, respectively for $n_M = 2, 3$, for $n_M = 2$ and for $n_M = 1, 2$.

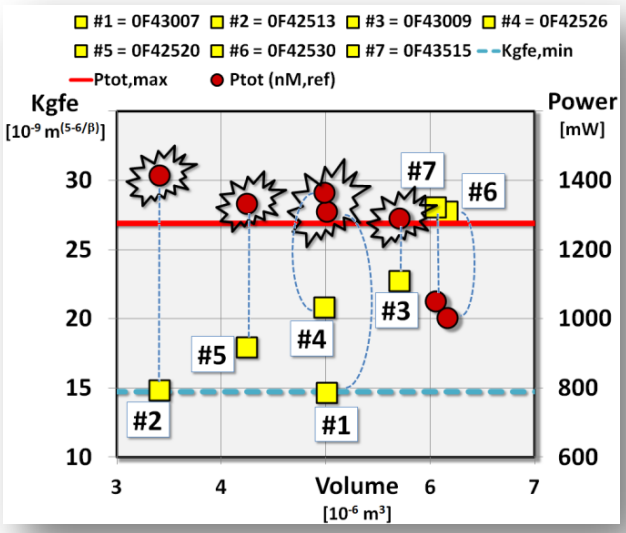


Figure 2.4 K_{gfe} and power losses vs core volume.

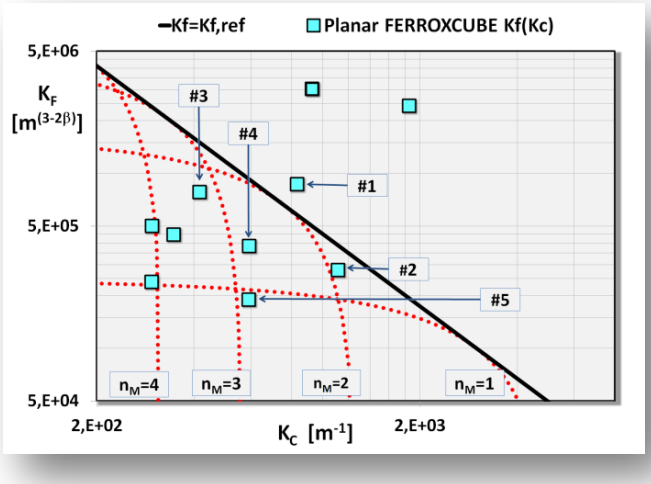


Figure 2.5 ABCs of magnetic cores for loss compliant transformer.

Figure 2.6 shows the values of total transformer losses vs the turn number n_M. Finally, Figure 2.7 shows the geometric constant K_{gfe} and minimum total transformer losses vs the volume for the cores #1 to #5. The plot highlights that:

- as expected, core #1 has a too small K_{gfe} and total transformer losses exceed $P_{tot,max}$;
- core #2 has $K_{gfe} > K_{gfe,ref}$, nevertheless the total transformer losses exceed $P_{tot,max}$;
- core #3, #4 and #5 have bigger K_{gfe} and quite larger volume and the resulting total transformer losses are lower than $P_{tot,max}$;
- core #5 has a very larger volume, three times the volume of core #3, nevertheless its resulting total transformer losses is only some tens *mW* lower than for core #3.

The use of the single geometric constant K_{gfe} yields misleading deductions as it hides the important role of core form factor on total transformer power losses correctly taken into account using the two GFFs K_f and K_c. The GFFs K_f and K_c also allows a quick identification of physically realizable transformers complying with a given total loss budget. Further insight in GFFs K_f and K_c theory and applications are provided in paragraph 2.4.1 and 2.4.2.

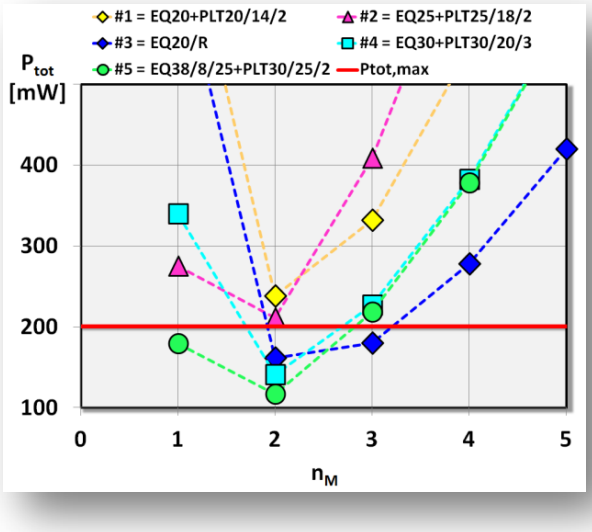


Figure 2.6 Total transformer power losses vs turns number n_M.

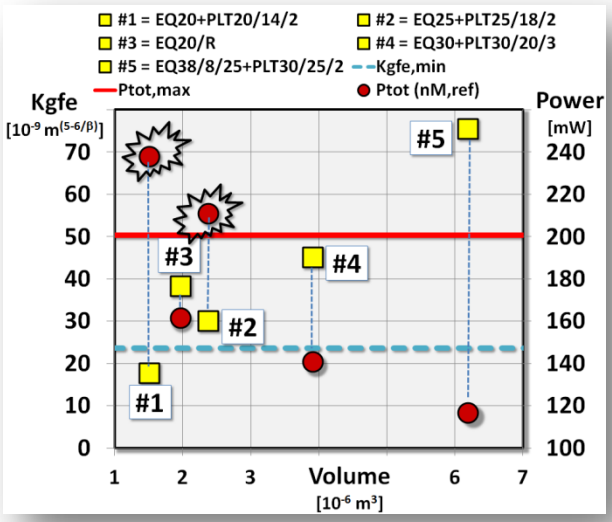


Figure 2.7 K_{gfe} and power losses vs core volume.

2.4.1 Thin cores *vs* Thick cores

Using n_M as parameter in K_f-K_c-based transformer design yields useful practical results and theoretical insight, like a mean for identifying the form properties of cores which help in making transformers physically realizable and an alternative formulation of the K_{gfe}-based design equation. The value of n_M ensuring the design of a transformer with minimum losses can be obtained by putting equal to zero the derivative of the total transformer loss with respect to n_M:

$$\partial P_{tot} / \partial n_M = 2\Gamma_c K_c n_M - \beta \Gamma_f K_f n_M^{-\beta-1} \tag{37}$$

from which:

$$n_{M,opt} = \left[\frac{\beta}{2} \frac{\Gamma_f}{\Gamma_c} \frac{K_f}{K_c} \right]^{1/\beta'} \tag{38}$$

Formula (38) highlights that stockier cores require lower n_M for minimizing the losses. As physical realization of the transformer requires that $n_{M,\text{opt}} \geq \max\{1, n_{M,\text{min}sat}\}$, (38) can be converted in (39):

$$\frac{K_f}{K_c} \geq \frac{2\Gamma_c}{\beta\Gamma_f}\left[\max\{1, n_{M,\min sat}\}\right]^{\beta'} \tag{39}$$

which allows to verify the possibility to design the transformer with minimum total losses achievable with a certain core. Condition (39) is highly instructive: it shows in a clear and quantitative way that for high-current/low-voltage applications (big Γ_c and small Γ_f) "*thin*" cores are required (big K_f and small K_c), whereas for low-current/high-voltage applications (big Γ_f and small Γ_c) "*stocky*" cores are required (big K_c and small K_f). This means that two transformers made with two different cores with the same volume ($1/K_fK_c$) and with different form factor (K_f/K_c) may dissipate much different power and, depending on the application, one can be better than the other, or vice versa, for the specific operating currents and voltages. Replacing (39) into (29) provides the minimum achievable losses of the transformer realized by means of a given core:

$$P_{tot}\left(n_{M,opt}\right) = \Gamma_\beta \left(\Gamma_c K_c\right)^{\beta/\beta'} \left(\Gamma_f K_f\right)^{2/\beta'} \tag{40}$$

For the realization of a transformer complying with loss budget and mimizing the losses at the same time it must be $P_{tot}(n_{M,opt}) \leq P_{tot,max}$. Thus, according to (40):

$$K_c^{\beta} K_f^{2} \leq P_{tot,\max}^{\beta'} \left[\Gamma_\beta^{\beta'} \left(\Gamma_c^{\beta} \Gamma_f^{2}\right)\right]^{-1} \tag{41}$$

It can be easily verified that (41) and (25) are the same equation. While in [11] the geometric constant K_{gfe} is obtained by searching the $B_{ac,opt}$ value, the derivation illustrated in this chapter is based on searching the optimal value of turn number $n_{M,opt}$. As both approaches are aimed at minimizing the transformer losses, and n_M and B_{ac} are related each other by (27) and (28), the $n_{M,opt}$ necessarily corresponds to $B_{ac,opt}$. Of course, $n_{M,opt}$ is likely expected to be non integer.

2.4.2 Duty-Cycle and Switching Frequency investigation

In previous analysis the total transformer losses P_{tot} have been calculated assuming given values of switching frequency f_s and duty-cycle D. These values are supposed to derive from silicon devices

selection, according to stress and loss analysis. As a consequence, some small cores are not acceptable as there is no integer value of n_M enabling loss compliant transformer design, like, for example, cores #2 in Figure 2.5. However, there can be values of duty-cycle D and/or of switching frequency f_s which might also be acceptable for silicon devices, in terms of stresses and losses, making those cores acceptable. Indeed, condition (29) can be rewritten as follows:

$$P_{tot} = K_f \Gamma'_f \; f_s^{c-\beta} n_M^{-\beta} + K_c \Gamma'_c \, D^2 n_M^2 \le P_{tot,\max} \tag{42}$$

where:

$$\Gamma'_f = a\left[\frac{V_{oM}}{2}\right]^{\beta}, \; \Gamma'_c = \frac{\rho}{K_u}\left[\frac{V_T I_{tot}}{V_{oM}}\right]^2 \tag{43}$$

Let $n_{M,ref}$ be the turns number according to which the transformer realization complies with the assumed loss budget. Then, assuming $P_{tot}(n_{M,ref})=P_{tot,max}$ yields the following equations:

$$D = \left(\frac{P_{tot,\max} - K_f \Gamma'_f \; f_s^{c-\beta} n_{M,ref}^{-\beta}}{K_c \Gamma'_c \, n_{M,ref}^2}\right)^{1/2} \tag{44}$$

$$f_s = \left(\frac{P_{tot,\max} - K_c \Gamma'_c \, D^2 n_{M,ref}^2}{K_f \Gamma'_f \, n_{M,ref}^{-\beta}}\right)^{1/(c-\beta)} \tag{45}$$

Applying (44)(45) to cores #1 to #5 of Figure 2.5, yields the results resumed in Table 2.2. For core #2, a slight change of the duty-cycle or of the switching frequency is sufficient to make it acceptable: both these different operating conditions can be adopted without a big impact on stresses and losses of silicon devices. Also smaller volume core #1 can be adopted by accepting a 15% reduction of the duty-cycle at the same switching frequency. Using the concept of ABCs descending from (34) and based on the two GFFs (35) allows several useful insight in feasible design solutions of transformers for high-frequency isolated power converters.

Table 2.2 Duty-Cycle and Switching Frequency Obtained with (44) and (45)

	CORE Part Code	$n_{M,rif}$	P_{tot} [mW]	D (@ fs=230kHz)	P_{tot} [mW]	f_s [kHz] (@ D=0.42)	P_{tot} [mW]
#1 = EQ20+PLT20/14/2	C_42014EC	2	238	0,36	201	322	201
#2 = EQ25+PLT25/18/2	0_42313EC	2	211	0,41	201	304	201
#3 = EQ20/R	0_42517EC	2	162	0,53	201	176	201
#4 = EQ30+PLT30/20/3	0_42521EC	2	141	0,54	201	122	201
#5 = EQ38/8/25+PLT30/25/2	0_43021EC	2	117	0,58	201	70	201

2.5 Experimental Verifications

The experimental measurements of the total high-frequency high-efficiency transformer losses in real power supplies operating conditions is still now a difficult task. For applications like those ones previously discussed, it is quite complex to evaluate losses with an accuracy ensuring meaningful results. In this sense, the main difficulties encountered are due to *on-line* acquisitions of transformer input and output current waveforms at the given switching frequency (usually, hundreds of *kHz*), switching times (tens of *ns*), losses rate (actually, transformer efficiency is estimated around *99.5%*), current rates (tens of Amps) and current slew-rates (up to some *Amps/ns*) of the application. Experimental set-up for off-line transformer losses measurements [26][27] has been discussed in literature. Unfortunately, they involve main difficulties in reproducing realistic on-line operating conditions with the same relevant critical rates and with the same layout conditions.

Thus, some on-line techniques for transformer losses measurement have been considered. Experimental activities have been realized by using the National Semiconductor Evaluation Boards (NSC EBs) of Active Clamp based Forward converter with different controllers:

- LM5025 Active Clamp PWM controller [28];
- LM5026 Active Clamp PWM controller [29].

These NSC EBs refer to a single output Forward converter with planar transformer and both permit to implement Forward converter design corresponding to *case b* previously discussed has been implemented with these boards. For the experimental verifications the following

specifications have been adopted: V_{in}*=48V,* V_{out}*=3.3V,* I_{out}*=15A÷25A,* f_s*=230kHz.*

The measurements have been quite difficult for this case study, because of troubling currents sensing both for primary and secondary side at high switching frequency, 1÷2A/ns slew rate, 15Amps rate and very high nominal transformer efficiency (around 99.5%). Bandwidth and very small available space on the boards are limiting factors for other sensing techniques based on transformers and Hall effect sensors. Thus, several anti-inductive sensing resistances based techniques have been considered and experimented in order to obtain a reliable current sensing both at primary and secondary side of the transformer. Such techniques represent a quite conventional way of current sensing. Sense resistors have been inserted in series with the primary and the secondary side of the transformer available on the board: in theory, if the value of the resistor R_{sense} is known, the current flowing through the input and output port of the magnetic devices is determined by sensing the voltage across R_{sense}. This method obviously produces a power loss in R_{sense}, and therefore reduces the efficiency of the converter. Nevertheless, the main target of this experimental investigation aims at obtaining transformer losses measurement, by sensing current and voltage at the two port of the magnetic device.

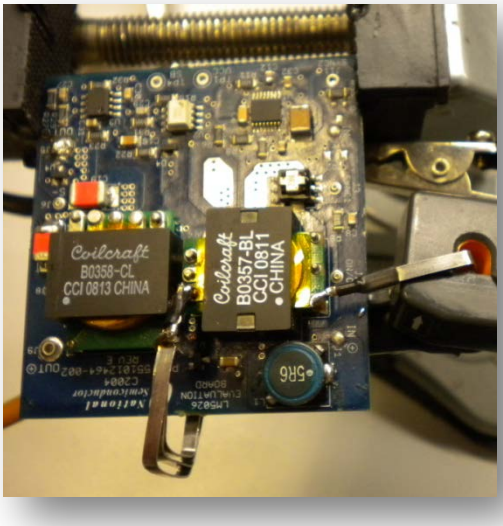
The Bourns PWR4412-2S Series resistors [30] with bare metal resistive element (see Figure 2.8(a)) have been used for the current waveforms acquisitions. These resistors have high current capability and low nominal inductance: nevertheless, the inductive effects produced by the resistances insertion cause anyway current waveforms delays with respect to the voltage waveform acquisitions, as shown in Figure 2.8(b).

The Ohmite CS3 Series resistors [31] with four terminal precision current sense resistance have been adopted too: they also have non-inductive nominal design and permit to achieve highly reliable non-inductive performance (see Figure 2.9(a)). However, the too low resistance value (CS3 Series resistances range goes from 1mOhm to *50mΩ*) and the still too high inductance values (some tens of *nH*) of these sensing elements do not permit to obtain a proper current waveforms acquisition, as shown in Figure 2.9(b).

Thus, different current-sensing techniques have been investigated. In order to minimize the inductive effects introduced through the insertion of sensing elements, the channel resistances of SMD MOSFETs biased in the ohmic region have been adopted: drain and source parasitic inductances of SMD MOSFETs are usually estimated in some tens of *pH* (thus, almost three order of magnitude lower than the non inductive declared commercial resistors). Consequently, the current sensing is determined by sensing the voltage across the drain-source of the MOSFET, provided that the drain-to-source resistance R_{ds} of the MOSFET is known. As the R_{ds} of the MOSFET is inherently nonlinear and has significant variations, because it varies with temperature, this measurement technique requires a preliminary calibration of the sensing MOSFETs gate-to-source voltage in order to detect the sensing constant through the passage of a known current through the MOSFET. If the calibration is well executed, this method can be used in many real contexts, because of the low influence of very small MOSFETs parasitic inductances.

As shown in Figure 2.10, two SO8 MOSFETs have been introduced on the LM5025 NSC EB, for sensing current at the primary and at the secondary side of the transformer. A proper MOSFET has been chosen and introduced in series at the primary side of the transformer, according to voltage and current stress it is required to support: VISHAY Si4982DY [32] is a TrenchFET Power MOSFET suitable for the reference application (V_{ds}=100V, $I_{ds,max}$=2.6A, $R_{ds,on}$=180mΩ).

In Figure 2.11(a)(b) the oscilloscope screenshots of voltage at the transformer primary side (blue curve) and voltage across Si4982DY drain-to-source resistance (red curve) have been shown for I_{out}*=10A* and I_{out}*=5A*, respectively. The waveforms shown in Fig.2.11(a)(b) are very encouraging, as they are lag-free, and tremendously much clean than waveforms obtainable with any other on-line measurement technique using sensing devices which can be used in the application under study.



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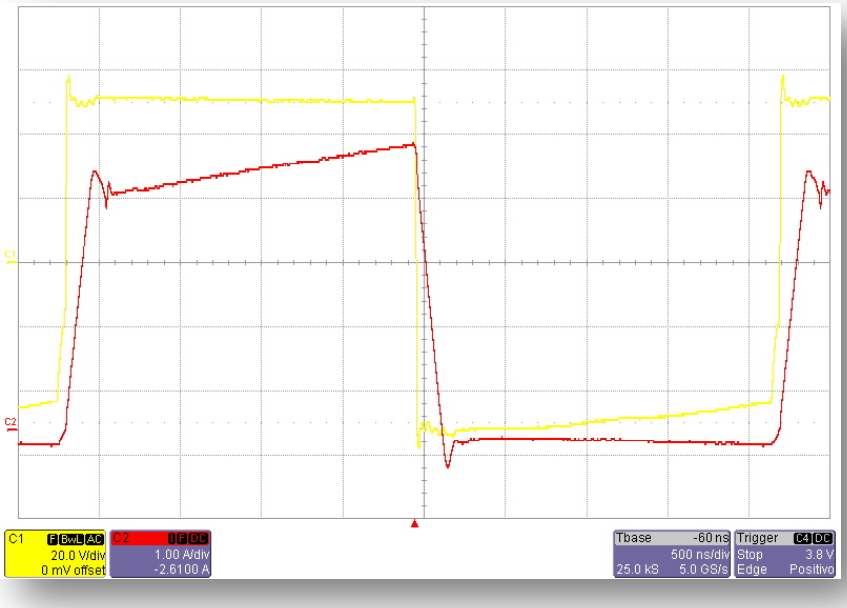
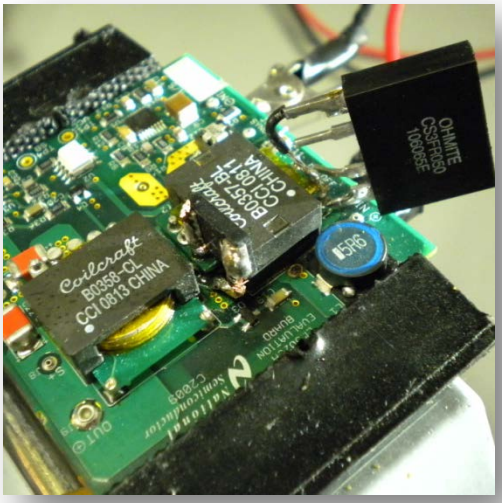


(b)

. 2.8 (a) Active Clamp Forward and PWR4412-2S series resistors; (b) transformer primary voltage (yellow) and current (red) waveforms.



(a)

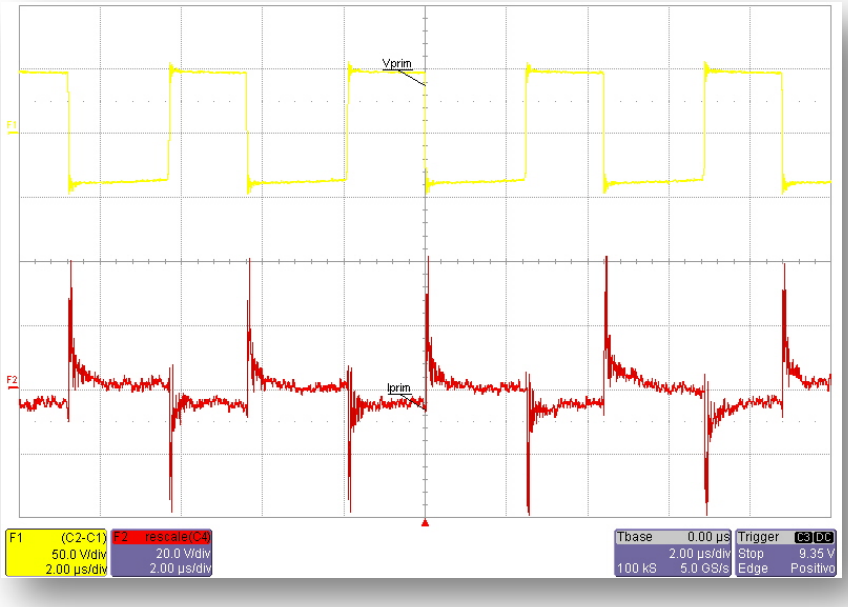


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Figure 2.9 (a) Active Clamp Forward and CS3 Series resistors; (b) transformer primary voltage (yellow) and current (red) waveforms.

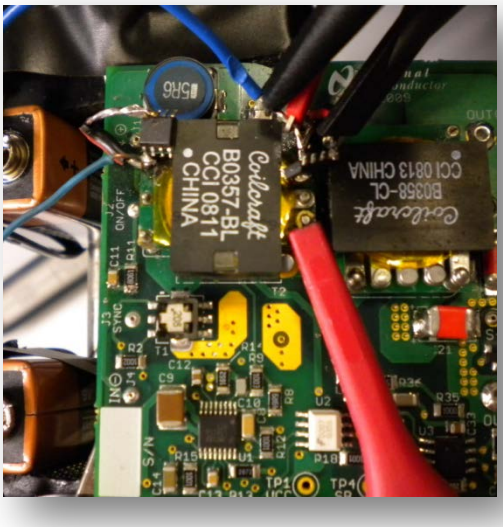
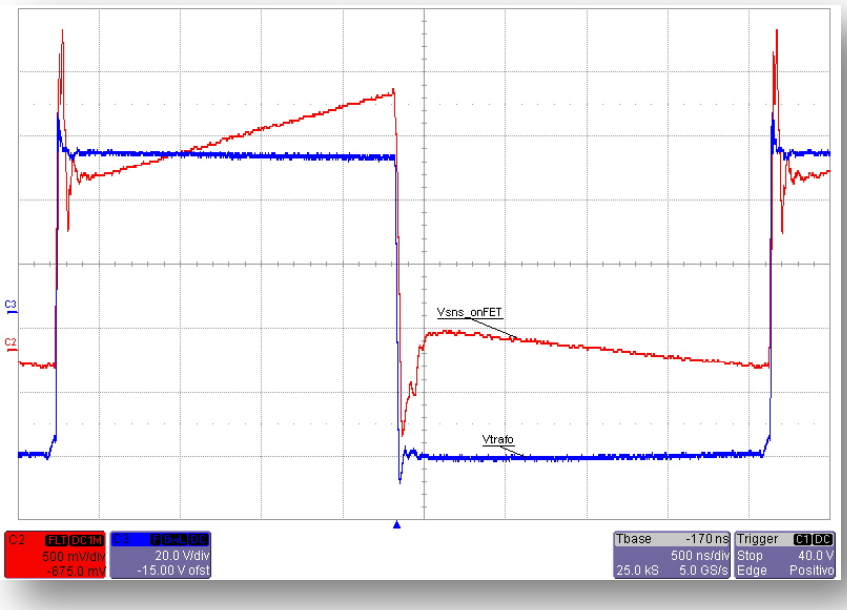


Figure 2.10 Active Clamp Forward and SO8 MOSFETs sensing resistors.



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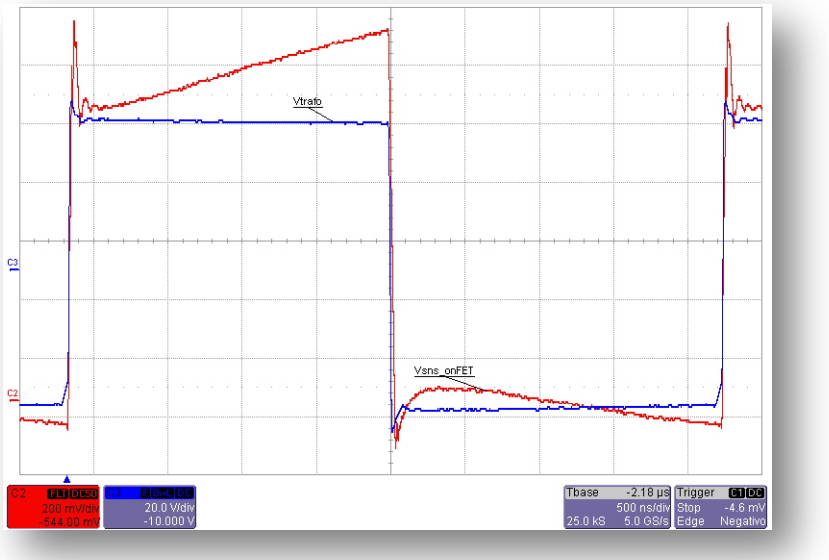

(b)

Figure 2.11 Transformer primary voltage (blue) and current (red) waveforms by using SO8 MOSFETs sensing resistors: for I_{out}=10A (a) and I_{out} =5A (b).

Although the development of the on-line measurement technique based on the use of MOSFETs as sensing resistors goes beyond the goals of this dissertation, at the moment of this writing it is still in progress. Indeed, some magnetic devices and silicon devices manufacturing companies have expressed interest for this approach.

Thus, further studies will be carried out also in the framework of future research collaborations with these companies to achieve the full operation of such online measurement technique.

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Chapter 3

Temperature Effects on Transformers Design Constraints

The new design approach suggested in Chapter 2 is aimed at the quick identification of combinations of cores and windings ensuring compliance with maximum loss budget and minimum core size constraints. Such analysis must also be done by properly considering possible thermal runaway of core [1]. Therefore, a suitable *Magneto-Electro-Thermal* (MET) model of the transformer is required, to be solved via numerical computation.

In this chapter a complete thermal model of the transformer is presented, which can be used to investigate the dependency of total transformer losses and consequent design constraints on the temperature. The proposed model considers the K_F-K_C design approach as basis for the identification of the design boundary curves and is based on the numerical solution of non-linear MET equations of transformer, with the addition of constraint equations corresponding to the desired design optimization goals. Boundaries for the core parameters can be obtained, allowing quick identification of feasible design solutions complying with all design constraints. A design example regarding the transformer of a multi-output forward converter is presented and discussed.

3.1 Transformer Thermal Model and GFFs

Each commercial magnetic core is identified by a set of values W_A, A_C, L_m, L_{MLT}. Figure 3.1 shows the shape of an *EE* core with relevant geometric measures. Such physical parameters are strongly influenced by the entire core geometry. At the same time, the values of W_A, A_C, L_m, L_{MLT} strongly influence the values of the primary winding turns number n_0 and the value B_{ac}, which are mutually dependent design

parameters too. In particular, n_0 is involved into the physical winding turns realization, whereas flux density B_{ac} is a magnetic operating parameter. The main transformer design problem consists in fixing n_0 and B_{ac} in such a way that the total loss and the magnetic flux density are jointly kept below given limits by using the smallest magnetic core [2]. For this goal is realistically achieved, thermal operating conditions of core and windings must be necessarily considered [3]-[9].

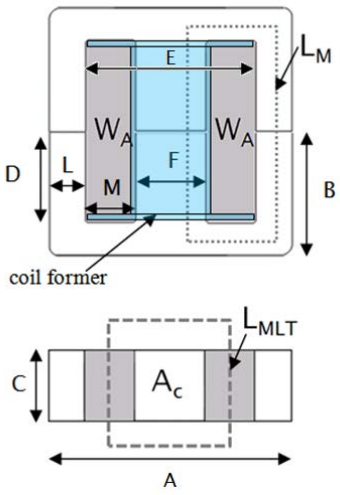


Figure 3.1 EE cores shape and transformer geometric measures.

The dependency of windings resistivity on the temperature T_{Cu} is expressed by (1)

$$\rho(T_{Cu}) = \rho_{25^\circ}\left[1+\alpha_T\left(T_{Cu}-25^\circ\right)\right] \tag{1}$$

where ρ_{25° and α_T are copper characteristic constants. The dependency of core losses on the temperature is more involved and it greatly depends on the material. In modern high frequency switching power supplies soft ferrites are mostly used for high-frequency magnetic devices. Soft ferrite show various dependency of loss density $p_{core}(T_{Fe}, f_s, B_{ac})$ on the temperature T_{Fe} and usually exhibit a minimum value of core loss density, which depends on the core material and corresponds to a certain value of temperature (T_{ML}), usually ranging from 40°C to 100°C and beyond, like shown in Figure 3.2 [10].

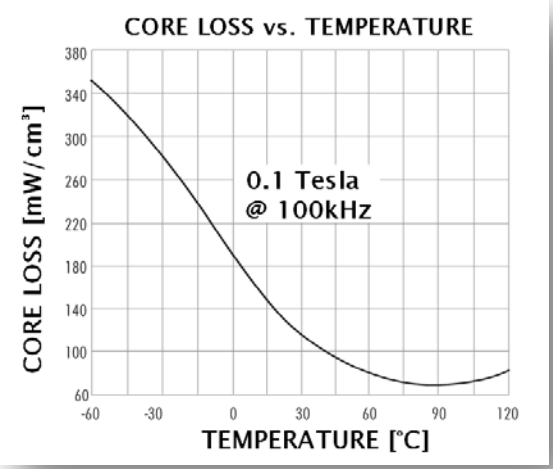


Figure 3.2 Core loss density *vs* core temperature (MAGNETICS Type R material [10]).

The Minimum Loss Density Point (MLDP) location is conditioned by the amplitude of *ac* component of flux density B_{ac} and the switching frequency f_s. Manufacturers provide loss density thermal curves for discrete values of B_{ac} and discrete values of frequency f_s. If the core operates in the range of temperature below the MLDP thermal stability is guaranteed. If the operating point enters the region where loss density is increasing, thermal instability may occur, with possible rise of the core temperature up to the Curie temperature. In the best case, the core might theoretically reach a stable thermal equilibrium, depending on thermal conductivity, at some temperature below the Curie temperature: however, no information would be available about the temperature and the losses in these conditions. A reliable transformer design, instead, must guarantee a predictable operating core temperature, located sufficiently below the MLDP, and predictable losses.

The core loss density $p_{core}(T_{Fe},f_s,B_{ac})$ can be determined by extracting data from technical datasheets of core manufacturers. The function p_{core} is usually expressed as in (2):

$$p_{core}\left(T_{Fe}, f_s, B_{ac}\right) = f_s^{\,c} B_{ac}^{\beta} \sum_{k=0}^{N_p} p_k T_{Fe}^{k} \tag{2}$$

where p_k and N_P are dependent on the core material type. The coefficients p_k in (2) can be extracted by interpolation of graphs of loss density curves vs core temperature (see Figure 3.2). For any set of values of f_s and B_{ac} it is possible to get an approximated estimation of the corresponding value of $p_{core}(T_{fe},f_s,B_{ac})$ as shown in (3):

$$p_{core}\left(T_{Fe}, f_s, B_{ac}\right) = p_{core}\left(T_{Fe}, f_{s,ref}, B_{ac,ref}\right)\left(\frac{f_s}{f_{s,ref}}\right)^{c}\left(\frac{B_{ac}}{B_{ac,ref}}\right)^{\beta} \tag{3}$$

A complete thermal model of the transformer can be obtained by considering the transformer thermal resistances of the thermal equivalent model discussed in [3]. The thermal resistance of interest are shown in Figure 3.3 and given by (4)-(6) (see List of Symbols):

$$R_{\theta v,Fe} = \frac{1}{h_{v,Fe} A_{v,Fe}} \tag{4.a}$$

$$R_{\theta h,Fe} = \frac{1}{h_{h,Fe} A_{h,Fe}} \tag{4.b}$$

$$R_{\theta,Fe} = \frac{R_{\theta v,Fe} \cdot R_{\theta h,Fe}}{R_{\theta v,Fe} + R_{\theta h,Fe}} \tag{4.c}$$

$$R_{\theta,Cu}{}' = \frac{1}{h_{Cu} A_{Cu}} \tag{5.a}$$

$$R_{\theta,Cu}{}'' = \frac{\ln\left(r_w / r_{cf}\right)}{2\pi K_{Cu} h_w} \tag{5.b}$$

$$R_{\theta,Cu} = R_{\theta,Cu}{}' + R_{\theta,Cu}{}'' \tag{5.c}$$

$$R_{\theta,cf} = \frac{\ln\left[\left(r_{cf} + \Delta_f\right) / r_{cf}\right]}{2\pi K_{cf} h_{cf}} \tag{6}$$

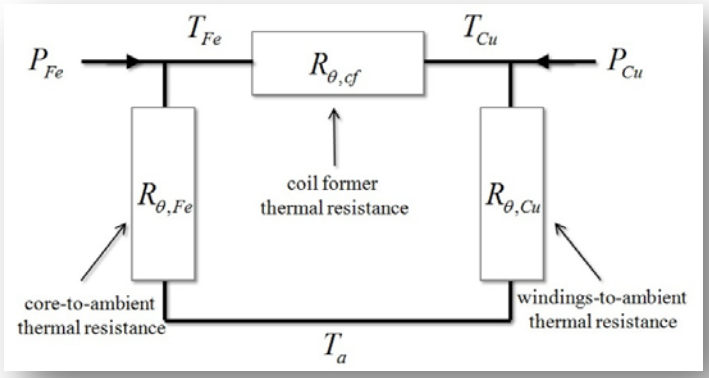


Figure 3.3 Transformer thermal model.

The thermal resistances $R_{\vartheta,Fe}$, $R_{\vartheta,Cu}$ and $R_{\vartheta,cf}$ and the powers P_{Fe} and P_{Cu} can be all written as functions of W_A and A_c, by considering the dependency of L_m and L_{MLT} on W_A and A_c. As a consequence, it is possible to write the following system of equations:

$$P_{Cu} = \rho(T_{Cu})\gamma_{Cu}(A_c, W_A) \tag{7}$$

$$P_{Fe} = p_{core}(T_{Fe}, f_s, B_{ac})\gamma_{Fe}(A_c, W_A) \tag{8}$$

$$T_{Cu} = T_a + R_{Cu}P_{Cu} + R_m P_{Fe} \tag{9}$$

$$T_{Fe} = T_a + R_m P_{Cu} + R_{Fe}P_{Fe} \tag{10}$$

$$R_{\vartheta,tot} = R_{\vartheta,tot}(T_{Cu}, T_{Fe}, A_c, W_A) = R_{\vartheta,Cu} + R_{\vartheta,Fe} + R_{\vartheta,cf} \tag{11}$$

$$R_m = R_m(T_{Cu}, T_{Fe}, A_c, W_A) = R_{\vartheta,Cu}R_{\vartheta,Fe} / R_{\vartheta,tot} \tag{12}$$

$$R_{Fe} = R_{Fe}(T_{Cu}, T_{Fe}, A_c, W_A) = R_{\vartheta,Fe}(R_{\vartheta,Cu} + R_{\vartheta,cf}) / R_{\vartheta,tot} \tag{13}$$

$$R_{Cu} = R_{Cu}(T_{Cu}, T_{Fe}, A_c, W_A) = R_{\vartheta,Cu}(R_{\vartheta,Fe} + R_{\vartheta,cf}) / R_{\vartheta,tot} \tag{14}$$

Depending on the specific application, different strategies can be applied in the transformer design, complying with maximum core temperature rise, maximum total loss, equalized core and windings

temperatures, minimum core size. Whatever design strategy is preferred, selection of adequate magnetic cores allowing the physical realization of the transformer is always the key issue. Starting point of the proposed design method is the characterization of cores of interest. For sake of clarity, let us refer here to the case of type R material EE cores (see Figure 3.1). Defined the geometric form factors h = D/M, w = F/C, d = B/D and g = L/F, the mean lengths of magnetic path and windings turn can be written as shown in (15) and (16):

$$L_m = \left[(d+1)\sqrt{2h} + \sqrt{2/h} \right] W_A^{1/2} + \left[2g\sqrt{w} \right] A_c^{1/2} = K_A^m W_A^{1/2} + K_c^m A_c^{1/2} \qquad (15)$$

$$L_{MLT} = \left[\sqrt{8/h} \right] W_A^{1/2} + \left[2(w+1)/\sqrt{w} \right] A_c^{1/2} = K_A^{MLT} W_A^{1/2} + K_c^{MLT} A_c^{1/2} \qquad (16)$$

The four form factors h, w, d and g vary core-by-core, as shown in Figure 3.4 for a set of 30 Magnetics EE cores, whose main dimensions are included in Table 3.1. Let h_A, w_A, d_A and g_A be the average values of the four form factors for this set of EE cores. For each core, it is possible to define two equivalent values W_{Ae} and A_{Ce} such that the values of core and copper losses calculated according to (1) and (2) using the average values of the four form factors correspond to the losses calculated using real values of W_A and A_C form factors. In order to achieve this result, the equations system given by (17) and (18) must be fulfilled:

$$\frac{A_{ce}\left[K_{Aa}^m W_{Ae}^{1/2} + K_{ca}^m A_{ce}^{1/2} \right]}{A_{ce}^{\beta}} = \frac{A_c\left[K_A^m W_A^{1/2} + K_c^m A_c^{1/2} \right]}{A_c^{\beta}} \qquad (17)$$

$$\frac{\left[K_{Aa}^{MLT} W_{Ae}^{1/2} + K_{ca}^{MLT} A_{ce}^{1/2} \right]}{W_{Ae}} = \frac{\left[K_A^{MLT} W_A^{1/2} + K_c^{MLT} A_c^{1/2} \right]}{W_A} \qquad (18)$$

Analytical solution of (17)(18) for W_{Ae} and A_{ce} is not available. An iterative numerical method must be adopted to solve the non linear equations system for the given set of magnetic core, for which the related form factors (h, w, d, g, h_A, w_A, d_A, g_A) and the specific constants ($K_{Aa}^{MLT}, K_{ca}^{MLT}, K_A^{MLT}, K_c^{MLT}, K_{Aa}^m, K_{ca}^m, K_A^m, K_c^m$) should be evaluated from the magnetic core data available on manufacturers catalogues [10].

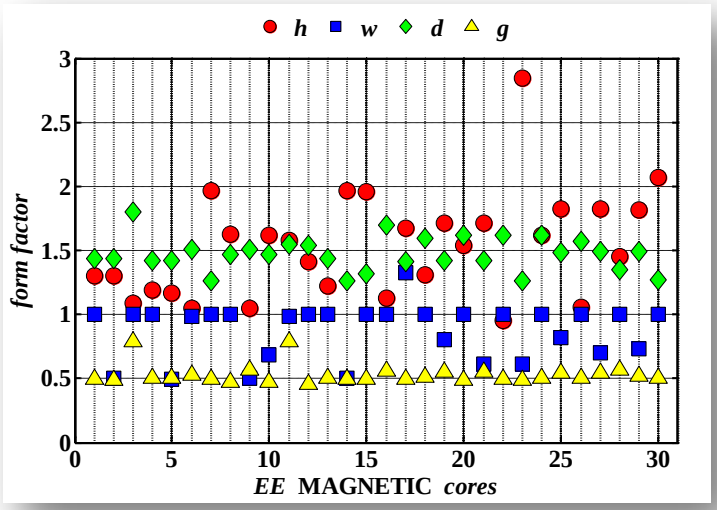
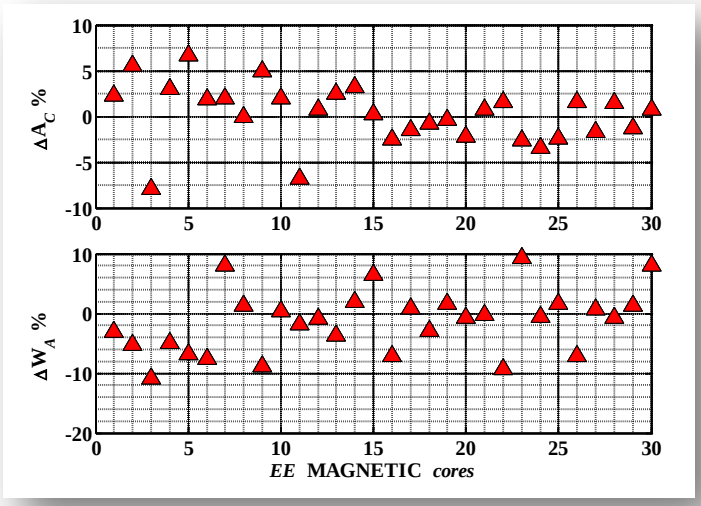


Figure 3.4 Form factors of EE cores.

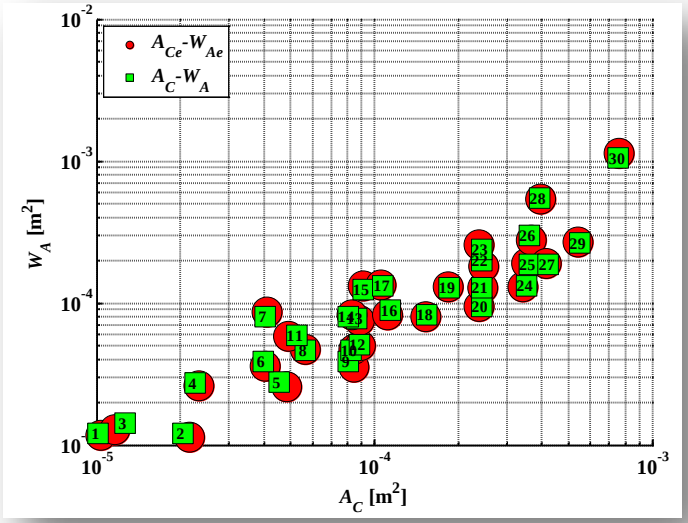
A Netwon-Raphson-based routine has been implemented in MATLAB®, assuming a maximum number of iteration n_{max}=20 and a minimum value of tolerance *tol*=1e-20. The percentage deviation of the (W_{Ae}, A_{ce}) *equivalent* values with respect to (W_A, A_C) *real* values is represented in Figure 3.5(a): for each core, the discrepancy among equivalent values (red circles) and real values (green squares) is less than 10%. In Figure 3.5(b) *equivalent* real geometrical constants (W_{Ae}, A_{ce}) and real geometrical constants (W_A, A_C) for EE cores are shown.
From (17)(18) and the (W_{Ae}, A_{ce}) equivalent values, let consider the equivalent GFF of each magnetic core, namely K_{feq} and K_{ceq}. The percentage deviation of the (K_{feq}, K_{ceq}) *equivalent* values with respect to (K_f, K_c) *real* values is represented in Figure 3.6(a): the almost vanishing discrepancy among the equivalent values (red circle) and real values (green squares) confirm the reasonable use of equivalent geometrical constants. In Figure 3.6(b) *equivalent* real geometrical constants (K_{feq}, K_{ceq}) and real geometrical constants (K_f, K_c) for EE cores are shown.

Table 3.1 *EE R*-type MAGNETICs core dimensions

Cores Part Code	dimensions [mm]							
	A	B	C	D	E	F	L	M
0R41203EC	12,70	5,69	3,18	3,96	9,19	3,18	1,57	3,05
0R41205EC	12,70	5,69	6,40	3,96	9,20	3,20	1,57	3,05
0R41707EC	16,80	7,11	3,56	3,94	10,40	3,56	2,79	3,63
0R41808EC	19,10	8,10	4,75	5,70	14,33	4,75	2,38	4,79
0R41810EC	19,30	8,10	9,53	5,70	14,00	4,75	2,38	4,89
0R42510EC	25,40	9,65	6,35	6,40	18,80	6,25	3,30	6,10
0R42513EC	25,00	12,80	7,50	8,70	17,50	7,50	3,55	5,35
0R42515EC	25,40	15,90	6,35	12,60	18,80	6,35	3,12	6,40
0R42520EC	25,40	9,65	12,70	6,40	18,80	6,35	3,60	6,10
0R42526EC	25,00	12,80	11,00	8,70	17,50	7,50	3,53	5,37
0R42530EC	25,40	15,90	12,70	12,60	18,80	6,35	3,12	6,40
0R43007EC	30,80	15,01	7,30	9,71	19,50	7,20	5,65	6,15
0R43009EC	30,95	13,10	9,40	8,50	21,41	9,40	4,29	6,00
0R43515EC	34,20	14,10	9,30	9,80	25,50	9,30	4,70	8,00
0R43520EC	34,90	20,62	9,53	15,60	25,10	9,53	4,75	7,95
0R44011EC	40,01	17,00	10,69	10,00	27,60	10,70	5,99	8,86
0R44016EC	42,15	21,10	9,00	14,90	29,50	11,95	5,94	8,90
0R44020EC	43,00	21,00	15,20	14,80	29,50	12,20	6,75	8,65
0R44022EC	43,00	21,00	20,00	14,80	29,50	12,20	6,75	8,65
0R44033EC	42,00	32,80	20,00	26,00	29,50	12,20	5,98	9,13
0R44317EC	40,60	16,60	12,40	10,40	28,60	12,45	6,33	7,95
0R44721EC	46,90	19,60	15,60	12,10	32,40	15,60	7,54	7,87
0R45528EC	56,20	27,50	21,00	18,50	37,50	17,20	9,35	10,15
0R45530EC	56,20	27,60	24,61	18,50	37,50	17,20	9,35	10,15
0R45724EC	56,10	23,60	18,80	14,60	38,10	18,80	9,50	9,03
0R46016EC	59,99	22,30	15,62	13,80	44,00	15,62	7,70	14,49
0R46527EC	65,00	32,80	27,40	22,00	44,20	20,00	10,40	12,10
0R47228EC	72,40	27,90	19,00	17,80	56,60	19,00	9,53	16,90
0R48020EC	80,00	38,10	19,80	28,20	59,10	19,80	11,25	19,45
0R49928EC	100,30	59,40	27,50	46,85	72,00	27,50	13,75	22,65

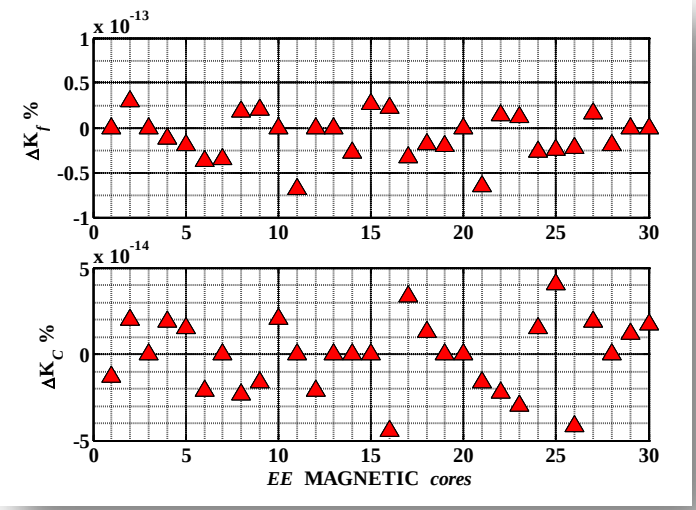


(a)

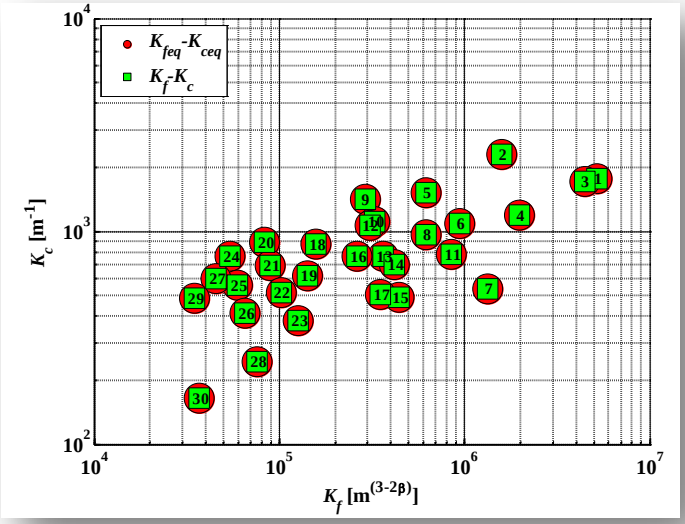


(b)

Figure 3.5 (a) Percentage deviation between A_C-A_{Ce} and W_A-W_{Ae} values; (b)Equivalent and real geometrical constants for EE cores.



(a)



(b)

Figure 3.5 (a) Percentage deviation between K_f-K_{feq} and K_C-K_{ceq} values; (b) Equivalent and real geometrical constants for EE cores.

3.2 Acceptability Boundary Curve for Magnetic Cores Selection

The following design approach is aimed at achieving magnetic core selection which complies with one of the following goals:

- ***a)*** given the primary turns number n_0 which is desirable to use, find the smallest core, *or*
- ***b)*** given a certain core which is desirable to use, find the primary turns number n_0,

such that the transformer always fulfils the following constraints:

- ***i)*** the total power loss must be lower than the maximum allowed power loss $P_{tot,max}$;
- ***ii)*** the ac component of core magnetic flux density must be lower than the maximum allowed flux density $B_{ac,max}$;
- ***iii)*** the core temperature must be lower than the maximum allowed temperature $T_{Fe,max}$.

Solving problem *a*) means determining a Region of Acceptability (RoA) in the K_f-K_c plane, such that all cores having couples of equivalent values (K_{feq}, K_{Ceq}) falling within RoA admit transformer design complying with constraints *i*)-*ii*)-*iii*). The curve bounding the RoA is called Acceptability Boundary Curve (ABC). Smallest cores allowing the transformer design can be easily detected by means of the concept of the ABCs [11].

Solving problem *b*) means verifying if a certain core allows the transformer design complying with constraints *i*)-*ii*)-*iii*). As the ABC changes with n_0, solving problem *b*) allows to seek possible values of n_0 such that a given core falls inside the RoA.

Both problems *a*) and *b*) can be solved analytically only if thermal issues are neglected, as shown in previous chapter, by assuming $\rho(T_{Cu})=\rho_{25^\circ}$ and $p_{core}=K_{fe}\,B_{ac}{}^{\beta}$ in formulas (1) and (2), respectively. In this case, the equations system (7)-(10) shrinks into the couple of equations (7)(8). However, if core thermal stability must be verified and the operating point has to be identified, then equations system (7)-(10) must be solved. Indeed, there is no guarantee that solving the reduced equations system (7)(8) by neglecting thermal issues leads to

compliance with constraints *i*)-*ii*)-*iii*). Let then examine the difference among design solutions achieved with simplified solution and solutions found by numerical computation including thermal modeling. For instance, let suppose that the design objective is given by goal *a*). The choice of n_0 is not a trivial problem. In fact, as preliminary constraint, the numerical value of the design solution for all transformer parameters must have physical consistence, in order to guarantee magnetic device physical feasibility. The port voltages are related each other by the conversion ratio $M(D)$, depending on the converter topology, and by windings turns numbers, according to (19):

$$\frac{n_j}{n_0} = \frac{V_{oj}}{M(D)V_i}, \qquad j = 1,..,m \tag{19}$$

where m represents the number of the converter outputs. In particular, all the number of turns n_j ($j=0,..,m$) must be integer and bigger than unity. For whatever multi output power supply it is always possible to sort the outputs for decreasing voltage. Let assume, without loss of generality, that the m-th winding of the transformer is terminated on the minimum voltage output V_{oM}, so that if the turns number $n_M \in \mathbb{N}^+$, then the same constraint will be fulfilled by the turns number n_j of all the other *m-1* output windings:

$$n_j = round\left(\frac{V_{oj}}{V_{oM}} n_M\right) \geq 1, \qquad j = 1,..,m,\ j \neq M \tag{20}$$

where the operator $round(x)$ provides the integer number closest to the argument x. According to (19) and (20), the primary winding turns number n_0 is given by (21):

$$n_0 = round\left(n_M \frac{V_i M(D)}{V_{oM}}\right) \tag{21}$$

However, n_0 and B_{ac} are related each other by (22):

$$B_{ac} = \frac{1}{2 f_s n_0 A_c} \int_{T_m} V_T dt \tag{22}$$

where V_T is the voltage applied to the primary winding of the transformer during the magnetizing time T_m, which change with the

converter topology. From (21) and (22), constraint ***ii)*** involves that the primary turns number n_0 must finally satisfy condition (23):

$$n_0 \geq n_{0,\min} = round\left\{\max\left[\left(\frac{1}{2B_{ac,\max}A_c}\int_{T_m} V_T dt\right),\left(n_M \cdot \frac{V_i M(D)}{V_{oM}}\right)\right]\right\} \tag{23}$$

The choice of minimum windings turns number n_M greatly influences transformer design. From (20), the smaller the n_M, the smaller all other windings turns numbers: so that, the windings length will decrease and cores with bigger K_c (i.e. smaller window area W_A) can be used. However, smaller the n_M, smaller also the turns number n_0: thus, the core flux density and the resulting core losses are expected to increase and cores with smaller K_f (i.e. bigger cross section area A_c) are needed. Moreover, small turns numbers increase leakage inductances. On the contrary, using higher turns numbers reduces leakage inductances and core flux density, but increase copper losses: thus, bigger K_f and smaller K_c are needed. Consequently, both too small and too big windings turns numbers increase the core size. Based on the previous observations, for any given set of design specifications there will likely be some optimal value of turns numbers allowing the use of minimum size core.

The model discussed in this chapter is aimed at investigating the effect of thermal properties of core and windings on the optimum turns number and core size. To this purpose ideal *Non-Thermal* ABCs (NT-ABCs) and real *Thermal* ABCs (T-ABCs) have been determined, as in the follow.

Referring to the equivalent GFFs (K_{feq}, K_{Ceq}), let consider system made by equations (24):

$$P_{Cu}(T_{Cu}, K_{feq}, K_{ceq}) = \rho(T_{Cu})\gamma_{Cu}(K_{feq}, K_{ceq}) \tag{24.a}$$

$$P_{Fe}(T_{Fe}, K_{feq}, K_{ceq}) = p_{core}(T_{Fe}, f_s, B_{ac})\gamma_{Fe}(K_{feq}, K_{ceq}) \tag{24.b}$$

$$T_{Cu} - T_a = R_{Cu}P_{Cu}(T_{Cu}, K_{feq}, K_{ceq}) + R_m P_{Fe}(T_{Fe}, K_{feq}, K_{ceq}) \tag{24.c}$$

$$T_{Fe} - T_a = R_m P_{Cu}(T_{Cu}, K_{feq}, K_{ceq}) + R_{Fe}P_{Fe}(T_{Fe}, K_{feq}, K_{ceq}) \tag{24.d}$$

The four equations system (24) contains six unknowns, which are: P_{Cu}, P_{Fe}, T_{Cu}, T_{Fe}, K_{feq} and K_{ceq}: two unknown must be fixed in order to get a system solution. Through the MATLAB® symbolic toolbox,

NT-ABCs can be obtained by solving equations (24.a)(24.b) with the constraint $P_{Cu}+P_{Fe} = P_{tot,max}$ and assuming fixed temperatures $T_{Fe}=T_{ML}$ and $T_{Cu}=T_a$. The symbolic expression of NT-ABC providing K_{feq} as function of K_{ceq} and n_0 is presented in (25)

$$K_{feq}(n_0, K_c) = \frac{P_{tot,\max} n_0^{\beta} \chi^{\beta} - \Gamma_c n_0^{\beta'} \chi^{\beta'} K_c}{\Gamma_f} \tag{25}$$

where, according to (19), χ is given by (26):

$$\chi = \frac{V_{oM}}{D \cdot V_i} \tag{26}$$

T-ABCs, instead, cannot be determined in analytical form, even using the MATLAB® symbolic toolbox. They can be obtained only by solving system (24) by means of an iterative numerical technique. Taking into account thermal properties of core and windings allows to get different types of T-ABCs, each one corresponding to different constraints. In particular, three different kinds of T-ABCs have been determined, according to the three following constraints:

c1) $P_{Fe}+P_{Cu} = P_{tot,max}$; *c2)* $T_{Fe}=T_{Fe,max}$; *c3)* $T_{Fe}=T_{Cu}$.

Constraints *c1*) and *c2*) express the compliance of transformer design with power loss and thermal stability constraints. Constraint *c3*) is of interest too, as having equal temperatures of core and windings means to have only heat flow towards outside of the transformer. Such condition would be optimal for heat dissipation, as there would be no reciprocal heating between core and windings.

3.2.1 Case Study

The transformer design of a seven outputs low power Forward converter is taken as case study, complying with the following specifications: $V_i=48V$, $V_{o1}=10V@1A$, $V_{o2}=7V@1.5A$, $V_{o3}=5V@1.5A$, $V_{o4}=3.3V@1.5A$, $V_{o5}=-10V@0.5A$, $V_{o6}=-5V@1.5A$, $V_{o7}=-7V@0.5A$, $f_s=250kHz$, $D=0.5$, η=88%, $P_{tot,max}=500mW$, (corresponding to 8% of the maximum power dissipation), K_u=0.5, n_M=4, B_{sat}=0.35 and $T_{Fe,max}$=75°C. In Figures 3.6 and 3.7, the *3D* plots of $\{P_{Fe}, P_{Cu}, P_{tot}\}$and $\{T_{Fe}, T_{Cu}\}$as function of (K_C, K_F), obtained by means of a NR numerical algorithm, are shown respectively.

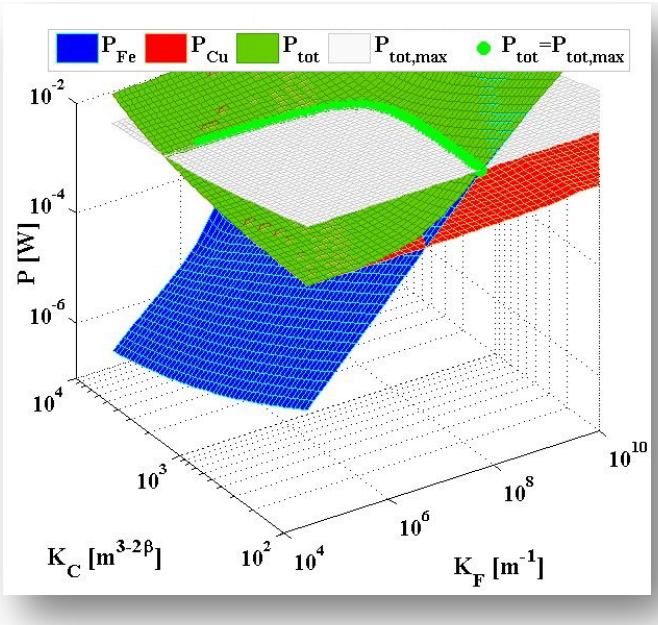


Figure 3.6 *3D* Surface plot of core, copper and total losses.

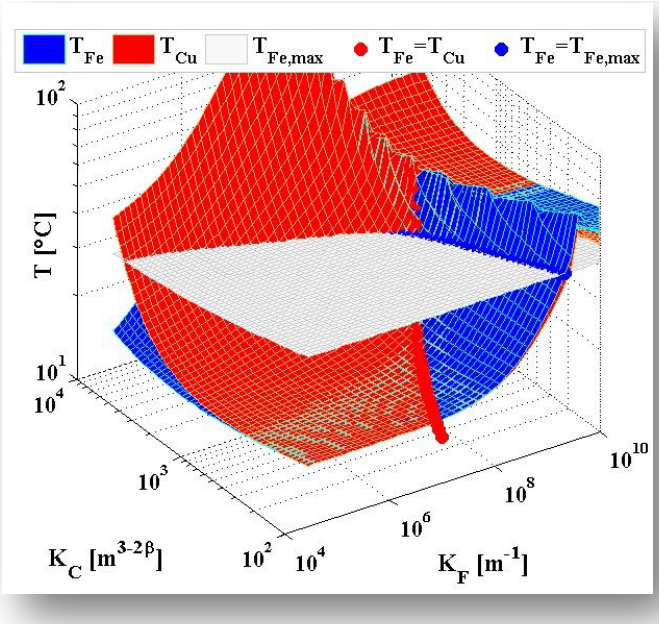


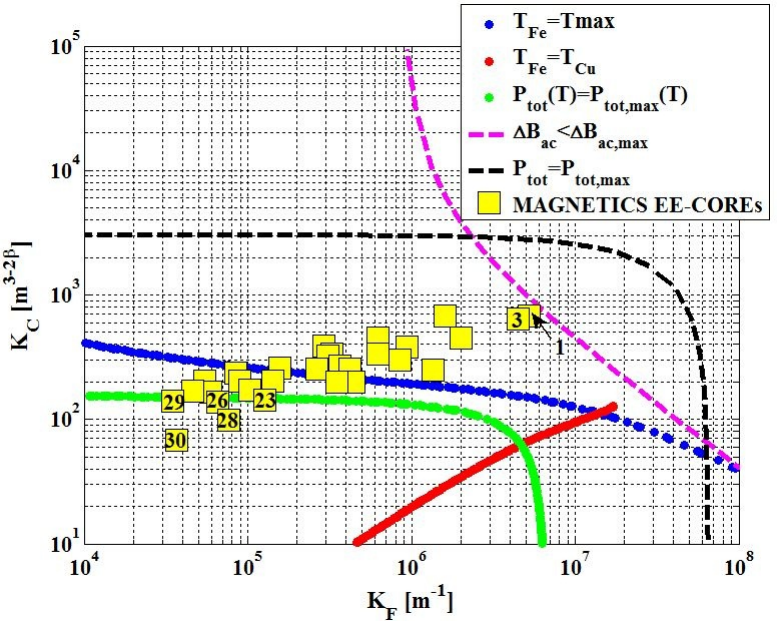
Figure 3.7 *3D* Surface plot of core and copper temperatures.

Figure 3.6 shows how core, copper and total losses change depending on the couple of values (K_C, K_F). The sequence of green circle points where total losses equal the maximum allowed value $P_{tot,max}$ (light grey horizontal plane) identifies the Type 1 T-ABC, determined by means of Newton-Raphson technique and reported in Figure 3.8(a). Figure 3.7 shows how core and copper temperatures change depending on the couple of values (K_C, K_F). The sequence of blue and red circle points where core temperature equals respectively the maximum allowed value $T_{Fe,max}$ (light grey horizontal plane) and the windings temperature (red surface) identify the Type 2 and Type 3 T-ABC, determined by means of Newton-Raphson technique and reported in Figure 3.8(a), too.

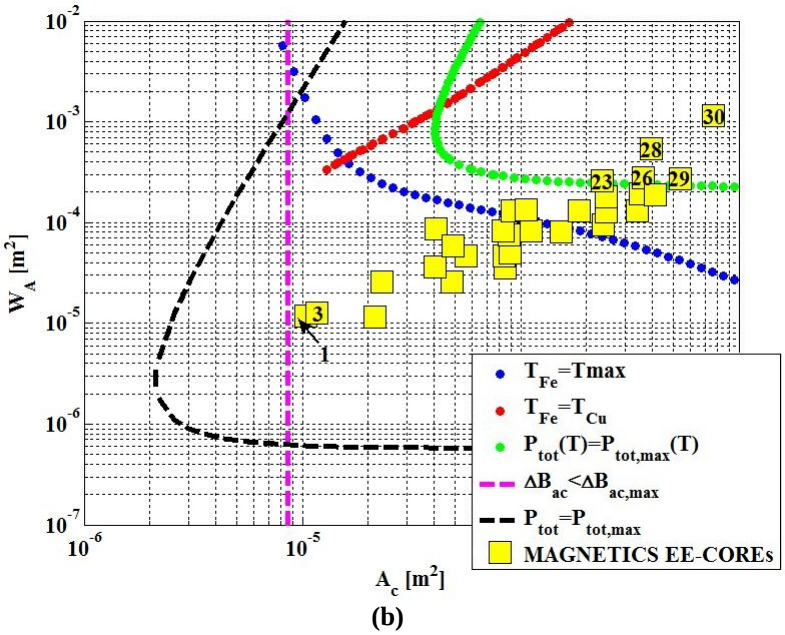
For the given case study, both T-ABCs and NT-ABCs are shown in Figure 3.8(a). Blue T-ABCs are the loci of couples (K_{Feq}, K_{Ceq}) ensuring $T_{Fe}=T_{Fe,max}=75°C$: couples (K_{Feq}, K_{Ceq}) lying down-left side the blue T-ABCs correspond to cores ensuring $T_{Fe}<T_{Fe,max}$. Red T-ABCs are the loci of couples (K_{Feq}, K_{Ceq}) ensuring $T_{Cu}=T_{Fe}$: couples (K_{Feq}, K_{Ceq}) lying down-right side the red T-ABCs correspond to cores ensuring $T_{Cu}<T_{Fe}$. Green T-ABCs are the loci of couples (K_{Feq}, K_{Ceq}) ensuring $P_{tot}=P_{tot,max}$: couples (K_{Feq}, K_{Ceq}) lying down-left side the green T-ABCs correspond to cores ensuring $P_{tot}<P_{tot,max}$. Magenta dash-dot line is the locus of couples (K_{Feq}, K_{Ceq}) ensuring $\Delta B_{ac}<\Delta B_{ac,max}$: couples ($K_{Feq}$, K_{Ceq}) lying down-left side the magenta line correspond to cores ensuring limitation of magnetic flux density below $B_{ac,max}$. Black dash-dot line correspond to the NT-ABC: couples (K_{Feq}, K_{Ceq}) lying down-left side the black NT-ABCs correspond to cores that, ensure $P_{tot}<P_{tot,max}$, neglecting thermal effects.

Figure 3.8(a) shows that, with $n_M=4$, the smallest cores allowing the design of the transformer and fulfilling the constraints *c1*)-*c3*) are *#23*, #26 and *#28*. Neglecting thermal effects would qualify cores *#1* and *#3* as suitable for the design. In Figure 3.8(b), similar considerations can be done, referring to (A_c, W_A) – based NT-ABCs and T-ABCs.

Figures 3.9 to 3.11 show the plots of magnetic cores data (K_{Feq}, K_{Ceq}) together with the NT-ABCs (black dash curves) and Type 1 to 3 T-ABCs (green, blue and red curves), for $n_M=\{3, 2, 1\}$.



(a)



(b)

Figure 3.8 ABCs for n_M =4 in (K_f, K_c) plane (a) and in (A_c, W_A) plane (b).

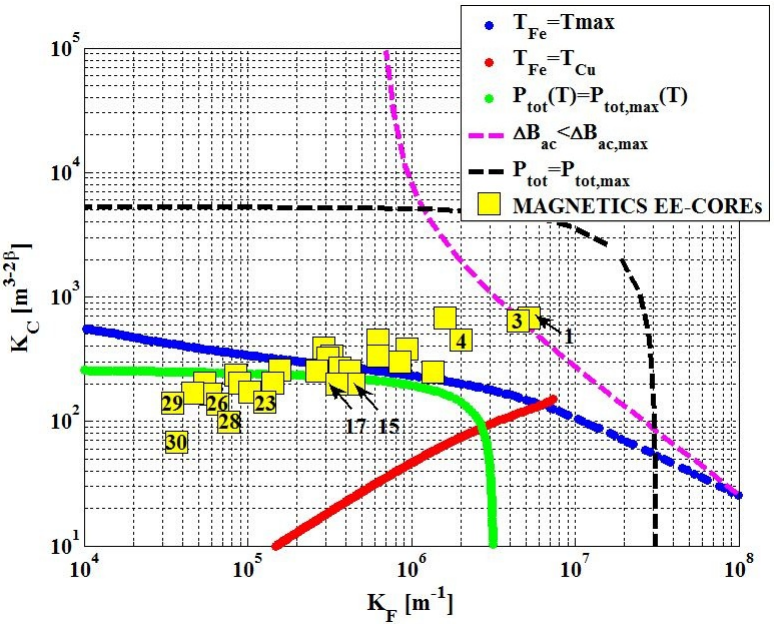


Figure 3.9 ABCs for n_M =3 in (K_f, K_c) plane.

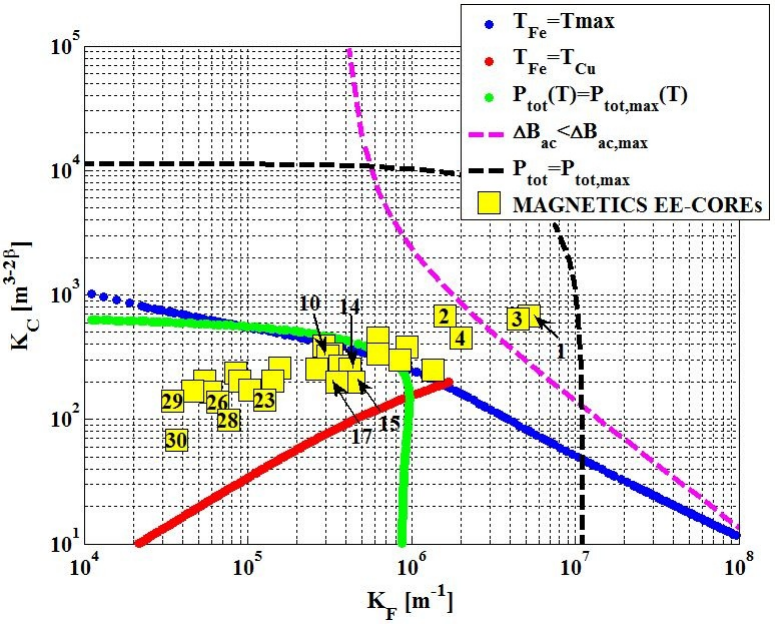


Figure 3.10 ABCs for n_M =2 in (K_f, K_c) plane.

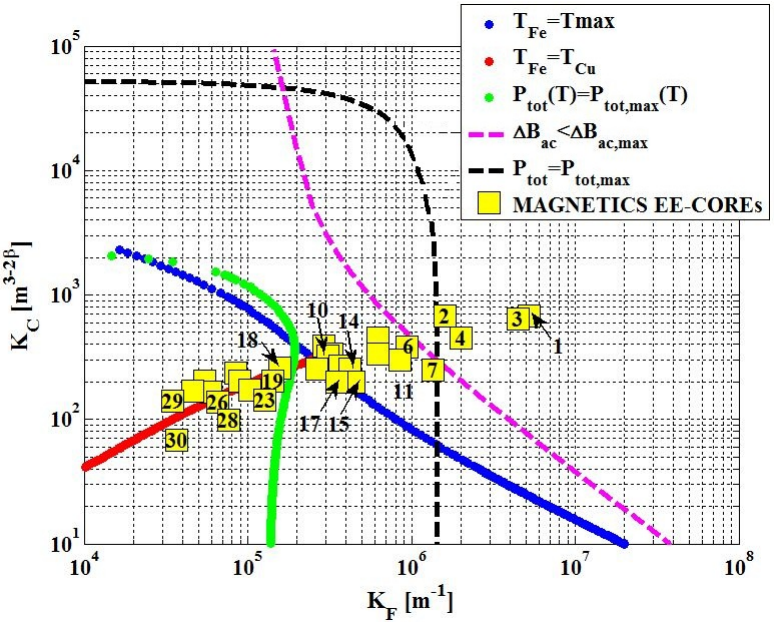


Figure 3.11 ABCs for n_M =1 in (K_f, K_c) plane.

Let us now summarize the key points. Figures 3.8 - 3.11 show that the smallest cores allowing the design of the transformer and fulfilling the constraints *c1*)-*c3*) are:

- for $n_M=4$ (Figure 3.8), *#23, #26* and *#28*;
- for $n_M=3$ (Figure 3.9), *#15* and *#17*;
- for $n_M=2$ (Figure 3.10), *#14* and *#15*;
- for $n_M=1$ (Figure 3.11), *#18* and *#19.*

Design solution obtained for $n_M=2$ is preferable as there is a margin both in the total transformer loss and core temperature with respect to the maximum allowed values, whereas design solutions obtained for $n_M=\{1, 3, 4\}$ are right on the bounds. Indeed, as various uncertainties affect real operating conditions and parameters, it is a good choice to stay far enough from ABCs in order to make the design solution more reliable. Moreover, it is possible to verify that rising n_M to 5 makes core *#30* the smallest and unique one allowing a compliant transformer design, with an increase of volume of a factor 2 with respect to core *#15*. Finally, for the given application, no feasible design solution exists for $n_M>5$. Evidently, $n_M=2$ is the best solution.

Figure 3.8(a) and Figures 3.9 - 3.11 show that the both Type 1 and Type 2 T-ABCs reach a certain maximum distance far from the origin, which identifies the minimum size cores allowing a design of the transformer complying with total loss (Type 1 T-ABC) or core temperature (Type 2 T-ABC) constraint. Plots of Figure 3.8(a) and Figures 3.9 - 3.11 highlight that for small turn numbers the core temperature constraint can become tighter than total loss one, whereas the opposite happens for big turns numbers. Indeed, the maximum distance point of the RoA moves from right bottom towards left top when turns number decreases, as shown in Figure 3.12. This means that cores with same volume but different shape are needed, depending on the choice of the turns number.

The RoA extension also depends on values of $T_{Fe,max}$ and $P_{tot,max}$ and on duty-cycle D and switching frequency f_s, which are global influence parameters for the isolated converter. Figures 3.13 and 3.14 show how the RoA moves towards bottom and toward right for higher values of duty-cycle D and switching frequency f_s, respectively.

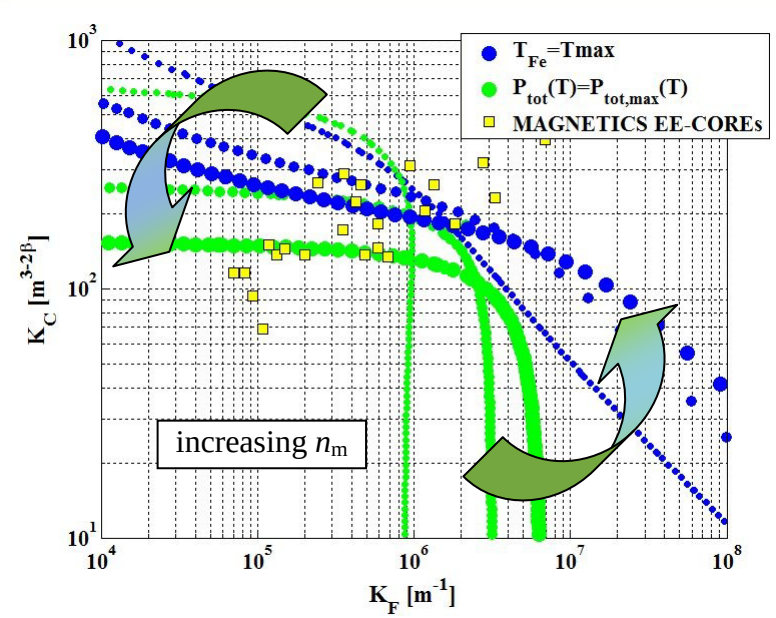


Figure 3.12 Type 1 and Type 2 T-ABCs for *D=0.5*, f_s*=250kHz*, n_M*={2,3,4}*.

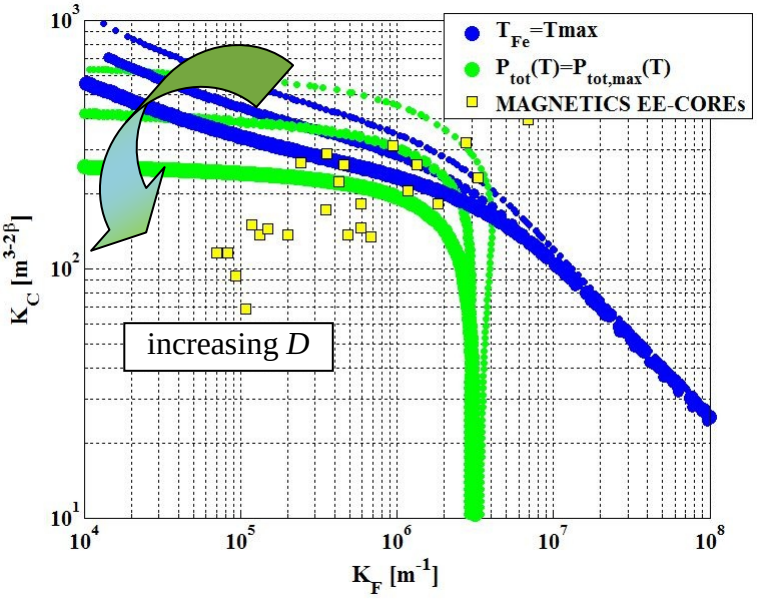


Figure 3.13 Type 1 and Type 2 T-ABCs for n_M =3, f_s=250kHz and D={0.2,0.4,0.6}.

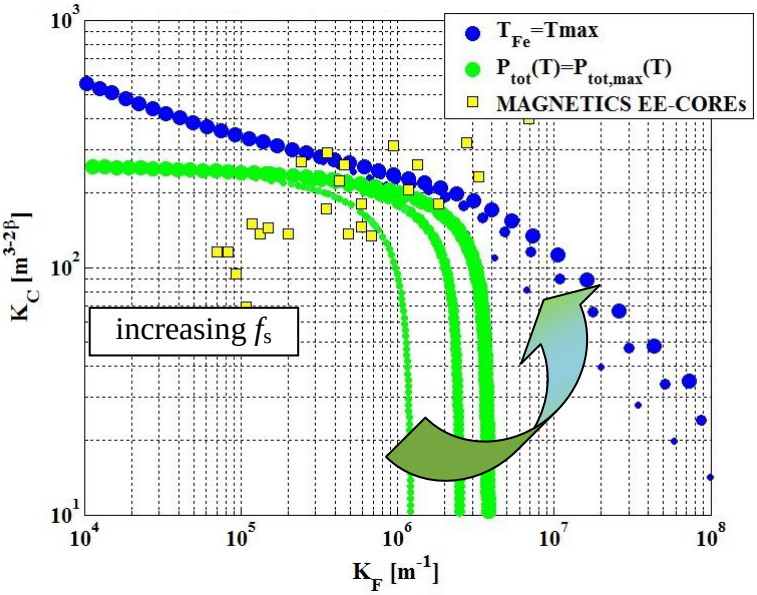


Figure 3.14 Type 1 and Type 2 T-ABCs for D=0.5, n_M=3 and f_s={100kHz, 200kHz, 300kHz}.

The core selection process based on T-ABCs can be summarized as follows:

- ***step#1*:** select families of cores of interest and calculate *h*, *w*, *d*, and *g* form factors and coefficients $K_A^{MLT}, K_c^{MLT}, K_A^m, K_c^m$ using cores datasheets
- ***step#2:*** calculate average values of form factors h_a, w_a, d_a, g_a and coefficients $K_{Aa}^{MLT}, K_{ca}^{MLT}, K_{Aa}^m, K_{ca}^m$
- ***step#3:*** generate equivalent (K_{feq}, K_{ceq}) couples by using formulas (17)(18)
- ***step#4:*** generate the system of equations (24.a)-(24.d) by using equations (1)-(14) with data of the specific design problem and formulas (15)(16) for the specific type of cores
- ***step#5:*** solve the system (24.a)-(24.d) with respect to (K_f, K_c)for different values of winding turns number n_M, with maximum total loss constraints and maximum core temperature *c1*) and *c2*), by means of a numerical technique (e.g. Newton-Raphson);
- ***step#6:*** plot Type 1 and Type 2 T-ABCs in the (K_f, K_c) plane together with equivalent (K_{feq}, K_{ceq}) couples of cores;
- ***step#7:*** repeat step#6 for different values of duty-cycle *D* or switching frequency f_s;
- ***step#8:*** identify design solution allowing the use of minimum size core for transformer design.

Comments

An investigation about the impact of temperature on optimal physical and operating parameters in transformer design for isolated dc-dc converters has been presented in this chapter. Using proper geometrical parameters scaling and form factors, together with thermal model of cores, lead to a non linear model whose solution allows the generation of Acceptability Boundary Curves for series of values of turns numbers n_0, duty-cycle *D* and switching frequency f_s, which enable an effective overall view of how the shape of the core impacts transformer and global converter performances. Thanks to the ABCs it is not necessary to make loss and temperature calculations for each commercial core of interest and it becomes easy to compare at

once many cores of different manufacturers, provided they are of the same type (EE, ETD, etc). Magnetic cores are preliminarily characterized by evaluating their thermal resistances and by expressing all the core geometric parameters as functions of the values (K_C, K_F) of the cores. The design problem is then translated into a feasibility investigation problem. The result is a quick and sharp classification of cores in suitable and unsuitable ones for the specific application. B_{ac} and turn number n_M are used as tuning parameters for the feasibility investigation, in order to generate a set of acceptability regions for magnetic cores in the parametric space associated to K_F and K_C. The results regarding the design case studies discussed above put in evidence that, depending on the application, the impact of thermal properties on the selection of the cores can be not so weak. This means that, if the achievement of transformer size minimization is needed for systems integration, then thermal properties of cores need to be taken into account to avoid overheating and unpredictable behavior.

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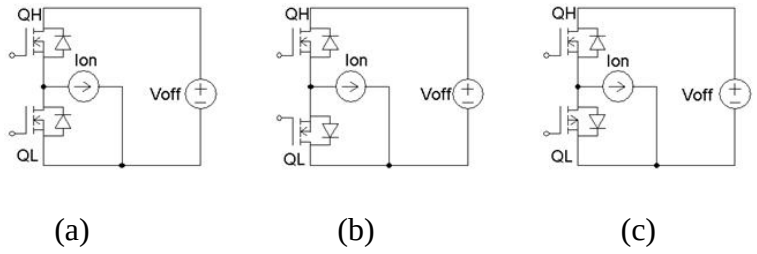
Chapter 4

MOSFETs Commutations Analysis

A novel method for the analysis of MOSFETs commutations and the evaluation of related losses and spike current issues in Switching Power Converters (SPC) design has been investigated. The Synchronous Rectification Switching Cells (SRSC) configuration, which is commonly used in High-Frequency High-Efficiency (H2EF) SPC design, is considered for the investigation. The proposed method is aimed at providing an effective tool for quick feasibility investigations and comparative evaluations among design solutions using different MOSFETs combinations for the design of H2EF SPCs. The method allows to use non-linear models of inter-electrode MOSFETs capacitances and adopts a novel numerical technique specifically developed to solve the SRSC model ensuring robust and fast simulations. Capacitive pulsating currents circulating through the MOSFETs and the SPC during commutations can be analyzed in detail by using the proposed method. Some examples are presented to show how the specific characteristics of MOSFETs and the operating conditions influence as the switching losses as the pulsing currents circulating through the SPC.

4.1 State of Art and research goals

A wide variety of topologies and switching techniques and several types of power silicon devices are adopted for switch mode power supplies design. Nevertheless, most of high-efficiency power supplies for low-voltage high-current DC-DC applications, such as Point-of-Load (PoL) and Telecom (TLC) regulators, use couples of MOSFETs to form the Synchronous Rectification Switching Cell (SRSC) configurations, also defined as Half-Bridge Leg, shown in Figure 4.1. Due to their positions, the two MOSFETs are commonly labeled as High-Side (HS) MOSFET (Q_H) and Low-Side (LS) MOSFET (Q_L).



(a) (b) (c)

Figure 4.1 Basic MOSFETs SRSC possible configurations: (a) N-channel MOSFETs with common source-drain;(b) N-channel MOSFETs with common source; (c) N-channel MOSFET and P-channel MOSFET with common source-drain.

Configurations (a) and (c) can be found in buck, boost and buck-boost converters and in primary side of active clamp Forward and Flyback converters. Configuration (b) can be found in self-driven secondary side of active clamp Forward converters. Depending on the specific topology, the voltage and current sources of Figure 4.1 may represent either real sources (e.g. battery) or passive energy storage devices (inductors, capacitors).

The model presented in this dissertation is referred to configuration (a), but it can be easily extended to other ones too. The focus is, in particular, on the analysis of switching losses and pulsating capacitive currents generated by MOSFETs commutations. The considered case studies are related to Low-Voltage High-Current (LVHC) MOSFETs, for which the problem of investigating numerous possible design alternatives is particularly important. In fact, while in Low-Voltage Low-Current (LVLC) dc-dc applications the use of controller IC with integrated MOSFETs and diode rectification is today mostly preferred, as it simplifies the regulator design, in most LVHC applications the use of external MOSFETs is still the main solution, due to efficiency and thermal issues. Many MOSFETs are today manufactured with integrated Schottky diode, specifically for PoL LVHC applications, in order to reduce the body-diode conduction losses during the dead-times and to avoid the effect of diode reverse recovery. However, the use of Schottky diodes increases the output capacitance of the MOSFET and this must be accounted for both in losses and in pulsating currents analysis. The selection of MOSFETs

for LVHC applications is then not so obvious and straightforward, in a scenario where the use of a very big number of different candidate parts and related combinations is allowed. Indeed, due to the increasing attention paid to energy saving issues and to the need of realizing small, cheap and well performing regulators, quick selection of couples of MOSFETs ensuring the desired trade-off is not easy. This is especially true in applications like FPGAs powering: in such context, the load is modular, and different voltage/current/power levels allow to use several different powering architectures each one requiring careful MOSFETs selection to achieve a good overall design. Such selection has also to take into account that the maximum switching frequency, which influences the size of passive components, is limited by MOSFETs losses [1].

In the following, two main issues connected to SRSC MOSFETs commutations in SPC operation are put in the focus: MOSFETs switching losses and MOSFETs capacitive currents circulating through the converter. The switching loss analysis is much more complicated than the analysis of conduction losses, as the waveforms of voltages and currents $v_{ds}(t)$, $i_{ds}(t)$, $v_{gs}(t)$ and $i_{gs}(t)$ during the commutations must be determined. This requires to take into account the MOSFET capacitances and their dependence on the voltages $v_{ds}(t)$ and $v_{gs}(t)$, which condition the transition from the interdiction region to the linear region passing through the saturation region. Although resonant techniques may help in reducing drastically the impact of the switching losses, they involve some complication in modeling and design and in increasing conduction losses. In the recent years many new MOSFETs have been introduced, which exhibit very small total gate charge and on-resistance product Q_g x $R_{ds,on}$ [2]. So that, in many applications, especially PoL and TLC ones, the basic hard-switching cells of Figure 4.1 offer good chances for the realization of low-cost high-efficiency low-power supplies. In this perspective, a reliable and quick switching loss analysis investigation of commercial MOSFETs, based purely on physical parameters provided in devices datasheets, is highly helpful to orient the design toward effective solutions. MOSFETs modeling and switching losses calculation are deeply treated in literature [3]-[5]. Over last decades, many studies have been presented in literature, highlighting the key importance of a proper modeling of non linear MOSFETs capacitance to get correct losses

prediction, especially in hard switching converters, and various approaches to MOSFETs modeling and related parameters extraction have also been proposed [6]-[14]. In particular, [12]-[14] discuss experimental tests allowing the identification of additional parameters, with respect to datasheets, which provide more accurate MOSFETs capacitances models for the analysis of commutations. Such parameters describe the area modulation effects of the varying gate-source and drain-source voltages on the inter-electrode capacitances during commutations. They are identified by means of empirical evaluations starting from experimental measurements during commutations. The parameters and the models obtained in this way are then fairly valid for the specific device under test in the operating conditions (voltage-current ratings, circuit layout, drivers, etc) adopted for the experimental tests. Libraries with MOSFETs models at different levels of detail are used in circuits simulators [15][16]. Detailed MOSFET models use the physical and geometrical parameters of the device and need circuit simulators. Such models are useful, and their use is meaningful, either when a MOSFET device is under design and deep characterization is needed to figure out its real performances and the way to optimize them, or when the MOSFETs for a certain power supply design have been selected and detailed waveforms and losses analysis is required to verify the compliance with loss restrictions and to for EMI analysis. Instead, if the problem is to design a power supply using existing commercial MOSFETs, sophisticated models and simulations are not needed nor they are useful, because the decision to select one device rather than another one is only based on data provided by MOSFETs manufacturers into datasheets, where only few fundamental parameters are available to globally characterize the devices in terms of power dissipation. Indeed, Printed Circuit Board (PCB) parasitic resistances and inductances also have a heavy influence on waveforms and losses during hard switching commutations in high-frequency power converters under real operating conditions [17][18]. The PCB, in turn, is fully defined only after that the power converter Bill of Material (BoM) is fixed and the layout is routed. As snubber circuits are often adopted to damp the oscillations caused by PCB parasitic effects, the switching waveforms are completely altered. Consequently, the detailed analysis of the effects of real MOSFETs capacitances on the

switching times and related losses is impeded. As a consequence, no meaningful and realistic experimental measurement of power MOSFETs switching losses in real world power converters operating conditions is allowed. Accurate measurements can only be valid for laboratory experiments realized by means of dedicated test boards, operated at de-rated switching frequency (tens of *kHz* vs hundreds *kHz* of normal conditions) which are far away from the final high-devices-density boards of power converter bricks. Moreover, inserting probes, sensing devices and snubbers into a real power converter board causes deep modification of waveforms. So that, thinking to validation of models for MOSFETs losses by means of experimental measurements does not make much sense, as pointed out in [4]. In real world, high-power-density high-switching-frequency power converters do not allow reasonable measurement at device level: only input/output rails voltage currents make sense for global efficiency measurements. For all the above reasons, there is neither a way nor a sense in trying to achieve accurate MOSFETs switching loss calculation (intended as determination of a mere number providing the value of switching losses of each device with a good degree of accuracy) in power converters, while these devices are under evaluation during the design of a power converter. Switching loss analysis (intended as comparative evaluation among the different devices to understand which is the impact of their main capacitive characteristics on switching losses) is only allowed and meaningful. Such kind of investigation is helpful in realizing a classification of MOSFETs and related technologies, in terms of application-dependent dissipation bent. For example, trench technology power MOSFETs are mostly used in PoL applications: manufacturers provide many MOSFETs devices whose current and voltage ratings are suitable for such applications (V_{ds}*=20÷30V*, I_F*=20÷40A*), having capacitive properties much different each other. Normally, the devices are roughly judged based on the numeric value of gate charge at certain voltage and current reference conditions (also changing from device to device) provided in the datasheets. MOSFETs switching losses depend, instead, on how the capacitances change with the drain-to-source voltage and a reliable analysis of MOSFETs dissipation bent must necessarily rely on mathematical models including such property. This is especially important to predict the impact of PCB stray inductances, to correctly size by-pass capacitors and also to verify the realization of

soft-switching in those applications, such as Forward Active Clamp, where the MOSFETs capacitances are part of the resonant ring ensuring the soft-switching [19]-[21]. The impact of SRSC MOSFETs capacitive currents circulating through the converter is important in terms of EMI. The voltage source appearing in the generalized configuration of the SRSC shown in Figure 4.1 represents, in the various possible converters topologies, either the input voltage (e.g. buck converter) or the output voltage (e.g. boost converter) or the difference between them (e.g. buck-boost converter). Depending on the converter topology, the currents needed to charge and discharge the output MOSFETs capacitances respectively during turn-off and turn-on commutations will circulate through input rail, output rail or both. In order to prevent undesired EMI effects of such currents in the input and output rails, by-pass capacitors need to be properly sized and tightly connected across the extreme terminals of the SRSC to sink the spike MOSFETs capacitive currents, whose peak amplitude and duration depends on how the MOSFETs capacitances change during the commutations.

The goal of this investigation is to discuss a numerical model specifically developed to allow investigations of the dissipation bent properties of low-voltage high-current power MOSFETs and of the effects of their capacitive currents in the converters during commutations, by means of a novel unified model allowing the dynamic analysis of couples of MOSFETs in SRSC configuration.

The proposed model allows the analysis of the two MOSFETs of the SRSC by means of a unified system of non linear differential equations including the dependence of inter-electrode capacitances on time-varying inter-electrode voltages. The aim of the model is to provide a versatile trade-off tool for quick investigation during the design of power converters, which can be used with different analytical models of MOSFETs capacitances. The application of the model presented in this chapter is based on the use of MOSFETs dynamic capacitances curves available in manufacturers datasheets, for which an exponential fitting is adopted to describe the non linearity of MOSFETs capacitances with respect to the drain-to-source voltage. Nevertheless, the model can be extended to more detailed capacitance models, like the ones discussed in [13][14], if the parameters are available. A robust numerical technique has been

developed to solve the SRSC model including the capacitance formulas, which requires minimum settings to achieve reliable and sustainable simulations.

4.2 MOSFET SRSC commutations analysis

The dynamic analysis of couples of MOSFETs in SRSC configuration can be obtained by referring to the circuit model of Figure 4.2. The analysis of MOSFETs losses in SRSC is usually done by considering the two devices separately and using some simplified formulas to take into account the effect of reverse recovery of low-side body diode on the high-side MOSFET channel current and the losses associated to the output capacitance charge and discharge (in Appendix *A* simplified models overview for MOSFETs switching losses analysis is given).

The model of Figure 4.2, instead, allow a deep and complete analysis of how the capacitive currents circulate through the two devices, at the level of detail allowed by the available capacitance model. Stray inductances and parasitic PCB inductances do affect the behavior of MOSFETs during the commutation, as discussed in [17][18]. The devices pin wires inductances are provided only in some datasheets, while PCB ones can be determined only after that the part list of the power converter is complete and the layout is routed.

The model discussed in this dissertation can be used both with and without all these inductances. In the first part of the discussion of the model, the simplified schematic of Figure 4.2, which does not include parasitic inductances, will be adopted, to stress the main effects of MOSFETs capacitances. The additional equations needed for complete analysis including inductances are discussed at the end of this section and will be used in the comparison among simulation results and experimental measurements presented in section 4.5 of this chapter.

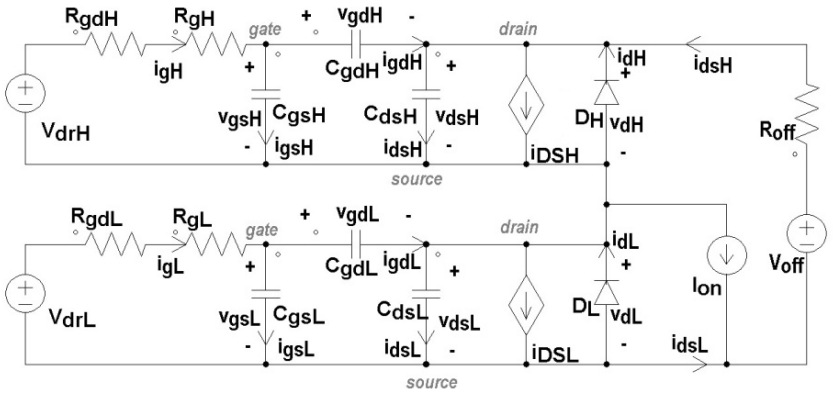


Figure 4.2 Circuit model: case study.

Loops and nodes Kirchhoff's equations (1) of the circuit of Figure 4.2 are:

$$\begin{cases} v_{gdL} = v_{gsL} - v_{dsL} \\ v_{gdH} = v_{gsH} - v_{dsH} \\ R_{gL} i_{gL} = V_{drL} - v_{gsL} \\ R_{gH} i_{gH} = V_{drH} - v_{gsH} \\ R_{off} i_{off} = V_{off} - v_{dsH} - v_{dsL} \\ I_{on} = i_{dsH} - i_{dsL} \\ i_{gL} = i_{CgsL} + i_{CgdL} \\ i_{gH} = i_{CgsH} + i_{CgdH} \\ i_{dsL} = I_{DSL} + i_{CdsL} - i_{CgdL} - i_{dL} \\ i_{dsH} = i_{off} = i_{DSH} + i_{CdsH} - i_{CgdH} - i_{dH} \end{cases} \tag{1}$$

where $R_{gx}=R_{gdx}+R_{gix}$ ($x=H,L$). The characteristic equations of MOSFET body diode and channel currents are:

$$i_{dx} = I_{\mu x}(e^{\frac{-v_{dsx}}{V_{Tx}}} - 1) \tag{2}$$

$$i_{DSx} = \begin{cases} \begin{array}{c} interdiction\ region: \\ v_{gsx} < V_{thx} \\ 0 \end{array} \\ \begin{array}{c} saturation\ region: \\ v_{gsx} > V_{thx}, |v_{dsx}| > v_{gsx} - V_{thx} \\ \frac{\beta_x}{2}(v_{gsx} - V_{thx})^2(1 + \lambda_x |v_{dsx}|)s_{Vdsx} \end{array} \\ \begin{array}{c} ohmic\ region: \\ v_{gsx} > V_{thx}, |v_{dsx}| < v_{gsx} - V_{thx} \\ \frac{\beta_x}{2}|v_{dsx}|\left[2(v_{gsx} - V_{thx}) - |v_{dsx}|\right](1 + \lambda_x |v_{dsx}|)s_{Vdsx} \end{array} \end{cases} \tag{3}$$

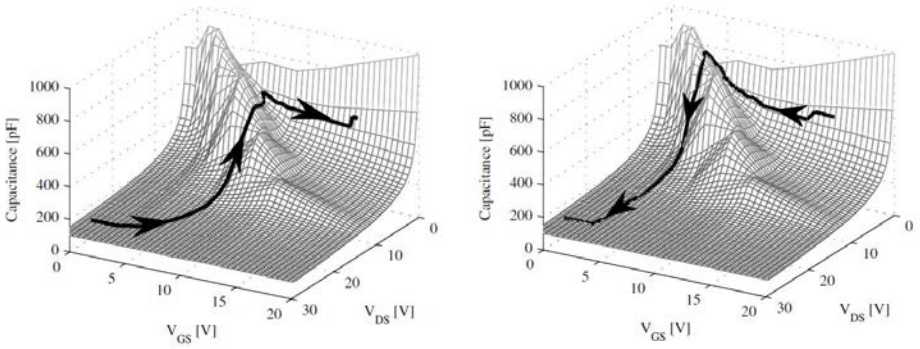
where $x=H,L$. The MOSFETs characteristic parameters V_{thx}, λ_x and β_x can be extracted from datasheets. The factor $sV_{dsx} = \{1,-1\}$ is used in equations (3) to take into account that the polarity of drain-to-source MOSFET channel current i_{DSx} is the same of the drain-to-source voltage v_{dsx}, whereas its magnitude depend on the absolute value of the voltage v_{dsx}. The elements determining MOSFETs losses in the circuit model of Figure 4.2 are the internal gate resistances R_{gix}, the controlled sources representing channel currents i_{DSx} and the body-diodes. Given any commutation occurring across a time interval $[0, t_{sw}]$, the total average commutation losses of each MOSFET are given by equation (4):

$$P_{sw} = f_s\left[R_{gix}\int_0^{t_{sw}} i_{gx}^2(t)dt + \int_0^{t_{sw}} v_{dsx}(t)i_{lossx}(t)dt\right] \tag{4}$$

where the total dissipative drain-to-source MOSFET current is $i_{lossx}=i_{DSx}-i_{dx}$. If the time-domain waveforms $v_{dsx}(t)$, $i_{lossx}(t)$ and $i_{gx}(t)$

are known over the switching time interval [*0*, t_{sw}], it is not necessary to subdivide MOSFET losses in many separate contributions associated to single parts and over multiple sub-intervals, nor it is necessary to separate the losses into additive contributions each one associated to a single part of the device as if it was a separate device. In (4), indeed, all the effects of MOSFET capacitances, which quickly charge and discharge during commutations and condition the $v_{dsx}(t)$, i_{lossx} (*t*) and $i_{gx}(t)$ waveforms, are included.

The real capacitances C_{gsx}, C_{gdx} and C_{dsx} are non linear functions of the gate-to-source and drain-to-source voltages [10]-[14]. Impedance measurements can help in the characterization of theses capacitances as function of both gate-to-source and drain-to-source voltage. In particular, in [12] *3D* graphs showing the evolution of the gate-drain capacitance C_{gd} during the switching commutations have been obtained: the capacitance operating points during the turn-on and turn-off event are marked as a line, respectively in Figure 4.3(a) and 4.3(b).



(a) **(b)**

Figure 4.3 Capacitance C_{gd} during the switching commutations: during the turn-on (a) and turn-off (b) event.

Nevertheless, as pointed out in the previous section, in power supply design the most convenient power devices have to be selected, by quickly identifying the commercial parts ensuring the best compliance with efficiency *vs* cost *vs* power density trade-off objectives. In such a task, the basic data provided by manufacturer in the device datasheets are the unique resource designers can use for rapid device selection.

Moreover, *information coming from datasheets is often insufficient for people who want to realize an accurate model of tested components* […], because *datasheets don't provide geometrical or "physics of semiconductor" parameters (like cell shapes and doping levels…) in order to derive accurate models* [13][14].

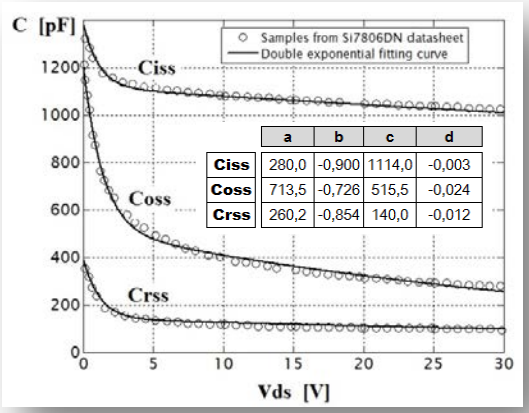
The values of the capacitances C_{gsx}, C_{gdx} and C_{dsx} are tabled only for specific v_{ds} and v_{gs} operating conditions [22][23]. However, they can be obtained from the capacitances C_{issx}, C_{rssx} and C_{ossx} according to equations (5):

$$\begin{aligned} C_{gsx} &= C_{issx} - C_{rssx} \\ C_{gdx} &= C_{rssx} \\ C_{dsx} &= C_{ossx} - C_{rssx} \end{aligned} \tag{5}$$

The plots of C_{issx}, C_{rssx} and C_{ossx} as functions of $|V_{dsx}|$ are the most detailed information provided by the MOSFETs manufacturers regarding the capacitances dependence upon the operating conditions. Figure 4.4 shows the C_{issx}, C_{rssx} and C_{ossx} sampled data for Vishay Si7806DN MOSFET [24]. The curves of Figure 4.4 can be approximated as a linear combination of two exponential terms, as shown in (6):

$$\begin{aligned} C_{issx} &= a_{ix}e^{b_{ix}|v_{dsx}|} + c_{ix}e^{d_{ix}|v_{dsx}|} = e_{aix} + e_{cix} \\ C_{ossx} &= a_{ox}e^{b_{ox}|v_{dsx}|} + c_{ox}e^{d_{ox}|v_{dsx}|} = e_{aox} + e_{cox} \\ C_{rssx} &= a_{rx}e^{b_{rx}|v_{dsx}|} + c_{rx}e^{d_{rx}|v_{dsx}|} = e_{aox} + e_{cox} \end{aligned} \tag{6}$$

where the coefficients $a_{yx}>0$, $b_{yx}<0$, $c_{yx}>0$, $d_{xy}<0$, for $y=i,o,r$ and $x=L,H$ can be determined by means of MATLAB® curve fitting tool. The first exponential term in (6) fits the plots in the low-voltage range (e.g. $v_{ds}<5V$ in Figure 4.4), where the plots show the highest rate of change, whereas the second exponential fits the plots in the high-voltage range (e.g. $v_{ds}>5V$ in Figure 4.4). Results of MATLAB® curve fitting for *a*, *b*, *c* and *d* of (6) are also shown in Figure 4.4.



	a	b	c	d
Ciss	280,0	-0,900	1114,0	-0,003
Coss	713,5	-0,726	515,5	-0,024
Crss	260,2	-0,854	140,0	-0,012

Figure 4.4 Si7806DN electrode capacitances.

The capacitances C_{gsx} and C_{gdx} are functions of v_{dsx}, which is not the voltage across their terminals: thus, they are treated as linear and controlled. The capacitance C_{dsx}, instead, depends on the voltage across its own terminals, and therefore it is treated as non-linear and non-controlled [25]. Consequently, we have:

$$\begin{aligned} i_{Cgsx} &= \frac{dQ_{gsx}(t)}{dt} = \\ &= \frac{dC_{gsx}\left(\left|v_{dsx}(t)\right|\right)}{d\left|v_{dsx}(t)\right|} s_{Vdsx} v_{gsx}(t) \frac{dv_{dsx}(t)}{dt} + C_{gsx}\left(\left|v_{dsx}(t)\right|\right) \frac{dv_{gsx}(t)}{dt} = \\ &= \delta_{gsx} \frac{dv_{dsx}(t)}{dt} + \gamma_{gsx} \frac{dv_{gsx}(t)}{dt} \end{aligned} \tag{7}$$

$$\begin{aligned} i_{Cgdx} &= \frac{dQ_{gdx}(t)}{dt} = \frac{dC_{gdx}\left(\left|v_{dsx}(t)\right|\right) v_{gdx}(t)}{dt} = \\ &= \frac{dC_{gdx}\left(\left|v_{dsx}(t)\right|\right)}{d\left|v_{dsx}(t)\right|} \frac{dv_{dsx}(t)}{dt} s_{Vdsx}\left[v_{gsx}(t) - v_{dsx}(t)\right] + \\ &\qquad + C_{gdx}\left(\left|v_{dsx}(t)\right|\right)\left[\frac{dv_{gsx}(t)}{dt} - \frac{dv_{dsx}(t)}{dt}\right] = \\ &= \delta_{gdx} \frac{dv_{dsx}(t)}{dt} + \gamma_{gdx} \frac{dv_{gsx}(t)}{dt} \end{aligned} \tag{8}$$

$$i_{Cdsx} = \frac{dQ_{dsx}(t)}{dt} = C_{dsx}\left(\left|v_{dsx}(t)\right|\right)\frac{dv_{dsx}(t)}{dt} = \delta_{dsx}\frac{dv_{dsx}(t)}{dt} + \gamma_{dsx}\frac{dv_{gsx}(t)}{dt} \tag{9}$$

where:

$$\begin{aligned}
\delta_{gsx} &= \left[b_{ix}e_{aix} + d_{ix}e_{cix} - b_{rx}e_{arx} - d_{rx}e_{crx}\right]s_{Vdsx}v_{gsx} \\
\delta_{gdx} &= \left[s_{Vdsx}v_{gdx}b_{rx} - 1\right]e_{arx} + \left[s_{Vdsx}v_{gdx}d_{rx} - 1\right]e_{crx} \\
\delta_{dsx} &= e_{aox} + e_{cox} - e_{arx} - e_{crx} \\
\gamma_{gsx} &= e_{aix} + e_{cix} - e_{arx} - e_{crx} \\
\gamma_{gdx} &= e_{arx} + e_{crx} \\
\gamma_{dsx} &= 0
\end{aligned} \tag{10}$$

Merging equations (7)-(9) with (1) yields the system of non linear state-space differential equations (11):

$$\begin{aligned}
\frac{dv_{gsH}}{dt} &= \dot{v}_{gsH} = +\Lambda_H\left[\delta_{dgH}i_{gH} + \delta_{ggH}\left(i_{DSH} - i_{dH} - i_{dsH}\right)\right] \\
\frac{dv_{dsH}}{dt} &= \dot{v}_{dsH} = -\Lambda_H\left[\gamma_{dgH}i_{gH} + \gamma_{ggH}\left(i_{DSH} - i_{dH} - i_{dsH}\right)\right] \\
\frac{dv_{gsL}}{dt} &= \dot{v}_{gsL} = +\Lambda_L\left[\delta_{dgL}i_{gL} + \delta_{ggL}\left(i_{DSL} - i_{dL} - i_{dsH} + I_{on}\right)\right] \\
\frac{dv_{dsL}}{dt} &= \dot{v}_{dsL} = -\Lambda_L\left[\gamma_{dgL}i_{gL} + \gamma_{ggL}\left(i_{DSL} - i_{dL} - i_{dsH} + I_{on}\right)\right]
\end{aligned} \tag{11.a}$$

where:

$$\begin{aligned}
&\delta_{ggx} = \delta_{gsx} + \delta_{gdx}, \quad \delta_{dgx} = \delta_{dsx} - \delta_{gdx} \\
&\gamma_{ggx} = \gamma_{gsx} + \gamma_{gdx}, \quad \gamma_{dgx} = \gamma_{dsx} - \gamma_{gdx} \\
&\Lambda_x = \left[\delta_{dgx}\gamma_{ggx} - \delta_{ggx}\gamma_{dgx}\right]^{-1}
\end{aligned} \tag{11.b}$$

It should be noted that the structure of equations (11) does not change if a different model of the inter-electrode capacitances is adopted. In fact, if, for example, the parameters of model [13][14] are available, then the corresponding functions of capacitances $C_{gsx}(v_{gsx},v_{dsx})$, $C_{gdx}(v_{gsx},v_{dsx})$ and $C_{dsx}(v_{gsx},v_{dsx})$ can be used to generate the coefficients (10), which will just assume a different explicit form.

The non linear differential equations (11) do not allow an analytical resolution. They can only be solved by means of numerical techniques [26]. Most of the classical numerical methods for solving *Ordinary Differential Equations* (*ODE*) solution are for non-stiff equations only. These methods include the simplest Euler method, the most widely used fourth-order Runge-Kutta method and the multi-step Adams method (predictor-corrector method). A detailed description can be found in [26] and other textbooks on the topic. Euler and Runge-Kutta methods are one-step methods in that they refer only to one previous value to determine the current value. Adams' method, which refers to several previous values, is quite different, but this method may potentially incur few function calls. Most of numerical methods for ODE solving can become unbearably slow when the ODEs are stiff. Unfortunately, ODEs are stiff in many cases of practical interest.

Equations (11) are quite stiff indeed. In this cases it is very important to use an ODE solver that solves stiff equations efficiently also thanks to adequate tolerance setting. Solvers for stiff equations usually require to evaluate the Jacobian, which can be very expensive. Sophisticated solvers usually automatically switch between stiff and non-stiff methods to achieve good performance in both cases. These methods include for example the implicit Runge-Kutta methods, the Rosenbrock method or the Gear methods (also called as Backward Differentiation Formulae, BDF). Rosenbrock method is relatively simple to implement, but its performance is quickly degraded when we require higher precision. The BDF instead is a multi-step method and it is probably the most widely used method for stiff equations. Explicit methods, like forward Euler, need a very small time step to prevent numerical instability and to guarantee the simulation convergence in the solution of stiff equations, but very small time step may lead to very long computations. In this work, the ODE15s has been adopted as a reference solver to test the accuracy of the novel Euler-based technique discussed in the next Section, specifically developed to deal with system (11).

The basic system (11) can be adopted for the analysis of the inherent behavior of MOSFETs during commutations, as it would be in case of negligible effects of PCB and MOSFTs parasitic inductances. The effects of parasitic inductances as in the gate loops as in the output

loop is easily included, to enabling the EMI analysis of current ringing through LSM and HSM and external loops. In particular, the additional equations (12) can be merged with equations (11) for the analysis:

$$\begin{aligned}
\frac{di_{dsH}}{dt} &= \frac{1}{L_{off}}\left[V_{off} - v_{dsH} - v_{dsL} - i_{dsH}R_{off}\right] \\
\frac{di_{gH}}{dt} &= \frac{1}{L_{gH}}\left[V_{drH} - R_{gH}i_{gH} - v_{gsH}\right] \\
\frac{di_{gL}}{dt} &= \frac{1}{L_{gL}}\left[V_{drL} - R_{gL}i_{gL} - v_{gsL}\right]
\end{aligned} \tag{12}$$

Thus, the user can decide which model to use, depending on the need.

4.3 MOSFETs SRSC commutations analysis with MFE method

One main issue in using ODE solvers and circuit simulators based on implicit methods for stiff problems is that a preliminary analysis of the problem to be solved is needed in order to define the proper tolerance for calculations. Wrong tolerance values may lead to unsustainably long computations or to convergence failures. The search for the right tolerance and for the right stiff ODEs solver may cause a dramatic increase of the time-to-solution. For this reason, in order to preserve simplicity and computational effectiveness in the solution of model (11)(12), a modified version of the basic forward Euler method (13):

$$\begin{aligned}
v_{gsx}(t_{k+1}) &= v_{gsx}(t_k) + \dot{v}_{gsx}(t_k)\Delta t_k \\
v_{dsx}(t_{k+1}) &= v_{dsx}(t_k) + \dot{v}_{dsx}(t_k)\Delta t_k \qquad k = 1, 2, \ldots
\end{aligned} \tag{13}$$

has been adopted, which implements a special technique for the generation of the adaptive time step $\Delta t_k = t_{k+1} - t_k$. Adaptive time step, indeed, is normally adopted for efficient and reliable numerical solution of ODE. Many techniques can be used, which offer different levels of computational efficiency depending on the problem to be solved and to the type of ODE solver. The solution proposed in this

chapter consists in using an adaptive time step method specifically developed for the problem under investigation to guarantee stability and convergence of forward Euler method (13). The idea is to exploit the well defined structure of the entire system of non linear equations (2),(3),(5),(6),(10),(11),(12) to be solved, considering that the error in the numerical solution depends on the local rate of change of the variables.

Equations (11)(12) show that the elements mainly influencing the variability of the rates of changes of the state variables v_{dsx} and v_{gsx} are the MOSFETs capacitances, through the δ and γ coefficients of system (11), and the channel, gate and body diode current currents (the current I_{on} is fixed and the current $i_{dsH}=i_{off}$ linearly depends on v_{dsH} and v_{dsL}). These influencing factors are strongly dependent on the state variables v_{dsx} and v_{gsx}. Therefore, it is reasonable to operate a control of the rate of change of MOSFETs capacitances, channel currents and body diode currents to locally adapt the time step size. The rate of change of currents $i_{DSx}(t)$, $i_{dx}(t)$ and $i_{gsx}(t)$ during the commutations vary with the position of the Operating Point (*OP*) of the MOSFET from interdiction to saturation to linear region and vice-versa. While the MOSFET OP moves through the saturation region, the channel and body diode currents $i_{DSx}(t)$ and $i_{dx}(t)$ exhibit the major rate of change. While the MOSFET OP moves through either the interdiction or the linear region, $v_{gsx}(t)$ and $i_{gsx}(t)$ exhibit the major rate of change. The maximum rate of change of $i_{gsx}(t)$ during the commutations depends on the sign of the current I_{on}. In particular, if $I_{on}>0$, when the HSM turns off it releases its channel current to the LS body-diode and this one, in turn, releases the current to the turning on LSM channel; in dual manner, when the LSM turns off it releases its channel current to its own body-diode and this one, in turn, releases the current to the turning on HSM channel. In this case, the current $i_{gsH}(t)$ will mostly be an exponential function of the time, excepted during the Miller region, wherein it is almost flat; so that, there are only two steep fronts in its waveform, corresponding to the gate driver turn on and turn off. The current $i_{gsL}(t)$, instead, is a purely exponential function with two peaks corresponding to the gate driver turn on and turn off. The behavior of $i_{gsH}(t)$ and $i_{gsL}(t)$ is different when $I_{on}<0$: in this case, in fact, the HSM body diode will be exchanging the current with the two MOSFETs channels while LSM turns off and HSM turns on, whereas the LSM

body diode will be exchanging the current with the two MOSFETs channels while HSM turns off and LSM turns on. Therefore, both $i_{gsH}(t)$ and $i_{gsL}(t)$ will show a flat Miller region during the turn off of the relevant MOSFETs. For whatever kind of commutation, while the gate current $i_{gsx}(t)$ of a device goes through the flat Miller region, the gate current of the other device shows a bounce caused by the voltage rise/fall of the switching node.

Regarding the capacitances, their rate of change is high during the phases of the commutations involving quick changes of the voltage $v_{dsx}(t)$. This happens when:

- current is fast splitting from the MOSFET channel to a body-diode, and vice-versa: the MOSFET OP moves in this case through the linear region up to (or beyond) the boundary with the saturation region, the small negative voltage $v_{dsx}(t)$ is fast varying and consequently the capacitances are big and fast varying;
- voltage $v_{dsx}(t)$ is fast varying due to the charge (discharge) of MOSFET output capacitance, occurring before (after) that the current split between the MOSFET channel and a body diode starts (ends): the OPs of both MOSFETs move in this case through the saturation region, from low to high voltage or vice-versa depending on whether the device is turning off or on.

According to the previous discussion, the magnitude of Δt_k can be fixed step-by-step based on the highest rate of change among the currents and the capacitances. The maximum swings expected for the currents $i_{DSx}(t)$, $i_{dx}(t)$ and $i_{gsx}(t)$ during the commutations can be approximated by $\Delta I_{DSxmax}=2I_{on}$, $\Delta I_{dxmax}=I_{on}$ and $\Delta I_{gsxmax}=V_{drx}/R_{gx}$ respectively. The swing for the currents i_{DSx}(t) is expected to be twice than for the currents $i_{dx}(t)$ because of the effect of capacitive currents flowing through the MOSFETs channels. The maximum swing expected for each capacitance during the commutations can be approximated by its value at zero voltage $\Delta C_{max}=C_{yx}(0)$.

Let $\Delta I_{DSx}=\varepsilon_{IDSx}\Delta I_{DSxmax}$, $\Delta I_{dx}=\varepsilon_{Isx}\Delta I_{dxmax}$ and $\Delta I_{gsx}=\varepsilon_{Igsx}\Delta I_{gsxmax}$ be respectively the maximum allowed step variations for the currents $i_{DSx}(t)$, $i_{dx}(t)$ and $i_{gsx}(t)$, and let $\Delta C_{yx}=\varepsilon_{Cyx}\Delta C_{yxmax}$ be the maximum allowed step variation for the capacitance C_{yx}: then, a reference value

for the duration Δt_k of the time step starting at the sampling instant t_k is given by equation (14):

$$\Delta t_{k,ref} = \min_{\{x,y\}}\left[\frac{\Delta I_{DSx}}{|\dot{i}_{DSx}|_k},\frac{\Delta I_{dx}}{|\dot{i}_{dx}|_k},\frac{\Delta I_{gsx}}{|\dot{i}_{gsx}|_k},\frac{\Delta C_{yx}}{\left|\dot{v}_{dsx}\partial C_{yx}\right|_k}\right] \tag{14}$$

where $x=H, L$, $y=iss, oss, rss$, $\partial C_{yx}=dC_{yx}/d|v_{dsx}|$. Values for ε_{IDSx}, ε_{Idx}, ε_{Igsx} and ε_{Cyx} should reasonably fall in the range $[10^{-3},10^{-2}]$ to limit both the error and the computing time. From (2)(3)(6) we get:

$$\dot{i}_{DSx} = \begin{cases} \text{linear region: } v_{gsx} > V_{thx}, |v_{dsx}| < v_{gsx} - V_{thx} \\ \frac{\beta}{2}\left[2(v_{gs}-V_{th})(1+2\lambda|v_{ds}|)-|v_{ds}|(2+3\lambda|v_{ds}|)\right]\dot{v}_{ds} + \\ +\beta|v_{ds}|(1+\lambda|v_{ds}|)s_{Vds}\dot{v}_{gs} \\ \text{saturation region: } v_{gsx} > V_{thx}, |v_{dsx}| > v_{gsx} - V_{thx} \\ \beta(v_{gs}-V_{th})(1+\lambda|v_{ds}|)s_{Vds}\dot{v}_{gs} + \frac{\beta}{2}(v_{gs}-V_{th})^2\lambda\dot{v}_{ds} \\ \text{interdiction region: } v_{gsx} < V_{thx} \\ 0 \end{cases} \tag{15}$$

$$\dot{i}_{dx}(t) = -\left\{\left[i_{dx}(t) + I_{\mu x}\right]\Big/V_{Tx}\right\}\dot{v}_{dsx}(t) \tag{16}$$

$$\dot{i}_{gsx}(t) = -\dot{v}_{gsx}(t)\big/R_{gx} \tag{17}$$

$$\partial C_{yx} = b_{yx}e_{ayx} + d_{yx}e_{cyx} \tag{18}$$

If $\Delta t_{k,ref}=\Delta t_{k-1}$, then $\Delta t_k=\Delta t_{k,ref}$. In case $\Delta t_{k,ref} \neq \Delta t_{k-1}$, in order to avoid sudden changes in Δt_k from one step to the subsequent one, the value of Δt_k is obtained from the reference value $\Delta t_{k,ref}$ and from Δt_{k-1}, as shown in (19):

$$\Delta t_k = \frac{1}{2}\left\{\Delta t_{\max}\left[1+\frac{2}{\pi}\tan^{-1}\left(\frac{\alpha\left(\Delta t_{k,ref}-\Delta t_{k-1}\right)}{\min(\Delta t_{k,ref},\Delta t_{k-1})}\right)\right]+\Delta t_{k-1}\right\} \qquad (19)$$

Equation (19) yields increase of Δt_k with respect to Δt_{k-1} if the overall magnitude of derivatives in (14) decreases, and vice-versa. The upper limit of Δt_k given by (19) for $\Delta t_{k,ref} >> \Delta t_{k-1}$ is $\Delta t_k = \Delta t_{max} + 0.5\Delta t_{k-1}$, which saturates at $\Delta t_k = 2\Delta t_{max}$. The lower limit of Δt_k given by (19) for $\Delta t_{k,ref} << \Delta t_{k-1}$ is $\Delta t_k = 0.5\Delta t_{k-1}$, which saturates at $\Delta t_k = 0$. The joint use of (14) and (19) provides a smooth adaptation of time step Δt_k to the changing dynamic behavior of the MOSFETs during the commutations. The steepness factor α in (19) should be kept in the range [*0.1*,*0.5*] to ensure adequate smoothing of Δt_k variations from sample to sample. The value of Δt_{max} can be determined based on MOSFETs characteristics. In particular, Δt_{max} has to be settled by considering the phases of the commutation during which the maximum rate of change of state variables is slowest. This happens at the end of the exponential rise of the gate-to-source voltages $v_{gsx}(t)$ during the turn on of the devices. In these phase the drain-to-source voltage $v_{dsx}(t)$ is very low and the time constant $\tau_{iss} = C_{issx} R_{gx}$ of the gate circuit is maximum, due to the high value of the capacitance C_{issx}. Assuming that the turn on is almost complete when the voltage $v_{gsx}(t)$ equals the 99% of the gate driver voltage V_{drx}, it can be easily proved that over a time step $\Delta t = 10^{-4}\tau_{iss}$ the relative error involved by using linear approximation of the exponential rising waveform is about 10^{-4}.

Therefore the following setup can be adopted:

$$\Delta t_{\max} = 10^{-4} \min_{x=H,L}\left\{\tau_{issx}\right\} \qquad (20)$$

The adaptive time step forward Euler technique described above can be used to set-up a simple and portable simulation algorithm for MOSFETs SRSC commutations analysis as follows. The state of each MOSFET is identified with numbers *0, 1* or *2* if its OP falls within the interdiction, saturation or linear region respectively. Table 4.1 resumes the conditions for HSM and LSM state identification.

Table 4.1 Switch State truth table.

	$v_{gsx} < V_{thx}$	$v_{gsx} > V_{thx}$
$\|v_{dsx}\| > v_{gsx} - V_{thx}$	*0*	*1*
$\|v_{dsx}\| < v_{gsx} - V_{thx}$	*0*	*2*

Equations for MOSFET channel current and related derivative are given by (3)(15) for each state. Based on the previous outline, the synchronous HSM turn on and LSM turn off, and the synchronous HSM turn off of and LSM turn on, can be analyzed as summarized in the macro code sketch reported in Table 4.2.

The HS dead-time condition and LS dead-time condition in Table 4.2 depend on the kind of gate driver. Several proprietary adaptive dead time control techniques are adopted in switcher ICs. A typical implementation consists in fixing a built-in delay time t_{delay} (typically some tens of *ns*) between the detection of a threshold value (e.g. *1V*) at the gate-source terminals of the turning off device and the trigger of high level on the gate drive voltage of the turning on device. This type of dead-time control is referred to in [27], for example, for dead-time loss calculation. Both HS and LS gate charge termination have been assumed to be achieved when the gate-to-source voltage of MOSFETs reaches $99\%V_{dr}$. Based on the previous arrangements, the analysis of the MOSFETs SRSC commutations in a buck switching power converter for two case studies has been realized, as illustrated in next Section.

Table 4.2 Synchronous Commutations Analysis

HSM turn ON , LSM turn OFF analysis

FETs state before the commutation: *HSS=0, LSS=2.*

	v_g	i_{ds}	v_{ds}	v_{gs}
HS	*0*	*0*	V_{off}	*0*
LS	V_{drL}	I_{on}	$I_{on}R_{dsonL}$	V_{drL}

k=0, v_{gL}*=0, HSS=0,*

while *HS dead-time condition*

k=k+1

update $v_{gsx}(t_k)$ **and** $v_{dsx}(t_k)$ **[Eq. (11)(13)(14)]**

update *LSS* **[Table 4.1]**

end

$_{vgH}=V_{drH}$,

while *HS gate charge condition*

k=k+1

update $v_{gsx}(t_k)$ **and** $v_{dsx}(t_k)$ **[Eq. (11)(13)(14)]**

update *HSS* **and** *LSS* **[Table 4.1]**

end

HSM turn OFF , LSM turn ON analysis

FETs state before the commutation: *HSS=2, LSS=0.*

	v_g	i_{ds}	v_{ds}	v_{gs}
HS	V_{drH}	I_{on}	$I_{on}R_{dsonH}$	V_{drH}
LS	*0*	*0*	V_{off}	*0*

k=0, v_{gH}*=0, LSS=0,*

while *LS dead-time condition*

k=k+1

update $v_{gsx}(t_k)$ **and** $v_{dsx}(t_k)$ **[Eq. (11)(13)(14)]**

update *HSS* **[Table 4.1]**

end

$_{vgL}=V_{drL}$,

while *LS gate charge condition*

k=k+1

update $v_{gsx}(t_k)$ **and** $v_{dsx}(t_k)$ **[Eq. (11)(13)(14)]**

update *HSS* **and** *LSS* **[Table 4.1]**

end

4.4 Numerical simulation of SRSC commutations

The goal of the examples discussed in this section is manifold.

First, the robustness of the MFE method (13) using (14) and (19) in the solution of system (11)(12) based on the analytical approximations (6) is analyzed. To this purpose, the results obtained by solving system (11)(12) in MATLAB based on (13)(14)(19) are compared with the results obtained by using ODE15s and ODE 23s MATLAB routines [28] to solve the same system (11)(12) for different case studies.

Second, the importance of analyzing the two MOSFETs of the SRSC *together* is shown, in order to highlight the way capacitive currents circulate through the MOSFETs channels and through the external power circuit and their consequent effects on losses and noise.

Third, to highlight how the method discussed in this chapter allows to easily achieve more rigorous evaluation of losses, overcoming some trivial limitations of popular approximated formulas.

4.4.1 Case Study #1

The first example (case #1) is related to a buck converter case with the following operating parameters: $V_{in}=6V$, $V_{out}=1.2V$, $I_{out}=1.5A$, $\Delta i_{Lpp}=1A$, $f_s=1MHz$, $D=0.27$, $R_{dr,ON}=R_{dr,OFF}=2.5\Omega$. The Vishay Si7806DN [18] and the Vishay Si4620DY [23] with embedded Schottky diode have been considered as HSM and LSM, respectively. Data needed for set-up of equations (11)(12) have been extracted from the device datasheet. The built-in delay time t_{delay} of the adaptive dead-time control has been assumed to be *5ns*.

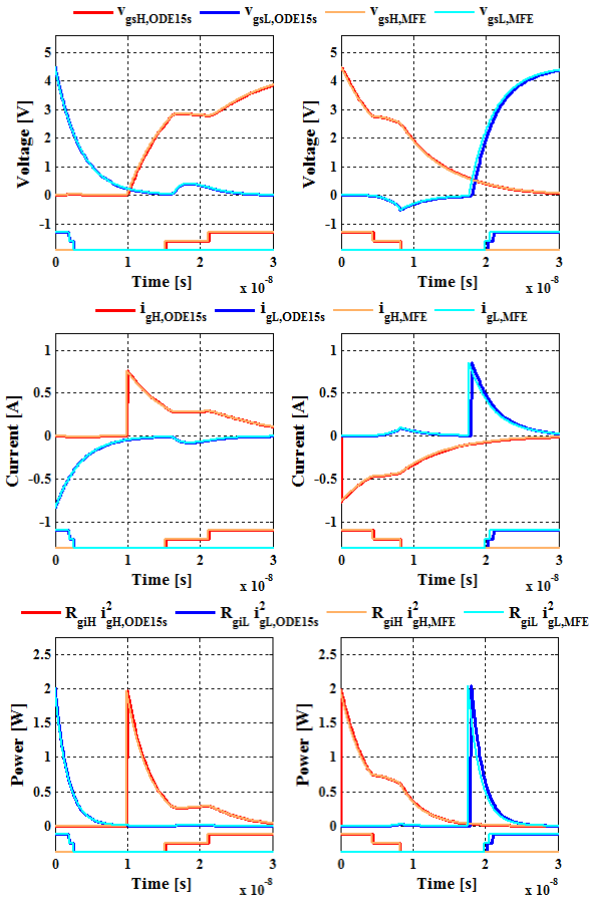
In Figure 4.5 the results obtained by solving system (11)(12) by means of MFE and of ODE15s MATLAB routines are compared. The MATLAB ODE15s routine has been set-up with *RelTol*=1e-6 and *AbsTol*=1e-6 [28]. These parameters have a heavy influence on the convergence and on the computing time in the solution of stiff systems like (11)(12). Their adequate setting is neither easy nor straightforward. Several attempts are needed before the right setup is

achieved and a good setup for a couple of MOSFETs can be bad for a different couple, as shown in the following examples. This makes the use of ODEs not so simple.

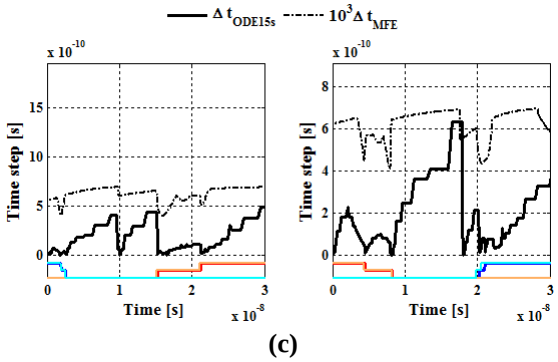
The MFE method discussed in this dissertation, instead, is based on automatic setup of time step based on (14)(19)(20) for whatever MOSFETs couple.

The voltage and current waveforms of Figure 4.5(a)(b) show a very good agreement for MFE and ODE15s. In the bottom part of each plot of Figure 4.5 the state time diagram (*0*,*1*,*2*) of both MOSFETs is reported (red/orange line = HSM, blue/cyan line = LSM). The Miller plateau is well evident in HSM gate-to-source voltage and current (red/orange curves) of Figure 4.4.

The plots of Figure 4.5(c) show the ODE and MFE time steps during the simulation. MFE globally works with a time step Δt much smaller than ODE15s. In this example, the ODE15s is much faster (about *50* times) than MFE in the pure run of the simulation: however, a time much longer than the one required by MFE run of the simulation has been spent to find an adequate setup of ODE15s tolerances.



(a)



(c)

Figure 4.5 MFE and ODE15s results for case #1: (a) HSM and LSM gate-to-source voltages (top), currents (middle) and gate power dissipation (bottom); (c) ODE and MFE time steps during simulations.

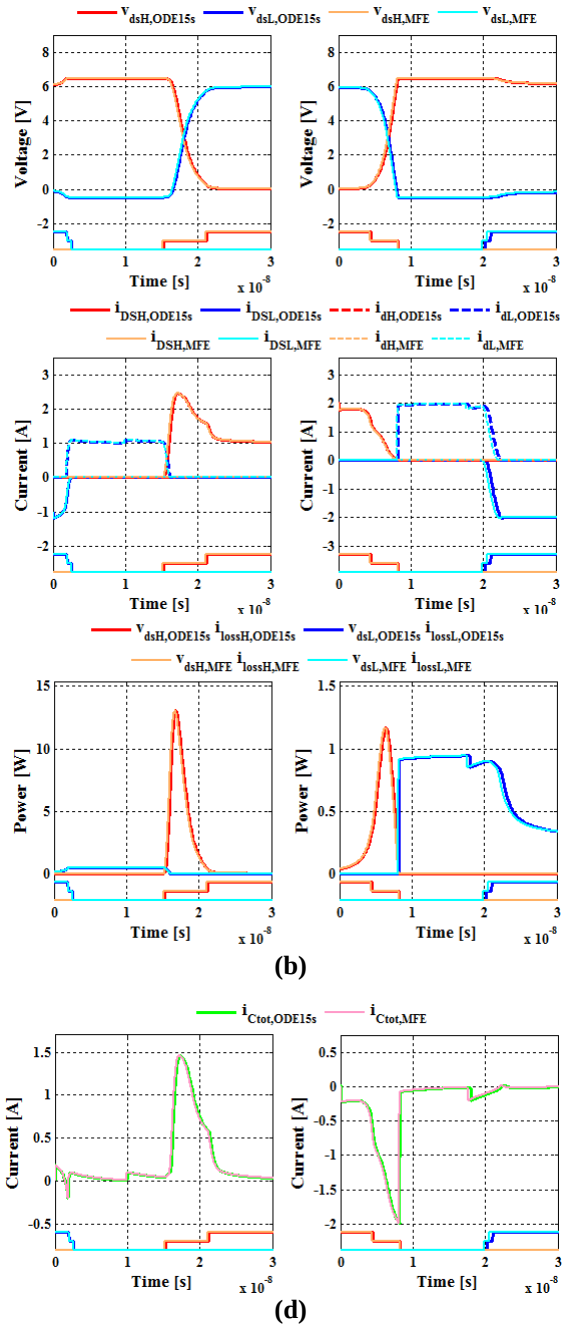


Figure 4.5 (Cont.) MFE and ODE15s results for case #1: (b) HSM and LSM drain-to-source voltages (top), channel and diode currents (middle) and channel and diode power dissipation (bottom); (d) total capacitive current flowing through HSM channel.

4.4.2 Case Study #2

The second example (case #2) is related to a buck converter with the following operating parameters: V_{in}*=3.3V*, V_{out}*=1.2V*, I_{out}*=10A*, Δi_{Lpp}*=3A*, f_s*=500kHz*, *D=0.43*, $R_{dr,ON}$*=3*Ω, $R_{dr,OFF}$*=2*Ω, t_{delay}*=5ns*. The Dual N-channel Vishay SiZ790DT with embedded Schottky diode in parallel to LSM has been considered for the given application. Data needed for set-up of equations (11)(12) have been extracted from the device datasheet [30].

In this example the ODE15s with the same tolerances adopted for previous example do not converge to correct results. Even reducing the tolerances setup does not provide acceptable solutions. Therefore, the MATLAB ODE23s have been adopted for this second example. In Figure 4.5 the results obtained by means of MFE and of ODE23s are compared. The ODE23s tolerance set-up *RelTol*=1e-15 and *AbsTol*=1e-6 have been found to be suited to the case, as a result of a rather time consuming investigation. Instead, like in the previous example, no time is spent for MFE tolerance setup, as it is automatically achieved by means of (14)(19)(20).

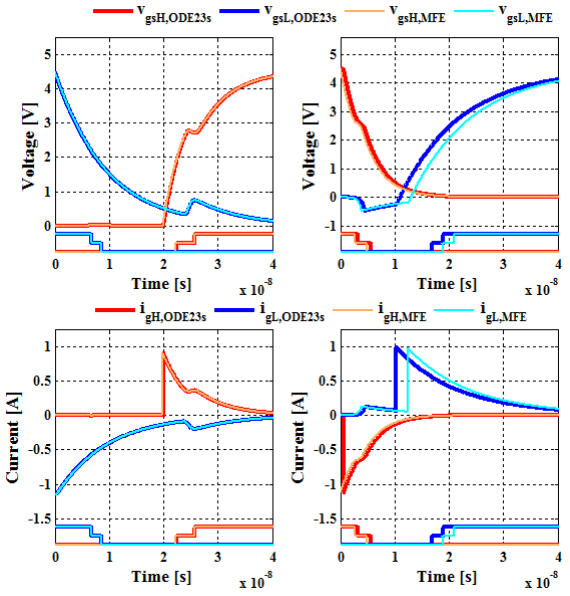
The voltage and current waveforms of Figure 4.6(a)(b) show quite good agreement between MFE and ODE23s during the first commutation. Instead, the agreement is not good for the second commutation (see right side plots of Figures 4.6(a)(b)). Adopting *AbsTol*=1e-7 for ODE23s yields the results shown in plots of Figures 4.6(c)(d). This highlights that the MFE results are correct, as the ODE23s approach the same results of MFE if the *AbsTol* setting is decreased. Indeed, if ODE23s *AbsTol* is too big, the exact instants of dead-time termination condition are missed. Decreasing *AbsTol* from 1e-6 to 1e-7 causes a big increase of ODE23s simulation time: accordingly, the ratio between the MFE and the ODE simulation times can decrease from about *20* to *2* (depending on the microprocessor power and on *AbsTol* setting, ODE simulation times can go from much less than *1* minute to few minutes).

The appropriate trade-off value of ODE *AbsTol* to achieve correct simulation in a short time is not predictable. Several trials may be needed before an acceptable solution is found. As a consequence, MFE simulation times are much shorter.

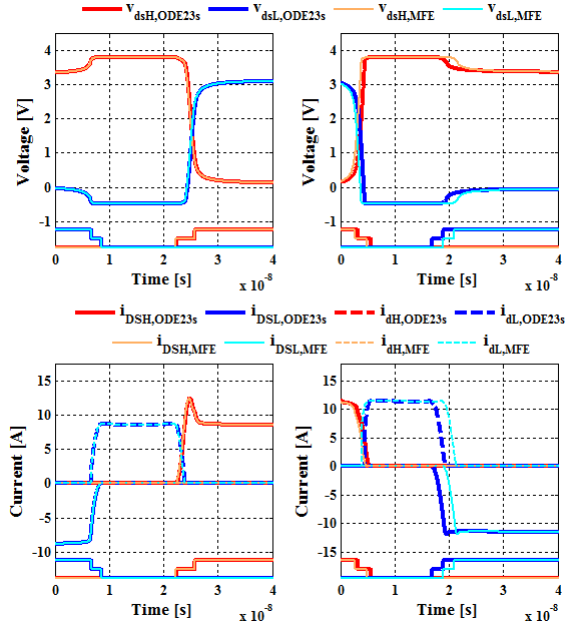
Case #1 and case #2 show that the MFE method based on (14)(19)(20) ensure higher reliability and lower net elaboration time than ODEs. Let now examine some characteristics of the waveforms obtained with the simulations, which are important for losses and circulating currents analysis, and the effect of charging/discharging gate-to-source and gate-to-drain capacitances of both MOSFETS during the commutation.

The overshoot in HSM channel current (see Figures 4.5(b) and 4.6(d)) is composed by I_{on} plus the bumps appearing in i_{CdsH}, i_{CgdH}, i_{CdsL} and i_{CgdL} currents, shown in Figures 4.7(a)(c)(e) for case #2, which are the effect of fast varying v_{dsH} and v_{dsL} voltages and of fast varying C_{dsH}, C_{gdH}, C_{dsL} and C_{gdL} capacitances (see Figures 6(b)(d)(f)).The plots point out that *both* the *discharging* current of output capacitance of HSM and the *charging* current of the output capacitance of LSM pass through the HSM channel, in both commutations. No capacitive current passes through the LSM channel in commutations occurring at heavy load. So that, the total capacitive current $i_{Ctot}=-i_{CdsH}+i_{CgdH}+i_{CdsL}-i_{CgdL}$ shown in Figure 4.7(l) must be taken into account during HSM turn ON and turn OFF. The net effect of the capacitive currents of Figure 4.7(l) on HSM switching losses depends on the magnitude of the inductor current ripple.

The capacitive currents flowing through the HSM channel from drain to source are positive during the turn on and negative during the turn off: therefore, the HSM channel current is higher than I_{on} at turn on and lower at turn off. The plots of Figures 4.5(b) and 4.7(h) show that, as a consequence of such current unbalance, the channel power loss at HSM turn off is much lower than at the turn on. Due to the inductor current ripple, when the HSM turns off it is $I_{on}=I_{out}+0.5\Delta i_{Lpp}$, whereas when the HSM turns on it is $I_{on}=I_{out}-0.5\Delta i_{Lpp}$.

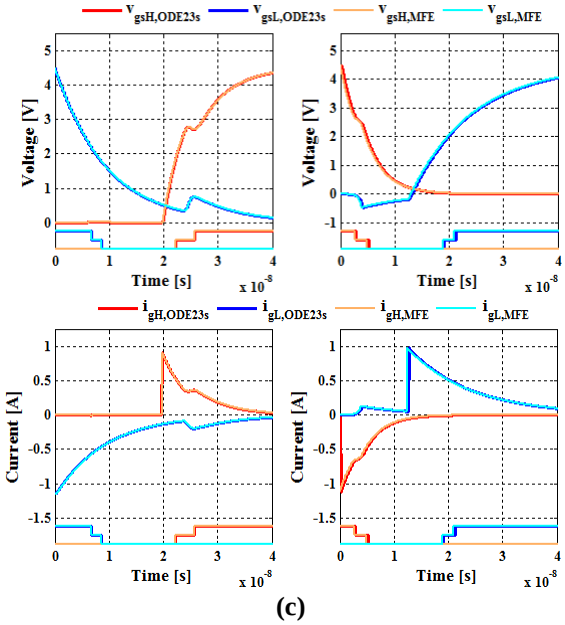


(a)

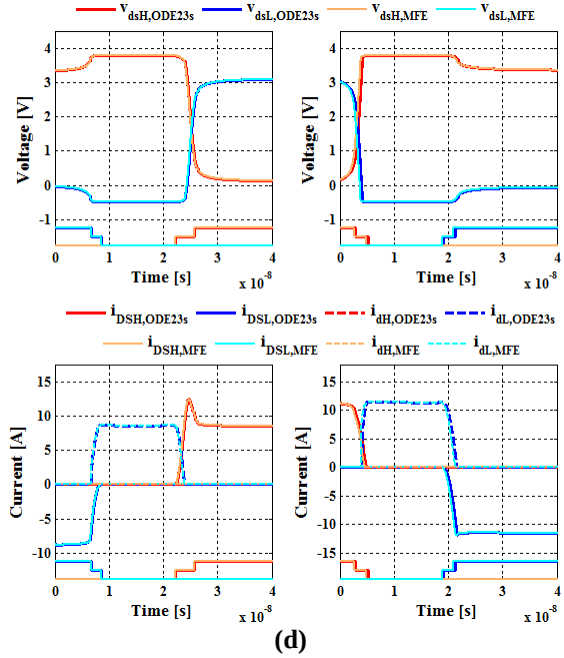


(b)

Figure 4.6 MFE and ODE23s results for case #2: (a) HSM and LSM gate-to-source voltages (top) and currents (bottom) with ODE23s AbsTol=1e-6; (b) HSM and LSM drain-to-source voltages (top), channel and diode currents (bottom) with ODE23s AbsTol =1e-6.

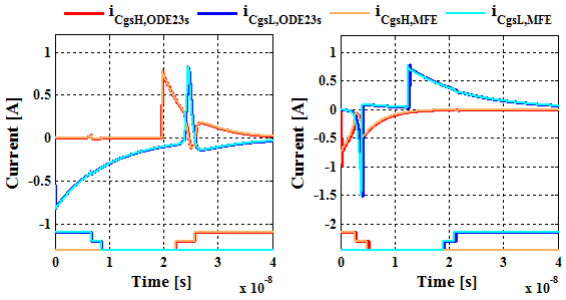


(c)

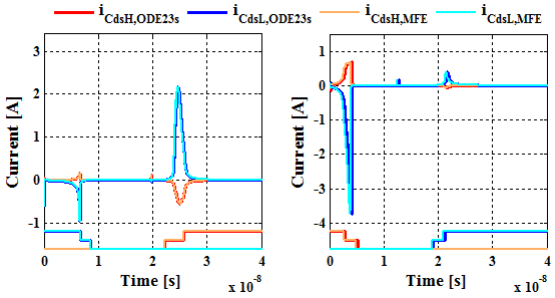


(d)

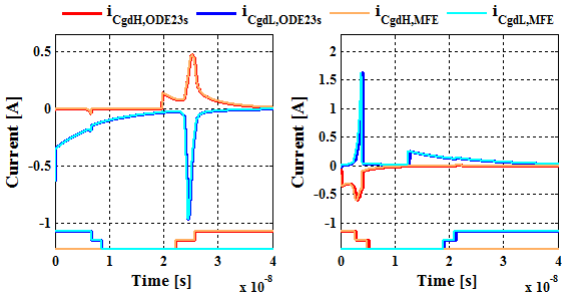
Figure 4.6 (Cont.) MFE and ODE23s results for case #2: (c) HSM and LSM gate-to-source voltages (top) and currents (bottom) with ODE23s AbsTol =1e-7; (d) HSM and LSM drain-to-source voltages (top), channel and diode currents (bottom) with ODE23s AbsTol =1e-7.



(a)

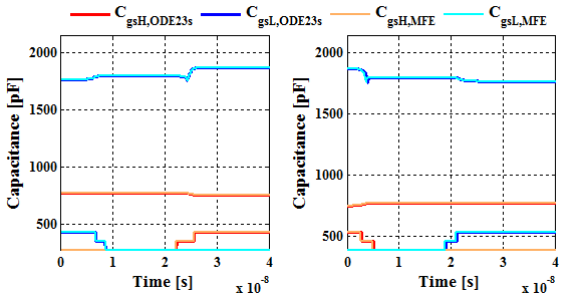


(c)

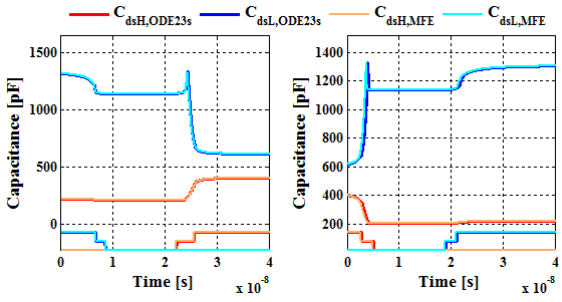


(e)

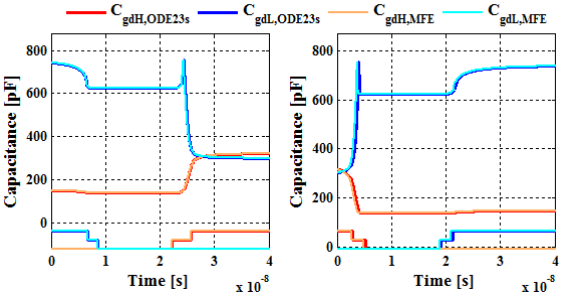
Figure 4.7 MFE and ODE23s with AbsTol=1e-7 results for case #2: (a)(c)(e) HSM and LSM capacitive currents.



(b)

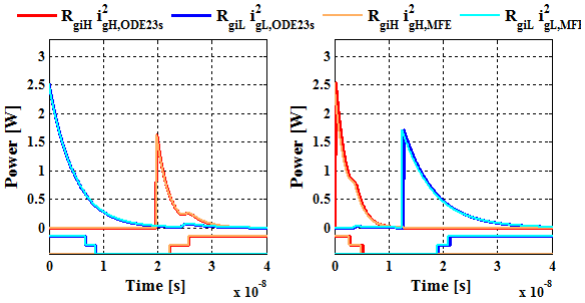


(d)

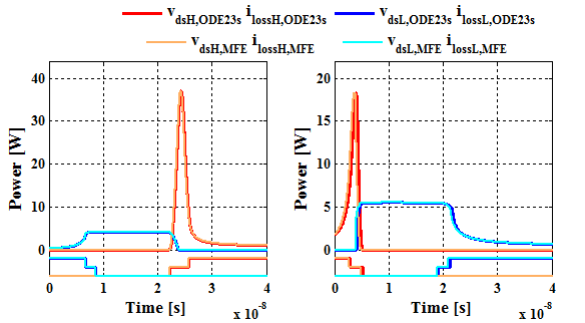


(f)

Figure 4.7 (Cont.) MFE and ODE23s with AbsTol=1e-7 results for case #2: (b)(d)(f) HSM and LSM capacitances.



(g)



(h)

Figure 4.7 (Cont.) MFE and ODE23s with AbsTol=1e-7 results for case #2: (g) HSM and LSM gate power loss; (h) HSM and LSM channel and diode power loss.

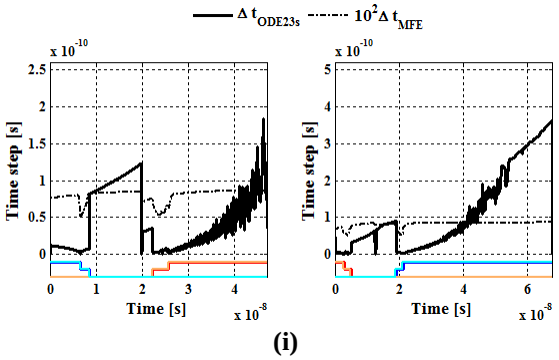


Figure 4.7 (Cont.) MFE and ODE23s with AbsTol=1e-7 results for case #2: (i) ODE23s and MFE time steps during simulations; (l) total capacitive currents flowing through HSM channel during commutations.

4.4.3 Case Study #3

Such difference may magnify the decrease of the HSM channel power loss at turn off and, depending of the ripple amplitude, the net result might be as a positive as a negative balance between HSM channel loss increase at the turn on and loss decrease at the turn off.

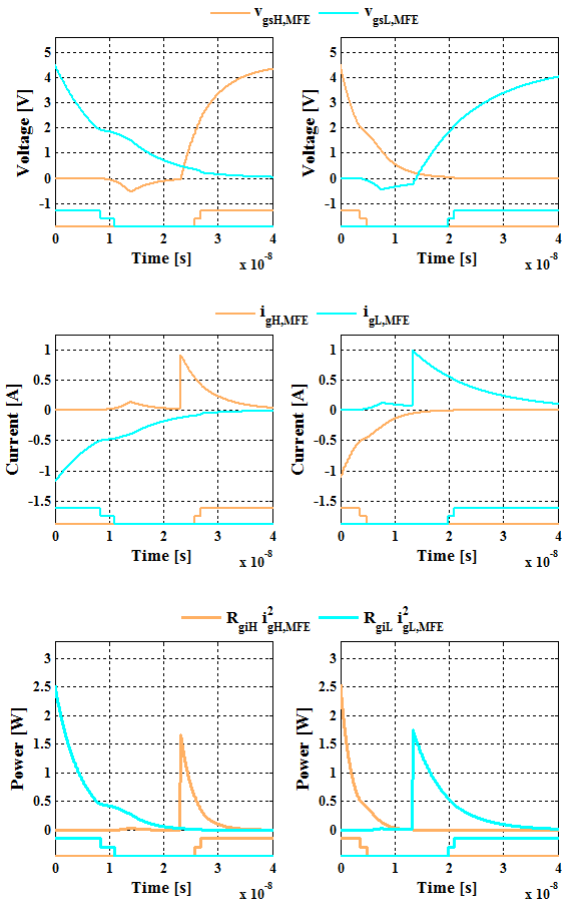
The power loss decrease due to capacitive currents is further emphasized in the third example (case #3), related to a buck converter of case #2 operating at low load with $I_{out}=1A$. The Dual N-channel Vishay SiZ790DT with embedded Schottky diode in parallel to low-side MOSFET has been considered for this case. The plots of Figure 4.8 highlight that the body diode of HSM conducts during the dead-time at LSM turn off while the Schottky diode of LSM conducts during the dead time at HSM turn off. Consequently, both MOSFETs exhibit hard turn off and soft turn on. This involves an equalization of switching losses between the two MOSFETs. The total capacitive current $i_{Ctot}=-i_{CdsH}+i_{CgdH}+i_{CdsL}-i_{CgdL}$ at low load passes through LSM channel during LSM turn off and through HSM channel during HSM turn off: in both cases the current i_{Ctot} produces a channel loss decrease, as shown in Figure 4.8(b).

In such a case the evaluation of C_{oss} losses is meaningless. Due to the capacitive currents circulation, and to specific MOSFETs parameters, the net effect of the output current ripple in the specific case is to decrease the HSM loss and to slightly increase the LSM loss, at high load, while a partial split of power loss from the LSM Schottky diode to the HSM body diode occurs at light load.

The above discussion highlights that the simplified formula $0.5C_{oss}V_{off}^2f_s$ provides a quite coarse approximation of HSM channel power loss due to charge/discharge of MOSFETs output capacitances. It is, instead, more opportune to look for noise and possible losses caused by the capacitive current spikes in the external circuit. Indeed, external circuit resistance dissipates power during charging and discharging HSM and LSM capacitances as part of the net charge injected into or extracted from the SRSC is fed by the external voltage source V_{off}. Such loss can be calculated by means of the simplified formula $Q_d f_s V_{off}$, where Q_d is the net charge exchanged during the turn ON and OFF of the HSM, as the current corresponding to Q_d is

normally fed by the by-pass capacitor connected across HSM drain and LSM source. So that, this loss is external to the MOSFET.

Another week point of simplified formulas for MOSFETs losses calculation concerns the gate losses. These are usually calculated as $P_{gate}=Q_g\ f_s V_{dr}$, where Q_g is the total charge transferred to/from the MOSFET through the gate during the commutation. Such formula is the average power lost in the resistance R of an RC circuit to bring the voltage of capacitance C from 0 to V_{dr} and vice-versa at a frequency f_s. Considering $P_{gate}=Q_g f_s V_{dr}$ as the loss taking place into the MOSFET gate is not correct for two reasons. First, only part of the resistance in the charging/discharging gate circuit, namely R_{gi}, belongs to the MOSFET, whereas the other part, R_{gd}, belongs to the driver, so that part of the power dissipation ascribed to the MOSFET occurs into the driver instead. Moreover, during each commutation the voltage of the two capacitances C_{gs} and C_{gd} are not equal, as V_{gs} swings between 0 and V_{dr} whereas V_{gd} swings between $-V_{off}$ and $R_{ds}I_{on}$. In other words, C_{gs} and C_{gd} cannot be seen as two capacitances truly in parallel between gate and source, as well as C_{ds} and C_{gd} are not truly in parallel between drain and source, during the MOSFET commutations.



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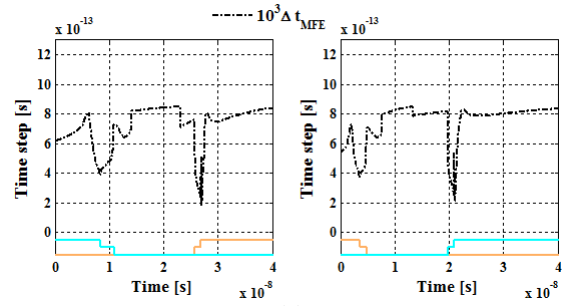


(c)

Figure 4.8 MFE simulation results for case #3: (a) HSM and LSM gate-to-source voltages (top) and currents (middle) and gate power loss (bottom), (c) MFE time step during the simulation.

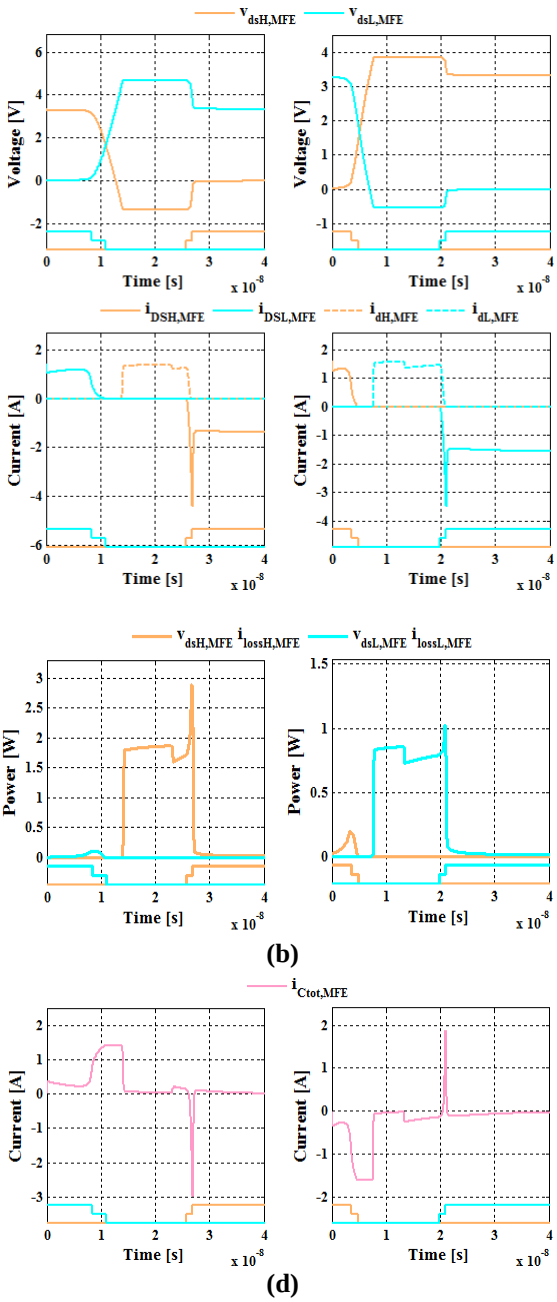


Figure 4.8 (Cont.) MFE simulation results for case #3: (b) HSM and LSM drain-to-source voltages (top), channel and diode currents (middle) and channel power loss (bottom); (d) total capacitive current flowing through HSM channel (right side plot) and LSM channel (left side plot).

Table 4.3 resumes the results of the HSM and LSM gate loss calculation, obtained by using the formula $P_{gate}=Q_g\ f_s V_{dr}$, based on datasheet values of Q_g at V_{dr} =4.5V. The results of simulations based on the MFE method discussed in this chapter allows a more appropriate and simple global analysis of charges flows and of related losses. Table 4.4 and 4.5 report, respectively, the results of the calculation of charges entering and exiting the gate and the drain terminals of HSM and LSM during the two commutations, and the calculation of channel and gate losses, for the three cases studies discussed above.

The formulas adopted for the calculation of charges and losses are shown in (21), where N represents the total number of points resulting from the simulation of the commutation.

$$\begin{aligned} Q_{gate} &= \sum_{k=1}^{N}[i_{Cgs}(t_k)+i_{Cgd}(t_k)]\Delta t_k \\ Q_{drain} &= \sum_{k=1}^{N}[i_{Cds}(t_k)-i_{Cgd}(t_k)]\Delta t_k \\ P_{gate} &= f_s\sum_{k=1}^{N}R_{gi}[i_{Cgs}(t_k)+i_{Cgd}(t_k)]^2\Delta t_k \\ P_{drain} &= f_s\sum_{k=1}^{N}V_{ds}[i_{DS}(t_k)-i_d(t_k)]\Delta t_k \end{aligned} \tag{21}$$

There is an evident discrepancy between the gate losses of Table 4.3 and Table 4.5. Although the results of Table 4.5 are not intended to be exact (they depend on the use of model of the capacitances obtained from the small signal curves available in the datasheets), they show that a big amount of losses caused by the gate charge transfer is external to the MOSFET and cannot be ascribed to it.

Table 4.3 Gate losses calculated with the approximated formula $P_{gate}=Q_g f_s V_{dr.}$

		losses [mW]	losses [mW]	losses [mW]
		case#1	case#2	case#3
HSM	P_{gate}	49,5	14,5	14,5
LSM	P_{gate}	18,0	33,5	33,5

Table 4.4 HSM and LSM gate and drain charges during commutations.

		charge [nC]		charge [nC]		charge [nC]	
		case#1		case#2		case#3	
		C_1	C_2	C_1	C_2	C_1	C_2
HSM	Q_{gate}	7,0	-7,0	5,2	-5,2	5,3	-5,3
HSM	Q_{drain}	-5,3	5,3	-2,8	2,8	-3,0	3,0
LSM	Q_{gate}	-3,4	3,4	-12,1	12,1	-12,2	12,2
LSM	Q_{drain}	1,9	-1,9	7,1	-7,1	7,2	-7,2

C_1 = LSM turning-off and HSM turning-on
C_2 = HSM turning-off and LSM turning-on

Table 4.5 HSM and LSM gate and drain losses during commutations.

		losses [mW]	losses [mW]	losses [mW]
		case#1	case#2	case#3
HSM	P_{drain}	35,7	67,7	12,4
HSM	P_{gate}	18,2	5,4	5,2
HSM	P_{driver}	13,4	6,5	6,2
LSM	P_{drain}	24,5	103,5	6,0
LSM	P_{gate}	7,1	11,1	11,8
LSM	P_{driver}	6,3	15,7	16,8

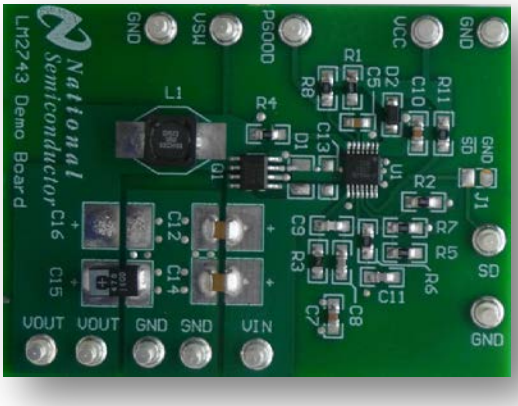
The MOSFETs capacitive currents shown in Figures 4.5(d), 4.7(l) and 4.8(d) flow through the external by pass capacitor connecting the HSM drain and the LSM source which prevents their circulation through the line rail or the load rail or both, depending on the topology. The charge injected into the by-pass capacitor is given by Q_d values in Table 4.4. Such charge divided by the allowed voltage variation ΔV_{offmax} provides the minimum required by-pass capacitance $C_{min}=Q_d/\Delta V_{offmax}$.

4.5 Experimental Tests

The model (11)(12) has been adopted to simulate the MOSFET SRSC in the LM2743 National Semiconductor Evaluation Board [31] of Figure 4.9(a), corresponding to case #1, with: V_i *=6V*; V_o*=1.2V*; I_o*=1.44A*; Δi_{Lpp}*=1A*; f_s*=963kHz*; dead time*=15ns*; R_{gdon}*=2Ω*; R_{gdoff}*=2Ω*; R_{gdext}*=2.2Ω*. The measurement set-up is shown in Figure 4.9(b) and its main components parameters are resumed in Table 4.6.

Table 4.6 Main components parameters of LM2743 Evaluation Board.

Devices	Part Number	Manufacturer	Main Attributes
HS and LS MOSFETs	Si9926BDY	Vishay	v_{DS}=20V, $R_{ds,on}$=24mΩ
Output Inductors	DR73-1R0	Cooper	L=1µH, I_{rms}=5.3A, DCR=10.2mΩ
Input Filter Capacitors	2x12103D106MAT	AVX	(Ceramic) C=10µF, V=25V
Output Filter Capacitors	6TPD470	Sanyo	C=470µF, V=6.3V, ESR=10mΩ



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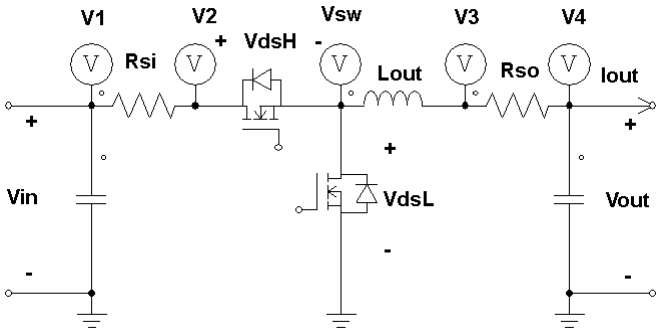
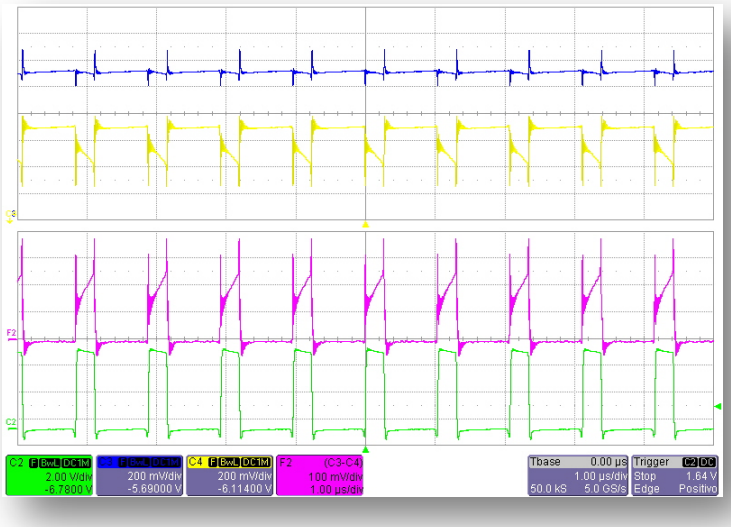


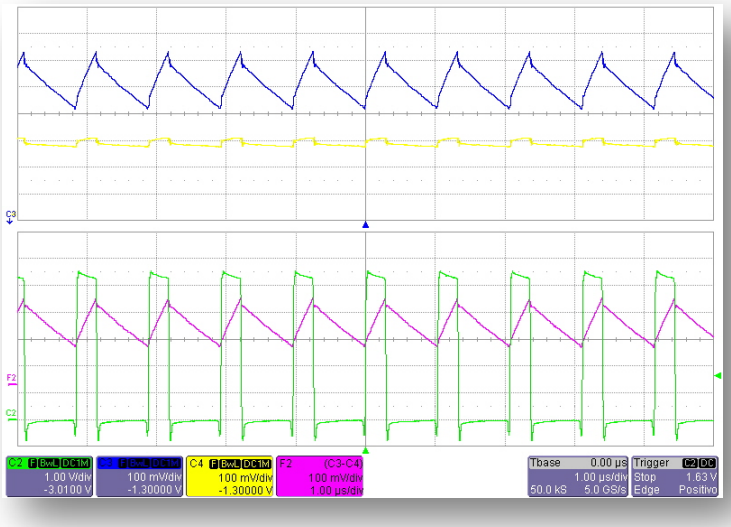
(b)

Figure 4.9 (a) LM2743 Evaluation Board , (b) measurement set-up.

Two additional Si4982DY MOSFETs are mounted on the original board. They are kept permanently ON and their resistances (R_{si} and R_{so} in Figure 4.9(b)), are used to sense the current entering the SRSC, i_{dsH}, and the current exiting the SRSC, i_{Lout}, in order to minimize the parasitic inductances. The current of LSM is given by i_{dsH}-i_{Lout}. The values of R_{si} and R_{so} can be easily calibrated by means of a reference current. The parasitic inductances in the MOSFETs gate and line branches have been estimated as follow: L_{gH}=9.5nH, L_{gL}=9.5nH, L_{off}=5nH. Figure 4.10 shows the oscilloscope screenshots of the voltages V_1, V_2, V_3, V_4 and V_{sw}.



(a) **blue=V_1, yellow=V_2, magenta=V_1-V_2, green=V_{sw}**



(b) **blue=V_3, yellow=V_4, magenta=V_3-V_4, green=V_{sw}**

Figure 4.10 Experimental measurements on EVB LM2743.

The HSM and LSM drain-to-source currents obtained with simulations based on model (11)(12) and with experimental measurements are shown in Figure 4.11. The comparison puts in evidence that the MFE method introduced to solve the non linear model (11)(12) allows reliable simulations even including parasitic inductances characterizing the SRSC MOSFETs as well as the external circuit. If parasitic parameters are correctly modeled, the agreement between simulations and measurements can be very good.

Moreover, the method also allows to detect behaviors of the switching cell which are determined by the joined effect of elements characterizing the operation of the driver and elements characterizing the MOSFETs. For example, the two prominent current peaks appearing at the turn on and at the turn off of the HSM are not due to MOSFETs capacitances nor to diode reverse recovery (indeed a Schottky diode is in parallel to the LSM): they are due to a slight cross-conduction of the two MOSFETs during the commutations caused by the specific dead-time set-up of the IC, which is too short for the particular couple of MOSFETs considered in the example.

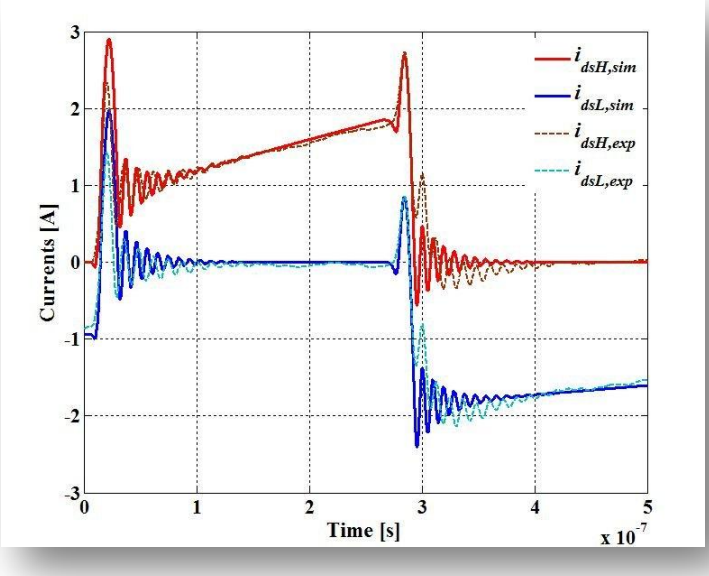


Figure 4.11 Comparison between simulation results and experimental measurements.

The method presented in this dissertation can then be used to test MOSFETs capacitive models as well as to make the identification of parasitic elements and specific operation of IC switchers influencing the MOSFETs commutations and related losses and noise, thus helping in the detection of the most opportune combinations of power and control devices.

4.5.1 Experimental Activity improvements

As discusses in Chapter 2, the experimental losses measurements for high-frequency high-efficiency devices, like in case of the switching cell discussed in this Chapter, is a complex task which has often limited practical value in terms of real possibility to ascribe certain characteristics of the observed wave-shapes to the physical properties of the device under test rather than to the wide variety of collateral parasitic elements and limitations of the measurements circuit and systems. Indeed, in most cases, *none of the experimental investigation approaches provide the physical insights of MOSFET switching operation* [4].

The on-line measurement technique based on the use of MOSFETs as sensing resistors illustrated in Chapter 2 has been also investigated and adopted in order to achieve losses estimation in synchronous rectification switching cells. As case study, let us refer to a synchronous buck converter with the following specifications:

- V_{in}=6V, V_{out}=3.3V, I_{out}=1.5A, f_s=100kHz.

The circuit schematic of Figure 4.12 represents a proof of concept for this experimental measurements investigation. The Texas Instruments TPS2836/7 gate driver [32] with dead-time control has been selected for this application. Two N-channel MOSFET SI4410DY [33] and a dual N-Channel MOSFET Si4936CDY [34] have been selected as HSM, LSM and sensing MOSFETs, respectively.

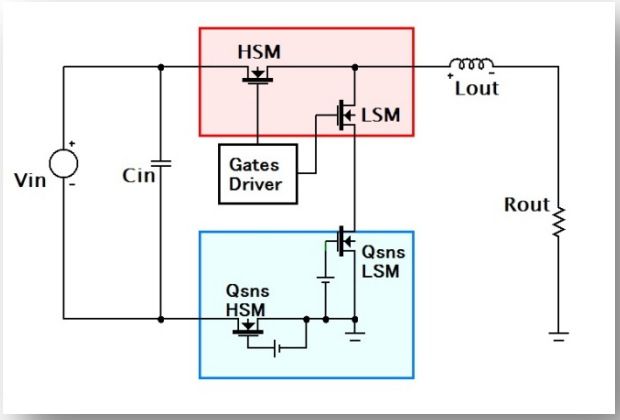
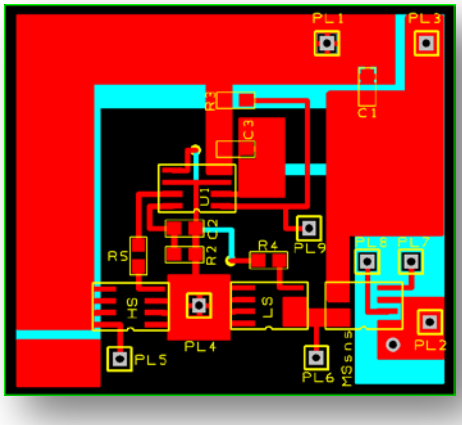


Figure 4.12 Circuit schematic adopted for experimental verification.

A first layout has been developed and realized using the Circuit Prototyping System T-Tech Quick Circuit 5000, available in the Power Electronics and Renewable Sources Laboratory of Salerno University. Layout and resulting board are shown in Figure 4.13(a) and 4.13(b), respectively. The preliminary sensing waveforms obtained with this board are characterized by high parasitic inductances, resulting in high *di*/*dt* paths and marked oscillations the waveforms commutation, as shown in Figure 4.14.



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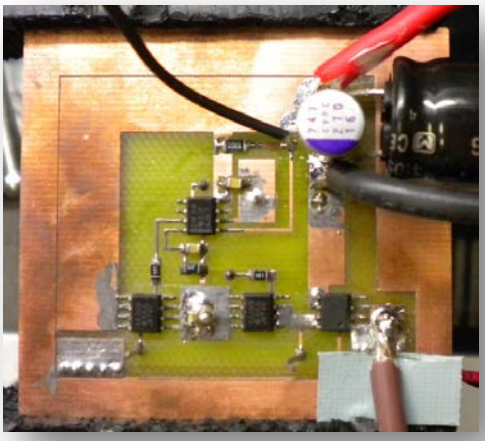


(b)

Figure 4.13 First layout (a) and mounted board (b).

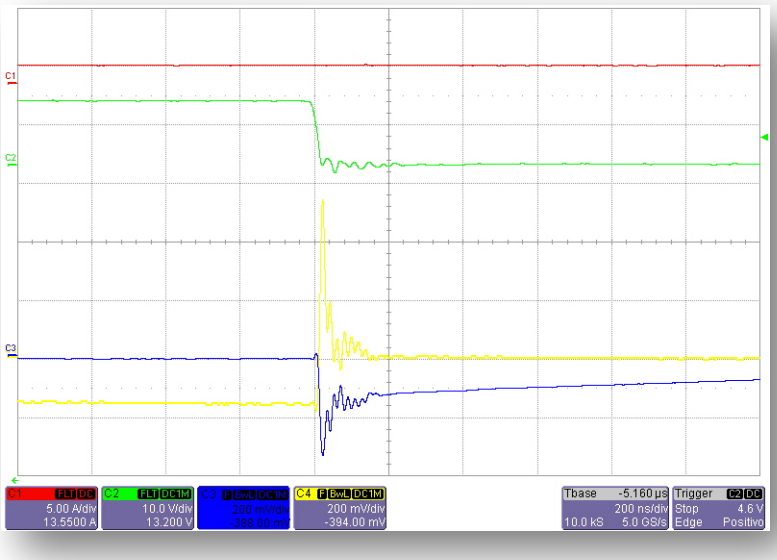


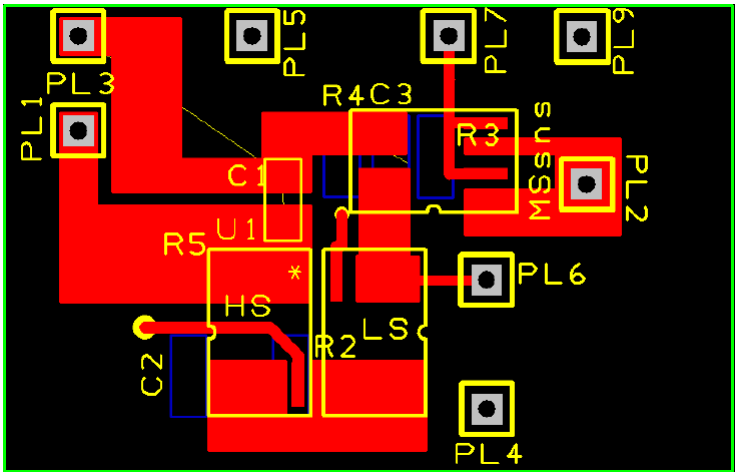
Figure 4.14 Experimental waveforms obtained with the first board: input current (red), HSM gate-to-source voltage (green), LSM sensing drain-to-source voltage (yellow), HSM sensing drain-to-source voltage (blue).

In order to improved the measurements, a new layout has been investigated, pursuing the following goals:

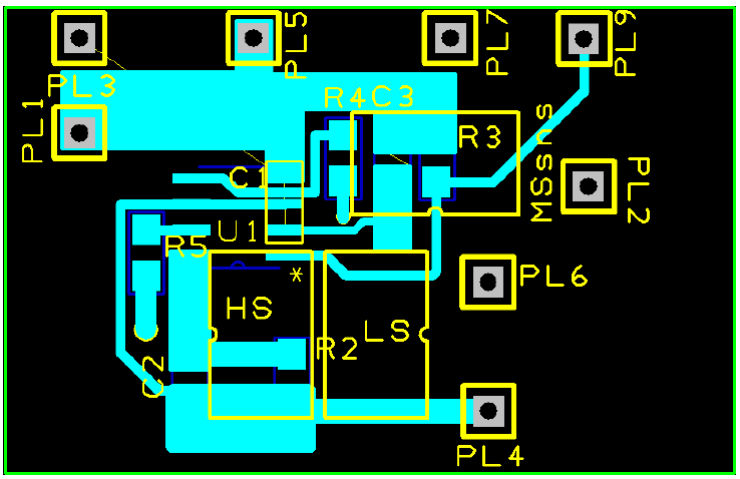
- minimize the loop area enclosed by HSM and LSM and input capacitor;
- minimize the gate loop area for HSM and LSM and their return paths;
- keep inductor very close to switching node, in order to stem the effects of high *dv*/*dt* node;
- minimize stray inductance in the power path.

The layout has been realized and the board has been mounted. They are shown in Figure 4.15 and 4.16, respectively. Preliminary test results are shown in Figure 4.17, where parasitic inductances effects are still quite evident. At the moment of this writing, experimental activities are still in progress. The on-line measurement technique based on the use of MOSFETs as sensing resistors goes beyond the goals of this dissertation. However, for completeness, experimental activities have been documented mainly because they have shown

very interesting future perspectives: in fact, some magnetic devices and silicon devices manufacturing companies have expressed interest for this approach. Thus, further studies will be carried out also in the framework of future research collaborations with these companies, to achieve the full operation of such online measurement technique.

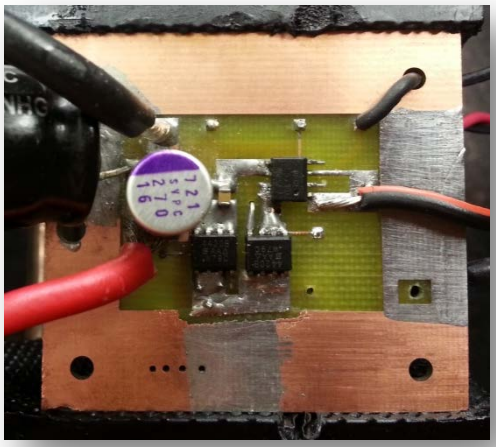


(a)

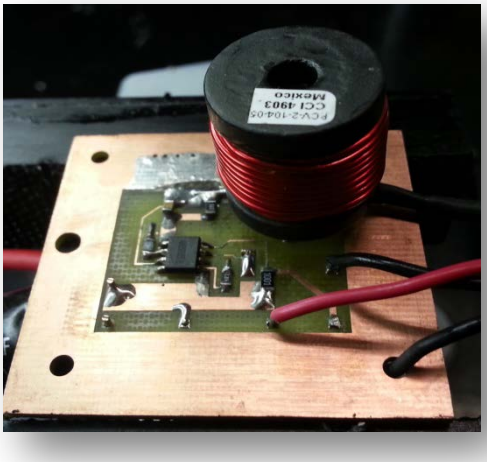


(b)

Figure 4.15 Second layout: top layer (a) and bottom layer (b).



(a)



(b)

Figure 4.16 Second mounted board: top layer (a) and bottom layer(b).

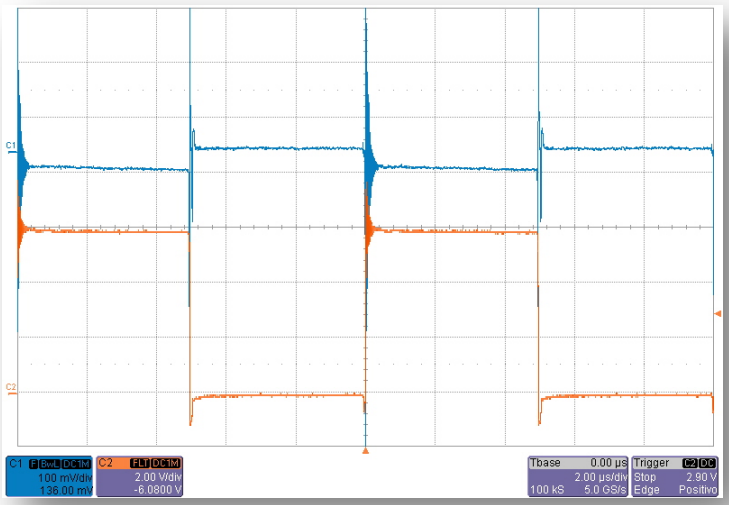


Figure 4.17 Experimental waveforms obtained with the second board: HSM gate-to-source voltage (red), HSM sensing drain-to-source voltage (blue).

Comments

The MFE method presented in this chapter allows to analyze the capacitive currents and the switching losses of couples of MOSFETs realizing the half-bridge elementary cell used in most of high-efficiency switching converters. The couple of MOSFETs is described by a unified system of non linear differential equations, based on the representation of MOSFET electrode capacitances as double exponential functions of the drain-to-source voltage. A dedicated Modified Forward Euler technique has been developed to solve the stiff non linear switching cell model, allowing the use of different types of capacitive models. The proposed solution technique provides a better trade-off between computing times and solution accuracy compared to implicit ODE solution routines, thanks to an adaptive time step control specifically developed to provide accurate and fast solution of the non linear differential equations describing the couple of MOSFETs. The waveforms obtained using the method presented in this dissertation allow more accurate switching analysis and loss

calculation with respect to simplified models presented in technical literature. One of the most important results achievable by using the proposed method consists in a more realistic analysis of MOSFETs capacitive currents during the commutations and in the correct determination of their magnitudes and paths through the MOSFETs and the external circuit, thus also supporting EMI and PCB issues investigations. A major benefit of the method presented in the chapter consists in providing a way to quickly analyze MOSFETs commutations with minimum coding, not requiring the use of circuit simulators.

The MFE method is best suited for loss analysis needed for MOSFET selection in high-efficiency converters design as it allows quick and reliable comparative evaluation of different MOSFET couples. Accordingly, in the future development of this research, the numerical model discussed in this chapter will be integrated in a more general algorithm, aimed at realizing the automatic detection of MOSFETs combinations ensuring minimization of total losses for whatever converter topology using synchronous rectification configurations like the ones of Figure 4.1.

In next chapter, the capability of the model to treat MOSFETs commutations including stray inductances will be exploited in the search of MOSFETs and transformers whose parasitic capacitances and leakage inductances, respectively, combined in such a way to ensure soft switching and total losses minimization in isolated converter topologies using synchronous rectification, like high-current dc-dc Forward Active Clamp.

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Chapter 5

System Level analysis of an Active Clamp based Forward Converter

Models developed and discussed in previous chapters can be adopted as building blocks for a generalized correlation model between stress and loss of solid-state and magnetic devices. The dc-dc Forward Active Clamp (FAC) converter is the topology chosen as case study in this chapter. This converter is a popular choice for single and multiple output power supplies within the range of 50 W to 500 W. There are several widely used techniques for achieving transformer reset [1]-[3], but the Active Clamp approach is today recognized as the best solution in terms of simplicity and optimal performance and same advantages can be advantageously obtained from Active Clamp based Flyback converters too [4]. Implementing active clamp technique for single-ended Flyback and Forward converter designs enhances efficiency at high switching frequencies, while lowering component stresses. Moreover, by providing soft switching, this technique also reduces EMI.

5.1 Forward Active Clamp Overview

Forward topology has been widely use for several decades. Its popularity has been based many factors, as designers have been draw to the positive cost, complexity and efficiency tradeoffs. Beyond the typical advantages of this isolated topology, Forward performance can be significantly enhanced by using active clamp/reset technique. A huge number of technical literature, including textbooks, scientific papers and application notes, has been produced on Forward Active Clamp converter (FAC) and many references [1]-[23] can be take into consideration for a complete survey on this subject. Some main issues of FAC converter can be resume as follow:

- optimum reset of magnetic core, with re-circulating of the leakage and magnetizing energy;
- better *B*-*H* magnetic utilization, since FAC uses the first and third quadrants of the *B*-*H* curve.
- minimum switching losses of the main power MOSFET, because turn-off transitions occurs at ZVS; theoretically, in some extent, it's possible to achieve ZVS also during turn-on transition;
- EMI reduction;
- possible duty-cycle operations above 50%;
- minimum stress to the primary MOSFET switch;
- possible synchronous rectification on the secondary side, with self-driven synchronous rectifiers.

Two possible FAC configurations can be obtained, applying the clamp circuit to either the high side, directly across the transformer primary, or the low side, directly across the drain-to-source of the main MOSFET switch (see Figures 1.3(a) and 1.3(b) in Chapter 1). There are some important differences in applying High Side (HS) or Low Side (LS) active clamp circuits. Firstly, the HS clamp uses an N-channel device as auxiliary MOSFET, so there are more component choices available than the LS clamp, which instead use a P-channel device. The HS clamp circuit also requires a gate drive transformer, while the gate drive circuit for the LS clamp is simpler, since a gate drive transformer is not required. Moreover, each clamping circuit results in a different voltage stresses and in the way they change with the input voltage for different values of the transformer turns ratio. Detailed comparison between HS and LS FAC can be found in [5]-[7].

In the following, without loss of generality, LS FAC is taken into consideration for discussing important and useful issues on correlation existing among magnetic and silicon devices. The same investigation can be proposed also for HS FAC and other active clamp based converter topology.

5.2 Stresses constraints in LS-FAC

As case study, let us consider a LS FAC with the specifications given in Table 5.1. Given efficiency requirements for the converter, the total allowed power dissipation is given by (1):

$$P_{diss} = P_{out} \frac{1-\eta}{\eta} \tag{1}$$

where P_{diss} and P_{out} are the dissipated and the output power of the converter and η is the required efficiency. According to [23], it is possible to consider the guess power distribution among magnetic and silicon devices according to percentages given in Table 5.2.

It is a common practice starting isolated converter design by fixing the secondary side output components. Given a reasonable range of duty-cycle value, the output power stage design can be quite easily done [24]. In this regard, FAC can push the maximum duty-cycle to 60% and has even been used with duty-cycle as high as 70-75% in some very low applications.

Table 5.1 LS FAC converter specifications.

Parameter	*Symbol*	*Value*
Input Voltage	V_{in} [V]	36÷72
Frequency	f_S [kHz]	250
Efficiency	η [%]	90
Output Voltage	V_{out} [V]	3.3
Output Voltage Ripple	ΔV_{out} [mV]	50
Output Current	I_{out} [A]	3÷30

Table 5.2 Guess Power distribution among devices.

Parts	[%]
Rectification MOSFETs	50
Main MOSFET	10
Power Transformer	15
Output filter	20
IC, Current Sensing & Control	5

For this example, it is reasonable to assume that the maximum duty-cycle is limited to 60% at $V_{in}=36V$ during normal operation, while the duty-cycle is approximately 30% at $V_{in}=72V$. Thus, power transformer is required to be fixed: this is a very critical choice. Indeed, as better clarified in the followings, this magnetic device puts tight constraints both on silicon devices and on operating conditions (e.g. higher *vs* lower duty-cycle) and reference topology reliability (e.g. self-synchronous *vs* control-driven secondary solution). In fact, using correlations among transformer turns ratio *N* and silicon devices stresses, it is possible to identify subsets of MOSFETs allowing feasible design for each transformer. Thus, the transformer and the four MOSFETs must be selected trying to balance stresses and losses.

For this case study, Pulse planar transformers have been considered. In particular, Pulse PA08xx and PA09xx [25] are the two high frequency planar transformer series investigated, with power rating up to 140W and 250W, respectively. In Pulse datasheet it is possible to find a complete "matrix" of all the configurations available for PA08xx and PA09xx platform (with single winding, dual winding or tapped winding configuration, both for primary and secondary side of transformers): according to how primary and secondary windings turns are linked together (in series or in parallel), different transformers can be realized. Thus, to the same device part code (which identifies the magnetic core and a certain number of turns for primary and secondary windings) can be practically associated more than one transformer. According to this, all the combinations for single primary and single secondary winding configurations have been considered, for both PA08xx and PA09xx platform, which can be assumed as transformers database available for the given application.

Once a configuration is selected, the formulae and charts reported in the transformers datasheet can be used to determine the approximate power dissipation of the magnetic device for the given application. The maximum transformer power loss can be calculated evaluating both core power losses and windings power losses. For core power losses P_{core}, Pulse provides formula (2):

$$P_{core} = f_s^{\alpha} \cdot \Delta B_{ac}^{\beta} \cdot K_{Vol} \tag{2}$$

where f_s [kHz] is the switching frequency, K_{Vol} is a factor depending on the volume of the core, α= 1.8, β=2.5 and ΔB [G] is the flux density. According to [25], ΔB can be evaluated in the worst case as in (3):

$$\Delta B = K_{Ac} \cdot \frac{V_{in,\min} D_{\max}}{f_s \cdot n_p} \tag{3}$$

where n_p is the primary winding turns number and K_{Ac} is a proper factor depending on the cross section area A_c of the core. According to Pulse series data, $K_{Ac}=180\cdot10^3$, $K_{Vol}=1.59\cdot10^{-13}$ for PA08xx and $K_{Ac}=120\cdot10^3$, $K_{Vol}=2.53\cdot10^{-13}$ for PA09xx. Windings power losses P_{wind} can be evaluated by (4):

$$P_{wind} = DCR_p \cdot I_{p,rms}^2 + DCR_s \cdot I_{s,rms}^2 \tag{4}$$

where DCR_p, DCR_s, $I_{p,rms}$ and $I_{s,rms}$ are the DCR values and the rms current values for primary and secondary windings, respectively. In particular, these currents can be calculated using (5) and (6):

$$I_{p,rms} \approx \frac{I_{out}}{N} \cdot \sqrt{D} \tag{5}$$

$$I_{s,rms} \approx I_{out} \cdot \sqrt{D'} \tag{6}$$

where $N=n_p/n_s$, $I_{p,rms}$ and $I_{s,rms}$ are the rms current of the transformer primary and secondary side, respectively. Accordingly, (4) can be also written as in (7):

$$P_{wind} = DCR_{p,eq} \cdot I_{p,rms}^2 \tag{7}$$

where:

$$DCR_{p,eq} = DCR_p + DCR_s \cdot N^2 \tag{8}$$

Thus, given a transformer database with proper power rating, turns ratio N is fixed and a first pre-selection for suitable device can be done evaluating both the achievable minimum and maximum duty-cycle (resulting from topology conversion ratio), and the resulting power losses.

Nevertheless, transformer turns ratio *N* and the resulting converter duty-cycle deeply impact also on silicon devices stresses. In the following, voltage and current stresses for MOSFETs in LS FAC converter have been summarized from (9) to (12), according to the circuit schematic of Figure 5.1:

$$V_{Q_1} = \frac{V_{in}}{1-D}, \qquad I_{rms,Q_1} = \frac{I_{out}}{N}\sqrt{D} \tag{9}$$

$$V_{Q_2} = \frac{V_{in}}{1-D}, \qquad I_{rms,Q_2} = I_{MAG}\sqrt{\frac{D'}{3}}, \quad I_{MAG} = \frac{V_{in}D}{f_{sw}L_{MAG}} \tag{10}$$

$$V_{Q_3} = \frac{D}{D'}\cdot\frac{V_{in}}{N}, \quad I_{rms,Q_3} = I_{out}\sqrt{D} \tag{11}$$

$$V_{Q_4} = \frac{V_{in}}{N}, \qquad I_{rms,Q_4} = I_{out}\sqrt{D'} \tag{12}$$

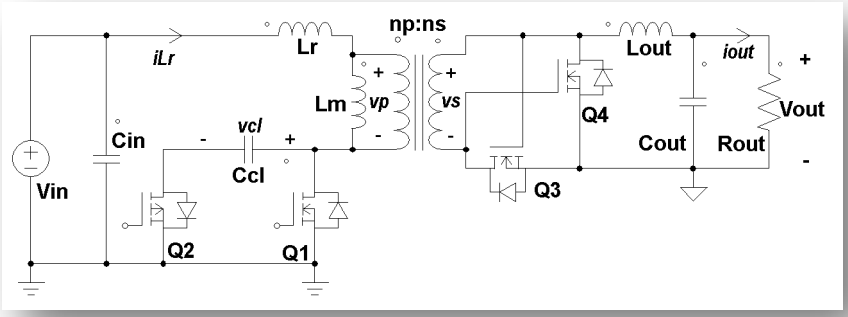


Figure 5.1 LS FAC converter circuit schematic.

Let now consider a set of commercial N-channel and P-channel MOSFETs from different manufactures, having the following voltage and current ratings: $|V_{DS}|=20V \div 200V$ and $|I_{DS}|=1A \div 100A$.

In V_{DS} *vs* I_{DS} plane, commercial MOSFETs can be identified by their voltage and current ratings, and commercial transformers can be represented by the voltage and current stresses they impose to MOSFETs as a consequence of by their turns ratio *N*. In Figures from 5.2 to 5.5 this concept is proposed. For example, in Figure 5.2 a set of commercial N-channel MOSFETs, identified by yellow circles, is represented according to their voltage and current ratings. In the same figure, red triangles represent a set of commercial planar transformers, available in terms of resulting duty-cycle and power losses for the given application: these transformers are identified by the voltage and current stresses (including a 20% of safety margin) they impose to MOSFET Q_1, depending on their own windings turns ratio. For each transformer, a MOSFETs Acceptability Regions (ARs) can be identified, in which a proper and not oversized Q_1 device can be chosen. For the same application and for the same set of transformers, similar analysis can be proposed for Q_2 (see Figure 5.3), Q_3 (see Figure 5.4) and Q_4 (see Figure 5.5).

Thus, let suppose to have fixed the magnetic device and Pulse PA0810 [25] has been chosen among all the available planar transformers: the corresponding ARs have been delimited by the colored boxes in each one of the V_{DS} *vs* I_{DS} plane (see Figure from 5.2 to 5.5). All MOSFETs falling into ARs allow feasible design: the ones with minimum power rating represent the more suitable for the design in terms of both minimum size of devices and maximum power density of the converter.

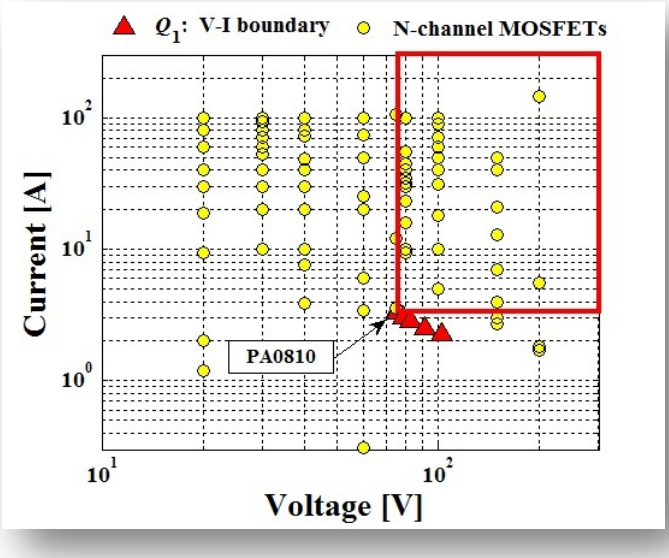


Figure 5.2 AR for MOSFET Q_1 according to PA0810 transformer.

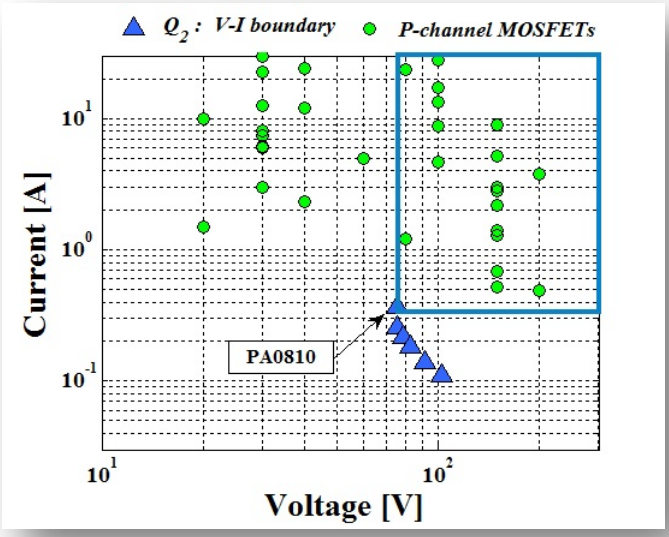


Figure 5.3 AR for MOSFET Q_2 according to PA0810 transformer.

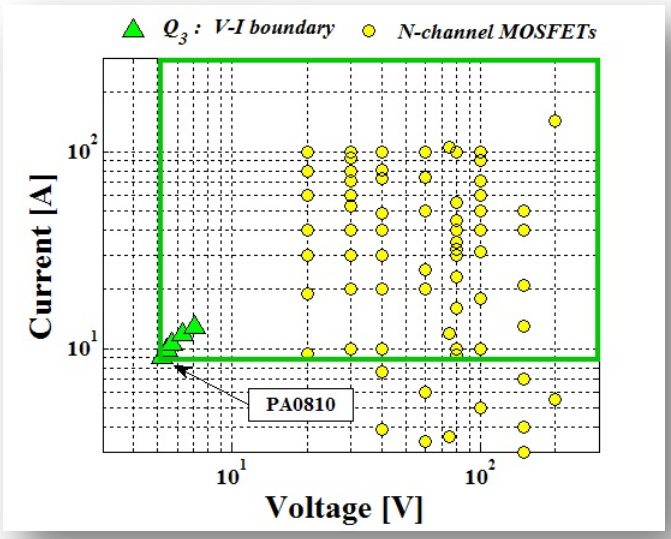


Figure 5.4 AR for MOSFET Q_3 according to PA0810 transformer.

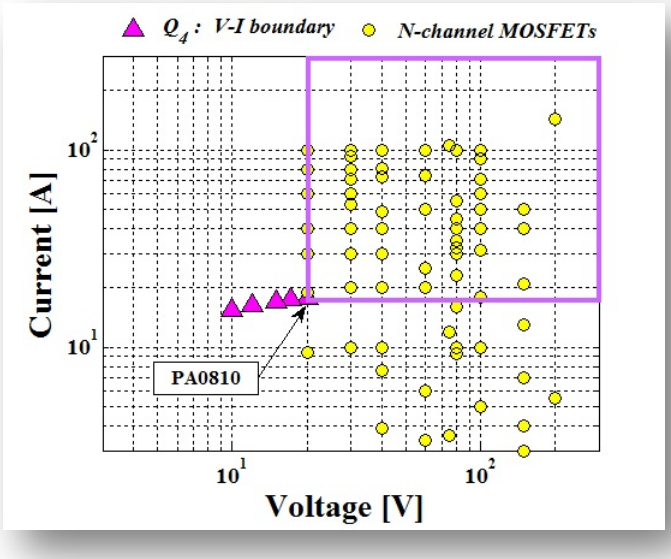


Figure 5.5 AR for MOSFET Q_4 according to PA0810 transformer.

Therefore, a quick and effective identification of the feasible joined selections of transformer and MOSFETs complying with the desired trade-off constraints (size, cost, etc) can be realized. A search algorithm to select the best Bill of Material (BOM) can be used using the fitness function concept, whose weighted figures of merit could be properly calibrated according to the overall design goals. In particular, based on design constraints, a preliminary selection of physical silicon devices and transformers can be done for the search of design solutions. The duty-cycle D is fixed for each transformer based on its turns ratio. For any given switching frequency f_s value, the feasible sets of physical devices to be compared are the only ones complying with losses budget, which depend on the required efficiency. Size and reliability constraints have also to be considered in the design solutions scoring. In order to analyze the overall design feasibility and performances, the fitness function (13) can be used:

$$f_x = c_P \gamma_{Px} + c_S \left(\alpha_S \gamma_{Sx} + \alpha_V \gamma_{Vx} \right) + c_R \gamma_{Rx} \leq 1 \tag{13}$$

where the weighted Figures of Merit (FoM) γ_{Px}, γ_{Sx}, γ_{Vx} and γ_{Rx} are related, respectively, to total losses, silicon devices stresses, transformer volume and reliability. The weights c_P, c_S and c_R, with $c_P + c_S + c_R = 1$, can be calibrated according to design priority (cost, loss, reliability or balance of them). Let us analyze some possible definitions for the FoMs. The loss FoM γ_{Px} can be defined according to (14):

$$\gamma_{Px} = \frac{P_{d,x} - P_{d,\min}}{P_{d,\max} - P_{d,\min}} \leq 1 \tag{14}$$

where $P_{d,x}$ is the total loss associated to the combination x of physical devices, $P_{d,min}$ is the total loss associated the combination ensuring minimum dissipation, $P_{d,max}$ is the total loss associated the combination involving the maximum dissipation. For silicon devices, the losses estimation can be quite easily done starting from datasheets parameters and using the models and methods discussed in the previous chapter. For each transformer, the loss calculation can be done by means of the data provided by manufacturers. Only windings losses estimation is possible for most of commercial transformers, as

manufacturers do not provide information to estimate core losses. This is due to the several facts. Mainly, manufacturers do not want to disclose the type of core they use and, in order to guarantee reliable operation, they specify operating current and frequency limits for their transformer such that core losses are negligible compared to windings ones. Indeed, most of commercial transformers are saturation-based rather than loss-based designed (see A_p design formulas in Chapter 2).

The silicon devices stress FoM γ_{Sx} can be defined according to (15.a):

$$\gamma_{Sx} = \frac{D_{p,x} - D_{p,\min}}{D_{p,\max} - D_{p,\min}} \leq 1, \quad D_{p,x} = \alpha_{der} \frac{S_x}{S} \tag{15.a}$$

where α_{der} is a de-rating factor (typically, *0.6÷0.8*), S is the global analytical stress factor and S_x is the global ratings factor, given in (15.b) and (15.c), respectively:

$$S = \sum_x V_{Qx} I_{rms,Qx} \ , \qquad x = 1,..,4 \tag{15.b}$$

$$S_x = V_{BDx} I_{Fx,} \quad x = 1,...,4 \tag{15.c}$$

where V_{BDx} is the breakdown voltage and I_F is the forward current of each silicon device.

The transformer volume FoM γ_{Vx} can be defined according to (16):

$$\gamma_{Vx} = \frac{V_x - V_{\min}}{V_{\max} - V_{\min}} \leq 1 \tag{16}$$

where V_x is the core volume of the transformer x, V_{min} is the core volume of the transformer of minimum size, V_{max} is the core volume of the transformer of maximum size.

The reliability FoM γ_{Rx} can be defined according to (17):

$$\gamma_{Rx} = 1 - \frac{MTBF_x - MTBF_{\min}}{MTBF_{\max} - MTBF_{\min}} \leq 1 \tag{17}$$

where $MTBF_x$, $MTBF_{min}$ and $MTBF_{max}$ are the values of Mean Time Between Failures, respectively, of device combination x and of device combination with minimum and maximum MTBF. Both FoMs γ_{Sx} and γ_{Vx} take into account the size of the relevant devices, even if in different way. Indeed, while the transformer size is merely related to its footprint and height, for silicon devices the size of the package is not a direct expression of the silicon area, as dies of different size can be encapsulated in the same package. Therefore, this is why the stress factor is used for silicon devices. The global weighted FoM ($\alpha_S\gamma_{Sx}+\alpha_V\gamma_{Vx}$) expresses the size of transformer and silicon devices. The weights α_S and α_V can be settled according to the design priority. Based on the definition of the FoMs and of the fitness function (13), given a set of weighting coefficients and given a set of silicon devices and transformers setups complying with voltage and current ratings constraints, all feasible design combinations can be analyzed and scored, based on the fitness function (13).

As far as the isolated converter is designed by using off-the-shelf commercial transformers and no special soft-switching feature is required based on their parasitic parameters (leakage inductance), the key point is the selection of the combination of parts ensuring the desired trade-off. It is a combinatorial problem which can be afforded either with exhaustive search, in case of not limited space of search, or with some more intelligent stochastic algorithm, such as Genetic Algorithms.

When the application requires the achievement of special soft-switching features, some more in-depth investigation is required to qualify and score appropriately each combination of power devices whose parameters are involved in the equivalent resonant circuit implementation. The case of FAC converter discussed in the next section falls in this category.

5.3 ZVS investigation in LS-FAC

LS-FAC and HS-FAC with secondary synchronous rectification have been largely discussed in recent year, mainly because the active clamp technique is actually one of the most attractive ZVS topologies for low voltage converter [8]-[12]. In literature, many references can

be found discussing the analysis, the design and the implementation of FAC. Many synchronous rectifier configurations (like half-wave rectifier and center-tap or current doubler full-wave rectifier) have been proposed both for LS-FAC and HS-FAC in order to improve converter efficiency [13]-[14], and several dedicated commercial driver ICs have been presented [21][23].

In [6] a detailed analysis of LS-FAC with self-synchronous rectifier is given (see Figure 5.1). The converter operations have been depicted and analyzed according switches and their relative body-diode states: over one switching period, twelve operating time intervals have been recognized and equivalent circuits of the resulting stages are also given in [6]. In Table 5.3 an overview of all switches (Q_x , $x=1,\ldots,4$) and intrinsic body diodes (D_x , $x=1,\ldots,4$) conduction states is given. The most critical stages are represented by states from 2 to 5 and by states from 9 to 12: in these intervals the ZVS turn-on of the auxiliary MOSFET and the eventually ZVS turn-on of the main MOSFET occur. Nevertheless, while the ZVS turn-on of Q_2 is determined by current circulating in the clamp circuitry, $_1$ realizes ZVS turn-on only if in resonance stages inequality (18) is fulfilled:

$$\frac{1}{2} L_r \; i_{Lr}^2(t_8) > \frac{1}{2} C_r \left[v_{Cr}(t_9) - v_{Cr}(t_8) \right]^2 \tag{18}$$

where the resonance inductor L_r and capacitor C_r are the parasitic components of transformer and Q_1 - Q_2 switches respectively, t_8 is the time instant ending state 8 and starting state 9, at which the voltage capacitor v_{Cr} falls to V_{in} and t_9 is the time instant ending state 9 and starting state 10, at which the voltage capacitor v_{Cr} reaches 0V. Thus, to ensure main switch ZSV, the energy stored into the resonant inductance L_r until the time $t= t_8$ must be sufficient to discharge the resonant capacitance C_r within the time interval from t=[t_8, t_9]. In the worst case, inequality (18) can be also written as in (19):

$$-i_{Lr}(t_8) > \sqrt{\frac{C_r}{L_r}} \; V_{in,\max} \tag{19}$$

where the "*minus*" is related to the negative current circulating in the resonance inductor in state 8.

Table 5.3. LS FAC switches and body diodes conduction states.

state	Q_1	Q_2	Q_3	Q_4	D_1	D_2	D_3	D_4
1	on	off	off→on	off	off	off	off	off
2	on→off	off	on	off	off	off	off	off
3	off	off	on→off	off	off	off	off→on	off→on
4	off	off	off	off	off	off→on	on	on
5	off	off→on	off	off	off	on→off	on	on
6	off	on	off	off→on	off	off	off→on	on→off
7	off	on	off	on	off	off	off	off
8	off	on→off	off	on	off	off	off	off
9	off	off	off	on→off	off	off	off→on	off→on
10	off	off	off	off	off→on	off	on	on
11	off→on	off	off	off	on→off	off	on	on
12	on	off	off	off	off	off	on	on

Therefore, given $V_{in,max}$ and according to (19), the main switch ZVS turn-on mainly depends on the resonant inductance L_r and capacitance C_r. Both L_r and C_r are parasitic parameters. The inductor L_r has an almost known value, because in a lumped model of the transformer it is associated to the leakage inductance, capacitor C_r is rather related to the equivalent capacitance that can be seen at the main switch drain node during the resonance interval.

Because of the great value of the clamping capacitance C_{cl} compared to MOSFETs parasitic capacitances, the resonance equivalent capacitance C_{req} is usually approximated in the literature with the parallel of output parasitic capacitances of the main and the auxiliary switches, $C_{oss,Q1} = (C_{ds,Q1} + C_{gd,Q1})$ and $C_{oss,Q2} = (C_{ds,Q2} + C_{gd,Q2})$ respectively, as given in (20):

$$C_{req} = C_{oss,Q1} + \left(\frac{C_{oss,Q2} \cdot C_{cl}}{C_{oss,Q2} + C_{cl}} \right) \simeq C_{oss,Q1} + C_{oss,Q2} \tag{20}$$

However, if formula (20) is used and the values of $C_{oss,Q1}$ and $C_{oss,Q2}$ are taken as the maximum values of the capacitances plots provided in the datasheets, results of equation (19) verification might be misleading in the prediction of the soft switching achievement. This

can be at the origin of possible wrong conclusions about the possibility to achieve sufficiently high efficiency with FAC, because of the apparent lack of commercial parts whose parameters comply with the ZVS condition (19). Indeed, the output capacitances of MOSFETs are non-linear dependent with respect to drain-to-source voltages across them.

In particular, in the time interval of interest [t_8, t_9], these voltages are strongly varying: from V_{clamp} to $0V$ for $C_{oss,Q1}$ and from $0V$ to $-V_{clamp}$ for $C_{oss,Q2}$, where $V_{clamp} = V_{in}$. In the time interval [t_8, t_9], both the main and auxiliary MOSFETs are off. In order to obtain an *equivalent* capacitance value that gives the same stored energy of C_{req} while the drain-to-source voltages of the two MOSFETs are varying, the following analysis has to be done.

Let consider the net energy absorbed by the unknown C_{req} during the time interval [t_8, t_9]:

$$E_{C_{req}}\left[t_8, t_9\right] = \int_{t_8}^{t_9} v_{ds,Q1} \cdot i_{ds,Q1} dt + \int_{t_8}^{t_9} v_{ds,Q2} \cdot i_{ds,Q2} dt \qquad (21)$$

where ($v_{ds,Q1}$, $i_{ds,Q1}$) and ($v_{ds,Q2}$, $i_{ds,Q2}$) are the voltages and the currents of the capacitances $C_{oss,Q1}$ and $C_{oss,Q2}$, respectively. According to [26], currents $i_{ds,Q1}$ and $i_{ds,Q2}$ can be written as in (22.a)(22.b):

$$i_{oss,Q1} = \left(C_{oss,Q1} + v_{ds,Q1} \frac{dC_{oss,Q1}}{\left| dv_{ds,Q1} \right|} \right) \frac{dv_{ds,Q1}}{dt} \qquad (22.a)$$

$$i_{oss,Q2} = \left(C_{oss,Q2} + v_{ds,Q2} \frac{dC_{oss,Q2}}{\left| dv_{ds,Q2} \right|} \right) \frac{dv_{ds,Q2}}{dt} \qquad (22.b)$$

From (21) and (22), (23) can be obtained:

$$E_{C_{req}}\left[t_8, t_9\right] = f_1\left(v_{ds,Q1}, C_{oss,Q1}\right) + f_2\left(v_{ds,Q2}, C_{oss,Q2}\right) \qquad (23)$$

where:

$$f_1 = \int_{V_{clamp}}^{0} \left[v_{ds,Q1} \cdot C_{oss,Q1} + v_{ds,Q1}^2 \cdot \frac{dC_{oss,Q1}}{\left| dv_{ds,Q1} \right|} sign(v_{ds,Q1}) \right] dv_{ds,Q1} \tag{24}$$

$$f_2 = \int_{0}^{-V_{clamp}} \left[v_{ds,Q2} \cdot C_{oss,Q2} + v_{ds,Q2}^2 \cdot \frac{dC_{oss,Q2}}{\left| dv_{ds,Q2} \right|} sign(v_{ds,Q2}) \right] dv_{ds,Q2} \tag{25}$$

Representing $C_{oss,Q1}$ and $C_{oss,Q2}$ as linear combinations of two exponential terms (as shown in Chapter 4), we get (26) and (27):

$$C_{oss,Q1}\left(v_{ds,Q1}\right) = a_{o1} e^{b_{o1}\left|v_{ds,Q1}\right|} + c_{o1} e^{d_{o1}\left|v_{ds,Q1}\right|} \tag{26}$$

$$C_{oss,Q2}\left(v_{ds,Q2}\right) = a_{o2} e^{b_{o2}\left|v_{ds,Q2}\right|} + c_{o2} e^{d_{o2}\left|v_{ds,Q2}\right|} \tag{27}$$

Merging (26)(27) with (24)(25), yields (28) and (29):

$$f_1 = \frac{a_{o1}}{b_{o1}^2}\left(1 - B_1 e^{b_{o1} V_{clamp}}\right) + \frac{c_{o1}}{d_{o1}^2}\left(1 - D_1 e^{d_{o1} V_{clamp}}\right) \tag{28}$$

$$f_2 = \frac{3\, a_{o2}}{b_{o2}^2}\left(1 - B_2 e^{b_{o2} V_{clamp}}\right) + \frac{3\, c_{o2}}{d_{o2}^2}\left(1 - D_2 e^{d_{o2} V_{clamp}}\right) \tag{29}$$

where

$$B_1 = \left(b_{o1}^2 V_{clamp}^2 - b_{o1} V_{clamp} + 1\right) \tag{30.a}$$

$$D_1 = \left(d_{o1}^2 V_{clamp}^2 - d_{o1} V_{clamp} + 1\right) \tag{30.b}$$

$$B_2 = \left(\frac{1}{3} b_{o2}^2 V_{clamp}^2 - b_{o2} V_{clamp} + 1\right) \tag{30.c}$$

$$D_2 = \left(\frac{1}{3} d_{o2}^2 V_{clamp}^2 - d_{o2} V_{clamp} + 1\right) \tag{30.d}$$

Finally, $E_{Creq}[t_8, t_9]$ can be written as in (31):

$$E_{C_{req}}\left[t_8, t_9\right] = \frac{1}{2} C_{req}\left[v_{Creq}(t_9) - v_{Creq}(t_8)\right]^2 = \frac{1}{2} C_{req} \Delta V_{ds}^2 \qquad (31)$$

As ΔV_{ds} [t8;t9]=V_{in}, from (23) and (31), C_{req} can be evaluated as in (32):

$$C_{req} = 2 \cdot \frac{f_1\left(v_{ds,Q1}, C_{oss,Q1}\right) + f_2\left(v_{ds,Q2}, C_{oss,Q2}\right)}{V_{in}^2} \qquad (32)$$

Therefore, inequality (19) can more properly be reformulated as in (33):

$$i_{Lr}(t_8) < -\sqrt{\frac{C_{req}}{L_r}}\, V_{in,\max} \qquad (33)$$

If the MOSFETs and the transformer are chosen in such a way that C_{req} and L_r fulfill (33), the main MOSFET ZVS turn-on is achievable.

The previous analysis does not take into account the amount of energy consumed due to the secondary side body diodes conduction: indeed, their voltage drop is not zero and thus part of the current flowing through the primary leakage inductance is diverted into the secondary winding. This leads to possible lost of soft-switching if the condition (33) is not met with a sufficiently big margin. The use of secondary side Schottky diodes in parallel to MOSFETs reduces such degrading effect, thus allowing the use of transformers with smaller leakage inductance.

In order to evaluate the total energy storage of resonance inductance L_r from $t=t_0$ until $t=t_8$, an explicit expression for $i_{Lr}(t_8)$ (i_{Lr8} in the following) is required. An interesting analytical expression for i_{Lr8} can be obtained referring to [6]. In particular, during the LS FAC operations, sinusoidal current and voltage expressions are given for each one of the twelve linear stage assumed in the switching period T_s. By means of first order Taylor approximations of sinusoidal terms, simplified time dependent current and voltage expressions can be obtained: each one of them depends on the same quantity at the

previous time interval. So that, i_{Lr8} results a function of i_{Lr7}, and i_{Lr7} is a function of i_{Lr6}, and so on (where i_{Lrx} means i_{Lr} at $t=t_x$). Nevertheless, no analytical formula can be found for i_{Lr8}. Indeed, let us assume that:

$$k_{45} = i_{Lr4} / i_{Lr5} \tag{34.a}$$

$$\begin{aligned} Z_1 &= \sqrt{(L_m + L_r)/C_{req}}, \quad Z_2 = \sqrt{L_r/C_{req}} \\ Z_3 &= \sqrt{L_r/C_{cl}}, \qquad\qquad Z_4 = \sqrt{(L_m + L_r)/C_{cl}} \end{aligned} \tag{34.b}$$

$$v_{Creq}(t_3) = v_{Ccl}(t_3) = v_{Ccl}(t_7) = V_{in}/(1-D) \tag{34.c}$$

$$V_\pi = (DV_{in})/(1-D) \tag{34.d}$$

$$\begin{aligned} v_{Creq3in} &= v_{Creq}(t_3) - V_{in} = V_\pi \\ v_{Ccl3in} &= v_{Ccl}(t_3) - V_{in} = V_\pi \\ v_{Ccl7in} &= v_{Ccl}(t_7) - V_{in} = V_\pi \end{aligned} \tag{34.e}$$

$$i_T = i_{Lr8} + \frac{V_{in} D}{f_s L_m} \tag{34.f}$$

$$i_T{}' = i_T + \frac{I_{on}}{N} \tag{34.g}$$

$$i_T{}'' = i_T{}' - \frac{V_{Creq3in}^2}{2 Z_2^2 i_T{}'} \tag{34.h}$$

The resulting value of i_{Lr8} value can be found by searching the zeros of (35):

$$i_{Lr8} - \frac{V_\pi^2 Z_4}{Z_1{}^2 \sqrt{2K_T(V_\pi + K_T)}} - \frac{\sqrt{2K_T(V_\pi + K_T)}}{Z_4} = 0 \tag{35}$$

where Z_1, Z_4 and K_T themselves are i_{Lr8} dependent, with K_T given by (36)-(39):

$$K_T\left(i_{Lr8}\right) = K_{T1} + K_{T2} + K_{T3} \tag{36}$$

$$K_{T1}\left(i_{Lr8}\right) = \frac{Z_3^2\left(k i_T - i_T'\right) i_T'' - v_{Ccl3in}^2}{v_{Ccl3in}} \tag{37}$$

$$K_{T2}\left(i_{Lr8}\right) = \frac{Z_3^2 (k_{45} - 1) k_{45}\ i_T^2}{K_{T1}} \tag{38}$$

$$K_{T3}\left(i_{Lr8}\right) = \frac{Z_4^2\ i_T^2}{K_{T1} + K_{T2}} \tag{39}$$

Given the converter operating conditions, and fixed all the parasitic parameters, the current i_{Lr8} can be evaluated. In Figure 5.6 a ZVS compliance boundary curve, obtained according to inequality (33) by means of *Netwon-Raphson* method, is shown. For each couples (C_{req}, L_r), the non linear equation (35) has been solved by using as guess value for i_{Lr8} the last one calculated for the previous couple (C_{req}, L_r). The up-side (down-side) area in plane C_r-L_r of Figure 5.6 corresponds to the couples couple (C_{req}, L_r) verifying (not verifying) the inequality (33) and assuring (not assuring) main MOSFET ZVS commutations.

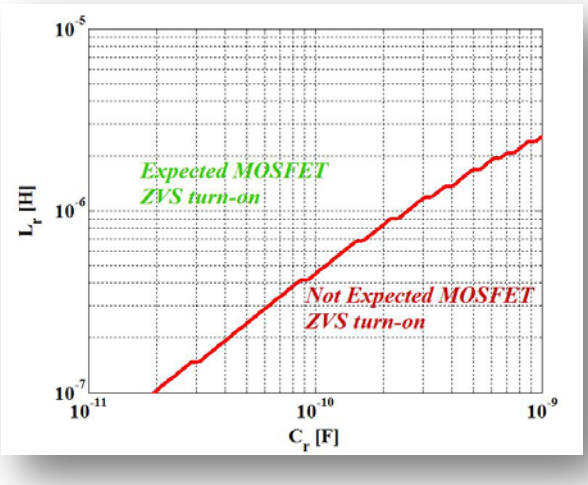


Figure 5.6 ZVS compliance boundary curve.

Next section illustrates an example of application of the ZVS compliance boundary curve, including the comparison of simulation results, obtained by applying both at primary side and secondary side MOSFETs the switching cell model described in Chapter 4, with experimental measurements.

5.4 Example of ZVS verification

The analysis presented in the previous section has been adopted to investigate the soft-switching behavior of the main and auxiliary MOSFETs in the UCC2897A Texas Instruments Evaluation Module (EVM) [27] of Figure 5.7, which is a *48V* to *3.3V* current mode controlled LS FAC.

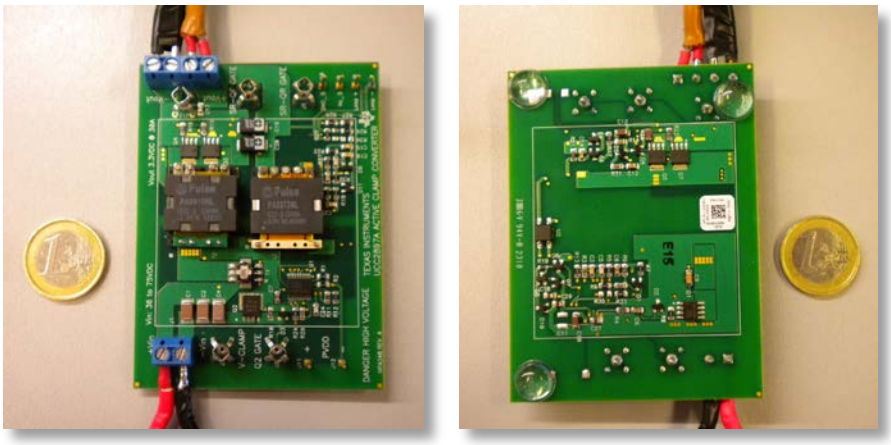
The EVM specifications are summarized in the following:

- V_{in}*=36V÷72V*; V_{out}*=3.3V*; I_{out}*=0÷30A*; f_s=225÷265*kHz*.

In Figure 5.8 the efficiency profile of the EVM is shown, for V_i*=48V* and I_o*=10A÷26A*: the maximum efficiency value reaches 93% at I_o≈16A. Therefore, the following analysis and tests have been done with V_i*=48V*, V_o*=3.3V*, I_o*=16A*, f_s*=250kHz*.

Main and auxiliary MOSFET gate-to-source v_{gs} and drain-to-source v_{ds} have been measured on the UCC2897A EVM. The oscilloscope screenshots are shown in Figure 5.9 and Figure 5.10.

In Figure 5.10(a) it is possible to observe the lack of ZVS turn-on of the main MOSFET: voltage $v_{ds,Q1}$ is still high, while $v_{gs,Q1}$ is already rising. The measured dead-time value is around *80ns*: this value is quite critical, as a wrong setup of this parameter would impede the ZVS operation. In fact, in this measurement, the dead-time value is too short. Even longer dead-time would not lead to main MOSFET ZVS turn-on, as in the first part of the commutation the $v_{ds,Q1}$ slope is too low (see Figure 5.10(a)) because of too small leakage inductance. In Figure 5.10(b), instead, the ZVS turn-on of the auxiliary MOSFET is achieved: voltage $v_{ds,Q2}$ is practically at *0V* because of its own body diode conduction; therefore $v_{gs,Q2}$ can rise with a negligible $v_{ds,Q2}$ value.



(a) **(b)**

Figure 5.7 UCC2897A Texas Instruments EVM: top layer (a) and bottom layer (b).

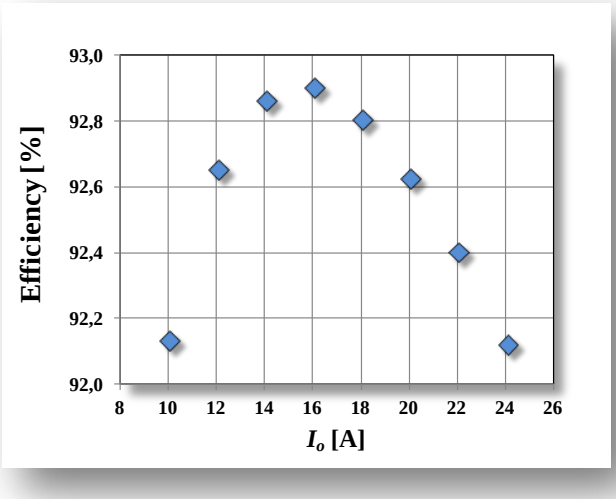


Figure 5.8 UCC2897A Texas Instruments EVM Efficiency.

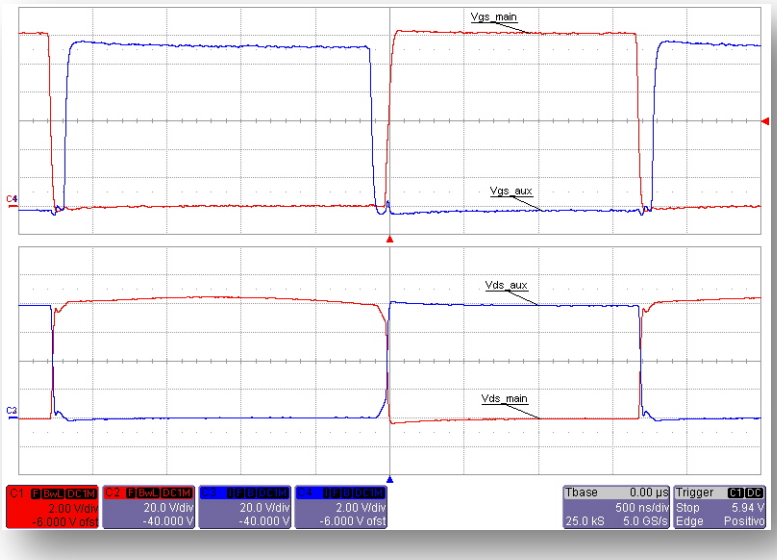
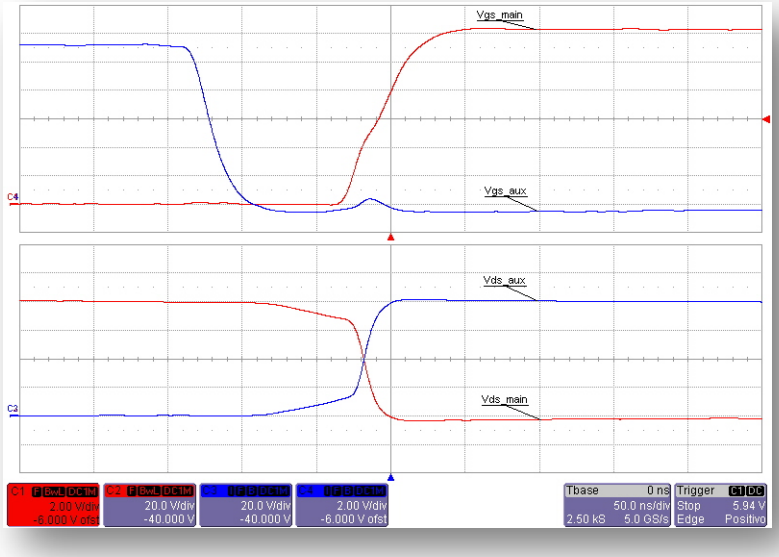
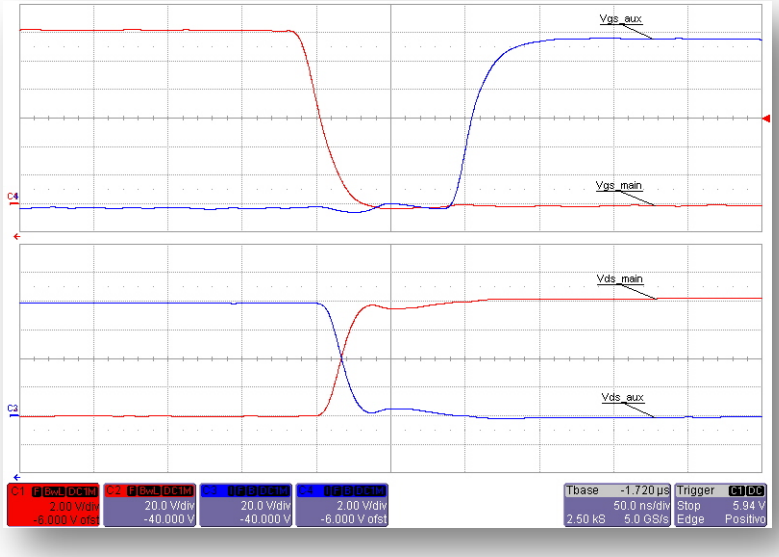


Figure 5.9 Experimental measurement on UCC2897A EVM. Top: Q_1 gate-to-source (red) and Q_2 source-to-gate (blue) voltages. Bottom: Q_1 drain-to-source (red) and Q_2 source-to-drain (blue) voltages.



(a)



(b)

Figure 5.10 Experimental measurement on UCC2897A EVM (See Caption of Figure 5.9): voltages waveforms during Q_2 turning-off and Q_1 turning-on interval commutation (a); voltages waveforms during Q_1 turning-off and Q_2 turning-on interval commutation (b).

Given the operating conditions and parameters values of the UCC2897A EVM devices, let evaluate the ZVS mapping presented in previous section according to inequality (33). In Figure 5.11 the ZVS compliance boundary curve is shown for the given case study. In particular, the leakage inductance value of the Pulse PA0810 transformer mounted on the EVM is of *0.65μH*. From the $C_{oss,Q1}$ and $C_{oss,Q2}$ capacitance values of main MOSFET (Vishay Si7846DP [28]) and auxiliary MOSFET (IR IRF6216PBF [29]), resonance equivalent capacitance C_{req} has been estimated in about *195pF*. This couple of values (C_{req}, L_r) has been represented as a blue square marker in the plane C_{req}-L_r of Figure 5.11. From the ZVS compliance boundary curve, the marker falls in red area of the plane C_{req}-L_r: this means that the resulting current i_{Lr8} does not verify inequality (33). Thus, main MOSFET ZVS turn-on results to be not achievable, which is in agreement with experimental verifications.

Let now introduce in series at the primary side of the transformer an external inductor L_{ext}. Hence the resulting equivalent resonance inductance becomes $L_{req}=L_r+L_{ext}$.

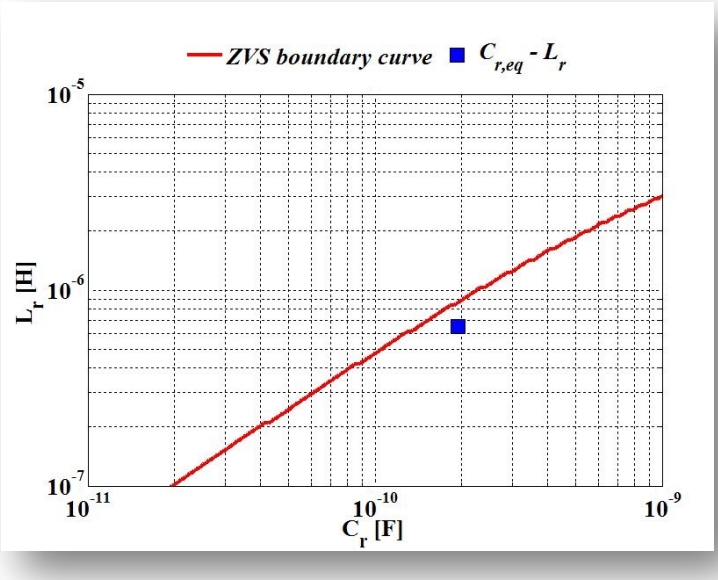


Figure 5.11 ZVS compliance boundary curve for the given case study.

According to ZVS mapping of Figure 5.11, a desirable additional inductance value should be *2.2μH*, with a resulting L_{req} of *2.85μH*. The modified EVM with the additional inductor L_{ext} is shown in Figure 5.12.

Main and auxiliary MOSFET gate-to-source v_{gs} and drain-to-source v_{ds} have been measured again on the UCC2897A EVM. In Figure 5.13 it is possible to observe the lack of ZVS turn-on of the main MOSFET: voltage $v_{ds,Q1}$ is still high (even if lower, with respect to previous measurement), while $v_{gs,Q1}$ is already rising. In Figure 5.14 the same waveforms measurement are shown with a L_{ext}=*4.7μH*. In both cases, a greater dead-time value will not assure main MOSFET ZVS turn-on: in fact, the $v_{ds,Q1}$ reaches a mean value *plateau*, from which the waveform moves only after the beginning of gate-to-source $v_{gs,Q1}$ rise.

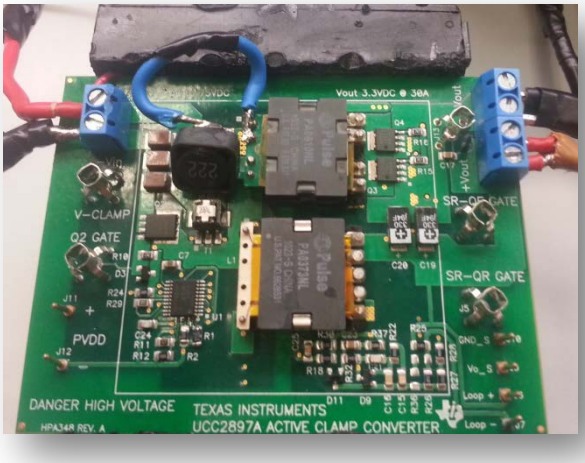


Figure 5.12 Modified UCC2897A EVM with additional inductor L_{ext}.

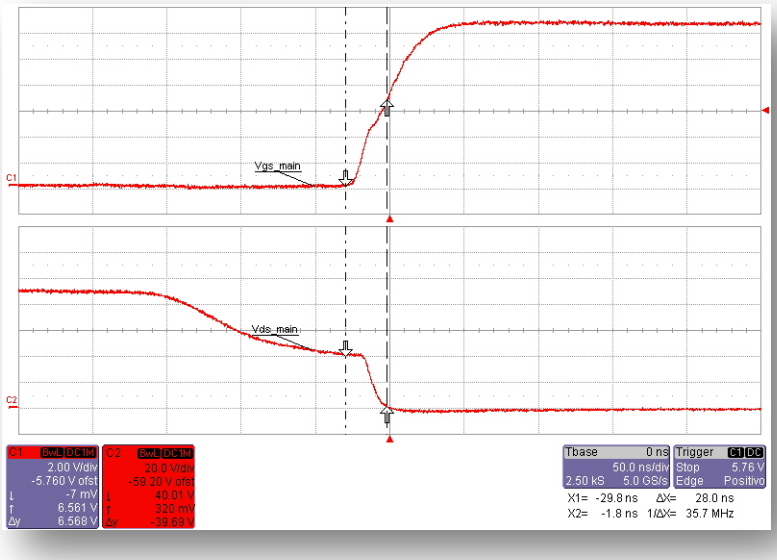


Figure 5.13 Experimental measurement on modified UCC2897A EVM with $L_{ext}=2.2\mu H$. Main gate-to-source voltage (top) and drain-to-source voltage at Q_1 turning-on.

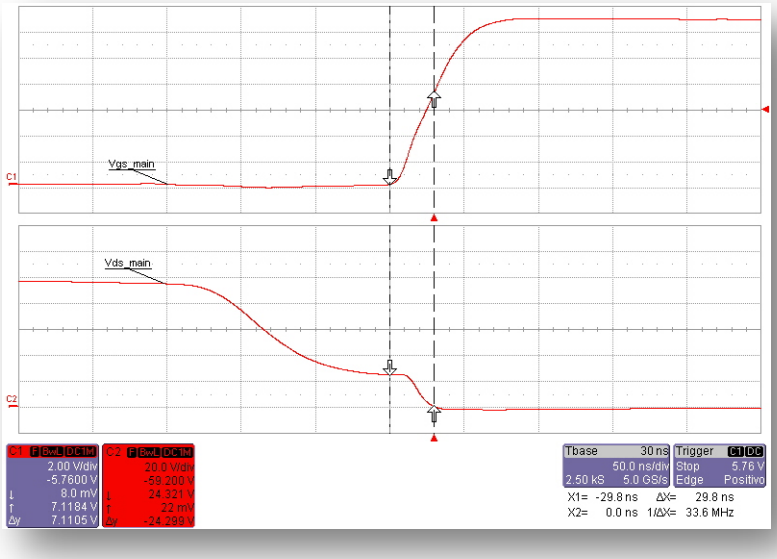


Figure 5.14 Experimental measurement on modified UCC2897A EVM with $L_{ext}=4.7\mu H$. Main gate-to-source voltage (top) and drain-to-source voltage at Q_1 turning-on.

Finally, a additional inductance value of $6.8\mu H$ has been selected, with a resulting L_{req} of $7.45\mu H$. The corresponding main and auxiliary MOSFET gate-to-source v_{gs} and drain-to-source v_{ds} have been reported in Figure 5.15. During the commutation of interest, the voltage $v_{ds,Q1}$ falls and reaches about $25V$, while $v_{gs,Q1}$ is starting to rise. In this case, thanks to the higher $v_{ds,Q1}$ slope, an increase in the defined dead-time (initially, fixed at $80ns$) of the converter may assure a complete achievement of main MOSFET ZVS turn-on, like shown in Figure 5.16, where a dead-time of $150ns$ has been adopted.

For $V_i=48V$, $I_o=16A$ and $L_r+L_{ext}=7.45\mu H$ the new efficiency profile of the modified EVM is of course much lower than the initial case study. Indeed, in addition to the ohmic and core losses of the additional inductance, the higher resonance inductance value also leads to a higher duty-cycle value, which impacts on stresses and conduction losses of silicon devices. Moreover, the dead-time impacts on the auxiliary body diode conduction losses too, so that, during the ZSV turn-on of the P-channel MOSFET, its own body diode is going to conduct for a longer time.

One main question arises: why a so big L_r+L_{ext} inductance is necessary to achieve ZVS although, accordingly to previous analysis, a small increase of the leakage inductance should verify the main ZVS turn-on?

To answer this question, a more detailed analysis of the circuit configuration during the resonant stage would be needed. In fact, while the secondary MOSFETs body diodes are conducting, their voltage is not zero and it is reflected to primary side, thus resulting in a not zeros voltage across the primary magnetizing inductance of the transformer during the interval of interest. This yields a more involved analysis of the resonant stage, which is out of the goals of the dissertation. Indeed, what is of interest here is to verify the possibility of achieving the numerical analysis of the FAC converter by using the model already described above in Chapter 4. A complete loss-based model for the FAC ZVS evaluation condition shall be the object of future investigation.

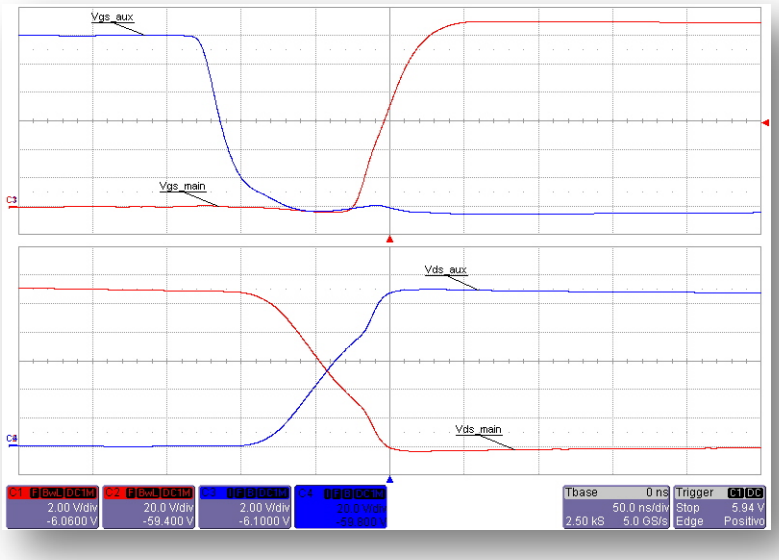


Figure 5.15 Experimental measurement on modified UCC2897A EVM with L_{ext}=6.8μH (See Caption of Figure 5.9): voltages waveforms during Q_2 turning-off and Q_1 turning-on interval commutation with dead-time set-up of *80ns*.

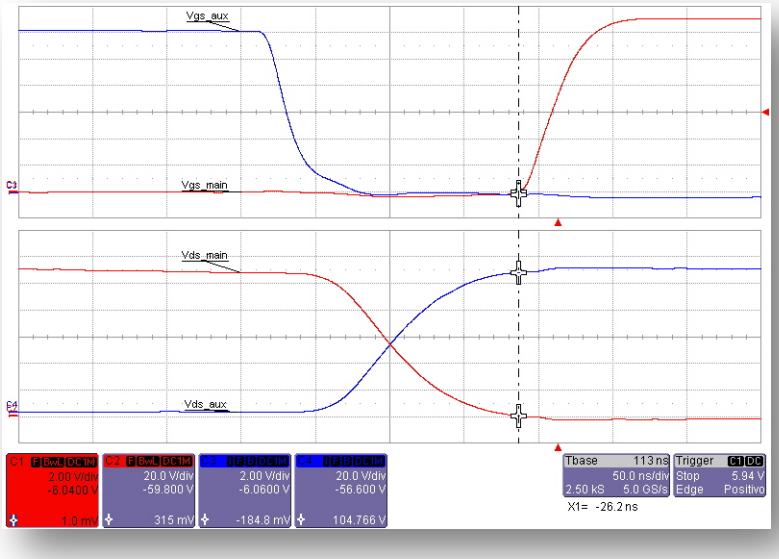


Figure 5.16 Experimental measurement on modified UCC2897A EVM with L_{ext}=6.8μH (See Caption of Figure 5.9): voltages waveforms during Q_2 turning-off and Q_1 turning-on interval commutation with dead-time set-up of *150ns*.

5.4.1 Simulations *vs* Experimental Measurements

The capability of the model adopted for the switching cell to treat MOSFETs commutations can be profitably exploited in the search of MOSFETs and transformers couples, whose parasitic capacitances and leakage inductances, respectively, combine in such a way to ensure soft switching and total losses minimization in isolated converter topologies. In this section, it will be shown how the model proposed in Chapter 4 can be also adopted for the high-current dc-dc FAC chosen in this Chapter as case study.

Moreover, in order to demonstrate the versatility of the model, its implementation has been realized as through MATLAB® coding as by means of a Micro-Cap[2] circuit simulation [30], where function sources allow to model instantaneous non linear behavior of devices. In particular, Micro-Cap sources can be mathematical function of any other circuit variable, such as a node voltage or a device current, and expressions can also be used for resistors, capacitors, and inductors values. In Figure 5.17 the Micro-Cap schematic circuit of the LS-FAC is given. In this schematic a mathematical function describes the current source behavior of each MOSFETs channel and voltages dependent functions are adopted for the parasitic capacitances of MOSFETs (see Equations (3) and (6) in Chapter 4).

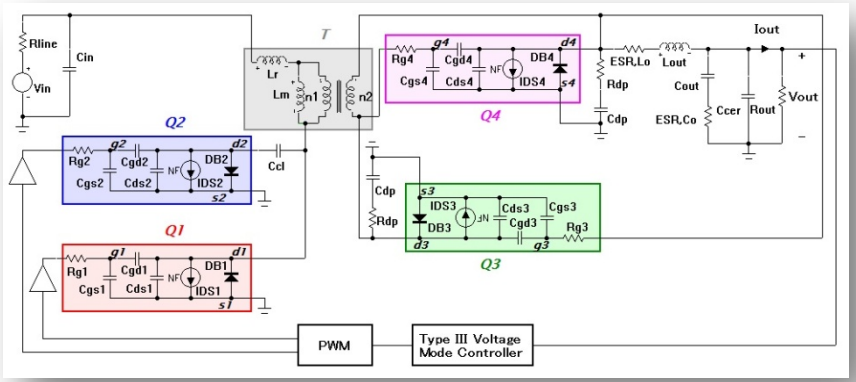


Figure 5.17 LS-FAC Micro-Cap schematic circuit.

[2]The Spectrum Software Micro-Cap is an integrated schematic editor and mixed analog / digital simulator that provides an interactive sketch and simulate environment for electronics engineers.

According to the UCC2897A Texas Instruments EVM, the following parameters have been adopted:

- $V_{in}=48V$; $V_{out}=3.3V$; $I_{out}=16A$; $f_s=250kHz$; $D=0.45$; $R_{line}=1m\Omega$; *dead-time=80ns*;
- $C_{cl}=33nF$; $C_{in}=6.6\mu F$; $C_{out}=660\mu F$; $ESR_{Co}=4.5m\Omega$; $C_{cer}=0.1\mu F$;
- $L_{out}=2\mu H$; $ESR_{Lo}=2.5m\Omega$; $L_r=0.68\mu H$; $L_m=86.3\mu H$; $n_1=6$; $n_2=1$;
- $V_{drive(Q1,Q2)}=\pm 12V$; $C_{dp}=470pF$; $R_{dp}=10\Omega$;
- Q_1: $R_{g1}=R_{g1,int}+R_{g1,ext}$; $R_{g1,int}=0.85\Omega$; $R_{g1,ext}=2.21\Omega$; $\beta_1=2.0$A/V^2; $V_{th1}=4.1V$; $\lambda_1=10^{-3}V^{-1}$;
- Q_2: $R_{g2}=R_{g2,int}+R_{g2,ext}$; $R_{g2,int}=5.55\Omega$; $R_{g2,ext}=2.21\Omega$; $\beta_2=2.6$A/V^2; $V_{th2}=-4.82V$; $\lambda_2=10^{-3}V^{-1}$;
- Q_3: $R_{g3}=R_{g3,int}+R_{g3,ext}$; $R_{g3,int}=0.55\Omega$; $R_{g3,ext}=1.1\Omega$; $\beta_3=83.3$A/V^2; $V_{th3}=1.61V$; $\lambda_3=10^{-3}V^{-1}$;
- Q_4: $R_{g4}=R_{g4,int}+R_{g4,ext}$; $R_{g4,int}=0.55\Omega$; $R_{g4,ext}=1.1\Omega$; $\beta_4=83.3$A/V^2; $V_{th4}=1.61V$; $\lambda_4=10^{-3}V^{-1}$;

In Figure 5.18 the experimental waveforms (dash-dot lines) and the Micro-Cap simulated waveforms (solid lines) are compared. The simulated waveforms confirm the lack of ZVS turn-on of the main MOSFET, in agreement with experimental verifications.

Of course, as already pointed out above, it cannot be expected to obtain a perfect matching between the two kind of waveforms, for several reasons, mainly due to the insufficient information given in devices datasheets (both for silicon and for magnetic devices):

- devices are characterized only for one/two main operating conditions and for one/two given temperature values; thus, for example, the same MOSFET may work with different driver voltage levels, but have a quite complete characterization just for one specific driver voltage value;
- sometimes, only *typical* values of devices parameters are given, as in case of threshold voltages or trans-conductance values for MOSFETs. Let consider that the typical value of a MOSFET threshold voltage is usually affected by a large uncertainty;

- gate drives pull-up and pull-down resistances are often badly characterized in the switcher ICs datasheet, and nominal values of this parameters that are often largely underestimated with respect to effective values in many cases;
- sometimes, power device parameter are available only in graphical format, like for the MOSFETs parasitic capacitances and for temperature dependent core loss density functions;
- sometimes, only *maximum* values of certain parameters are given, as in case of the leakage inductance for the transformer;
- sometimes, parameters value are simply *neglected*, as in case of gate resistances or parasitic inductances for many SMD MOSFETs.

Moreover, in case of this simulation, the equivalent circuit schematic does not reproduce the real IC operations, and the control loop adopted for the LS-FAC simulation is substantially a voltage mode controlled regulator, just designed in order to achieve asymptotic stability of the converter.

Finally, let us also to remember that Micro-Cap works with its own numerical solver methods (in Micro-Cap 9.0, for example, Gear and Trapezoidal [31] methods are included). As discussed also for ODEs in Chapter 4, these numerical methods adopt internal time-steps definition: thus, they require preliminary set-up operations, without which convergence solutions might be not ensured.

What is important is that the numerical model adopted for the analysis is robust and allows to achieve reliable and quick simulations, if the values of all parameters are available. Indeed, in the case under study, despite all, experimental and simulated waveforms have the same profile and simulations agree with experiments on detecting the lack of main MOSFET ZVS turn-on.

Finally, let us to refer to the experimental verification with $L_r+L_{ext}=7.45\mu H$. In Figure 5.19 the experimental waveforms (dash-dot lines) and the Micro-Cap simulated waveforms (solid lines) are compared. Also for this case study, the matching between the experimental waveforms and the Micro-Cap simulated waveforms is satisfactory, as both show the achievement of main MOSFET ZVS turn on.

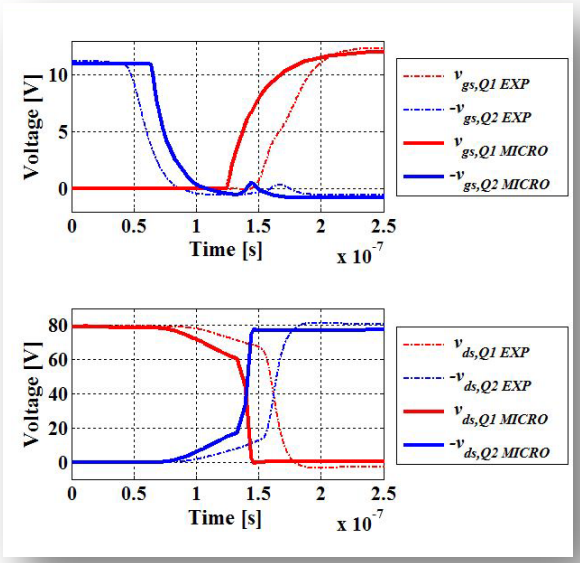


Figure 5.18 Experimental waveforms and Micro-Cap simulated waveforms (L_{ext}=0.68μH).

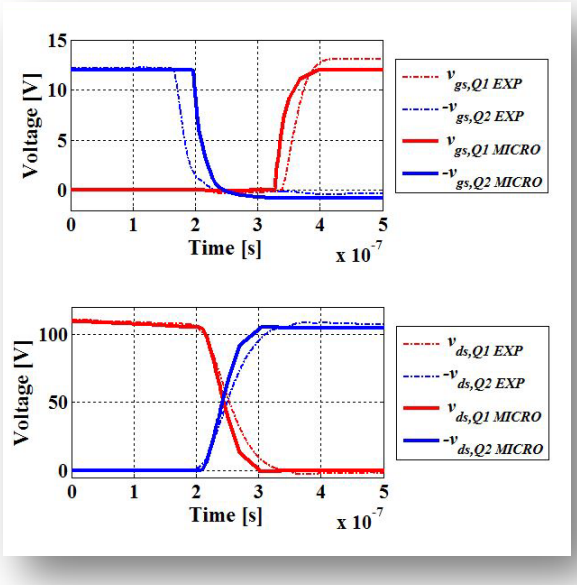


Figure 5.19 Experimental waveforms and Micro-Cap simulated waveforms (L_{ext}=6.8μH).

Similar considerations can be done by comparing the experimental waveforms (dash-dot lines) and the MATLAB® simulated waveforms (solid lines) given in Figure 5.20 and 5.21, and detecting the lack (Figure 5.20) or the achievements (Figure 5.21) of the main MOSFET ZVS turn on. In particular, in Figure 5.20 and 5.21 the MATLAB® simulated waveforms show a major agreement with the experimental ones: this has been possible by doing a more accurate tuning of the circuit parameters (e.g. gate driver resistances, leakage inductance, MOSFETs threshold voltages, ect.).

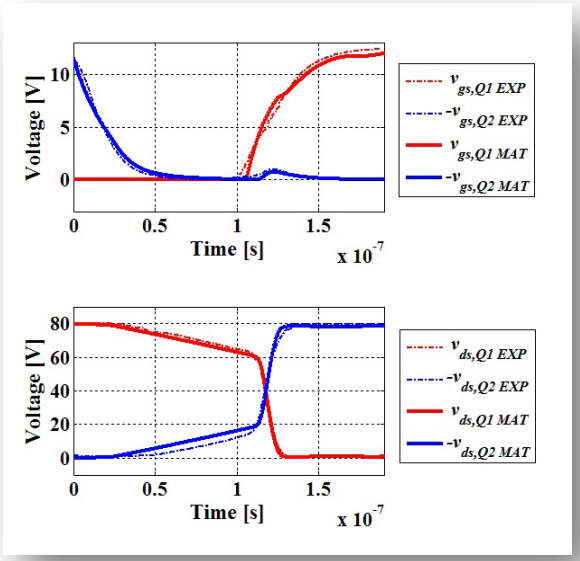


Figure 5.20 Experimental waveforms and MATLAB simulated waveforms (L_{ext}=0.68μH).

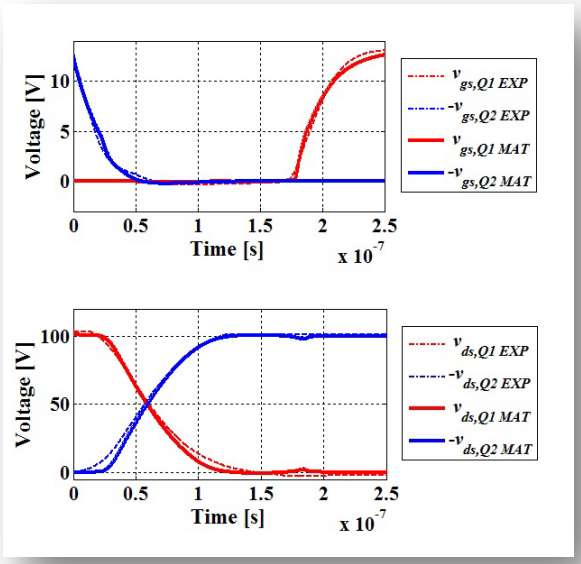


Figure 5.21 Experimental waveforms and MATLAB simulated waveforms (L_{ext}=6.8μH).

Comments

The model proposed for the switching cell to treat MOSFETs commutations, and adopted in the previous section for the analysis of a more involved isolated topology, can be used to test MOSFETs capacitive models, as well as to make the identification of other parasitic elements (e.g. leakage inductances) and specific operation of IC switchers influencing the MOSFETs commutations (e.g. dead-time set-up). The proposed model confirms its own robustness and reliability, working well both in MATLAB® code implementation and in circuit simulators, like Micro-Cap.

No detailed or complex devices models are required while the preliminary comparative evaluation among several possible design solutions is the goal on the analysis: indeed, silicon and magnetic devices *behavioral models* are sufficient, provided that a versatile and reliable numerical model is available, enabling system level analysis. In power design context, behavioral models are also the only ones to which a designer can refer to. Accordingly, worldwide power devices manufactures are now increasing the offer of on-line parts selectors and in some cases true design support tools (e.g. WEBENCH), thanks to which a designer can quickly discriminate and highlight different figure of merits among huge numbers of devices. Some manufactures are also improving datasheets information, including more interesting features for dynamic characteristics, like for example the equivalent fixed capacitance value that can give the same stored energy in a parasitic MOSFET capacitance during a commutation.

The model and methods investigated during the research whose results are illustrated in this dissertation, are specifically conceived to be adopted as computational core for WEB-based *investigation tools* for power designers, allowing them to quickly make comparisons among a great number of design solutions and devices.

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Conclusions and Future Works

Isolated power supplies design requires the achievement of overall stress, losses, cost, size and reliability trade-off. This problem is of considerable importance in modern applications of power converters, as for energy saving issues as for the achievement of high power density capabilities needed to integrate the power supply into the same boards where the system they feed is hosted.

Transformer design is the central issue in isolated switching power supplies design. Affording a preliminary reliable investigation of possible feasible power supply designs using off-the-shelf transformers can be of great help in reducing the time to prototyping and the time-to-market. Even though many off-the-shelf transformers are available today for standard applications, many special situations occur such that the design of a custom transformer is required. New design method are needed in order to enable a wider detection and investigation of possible transformer design solutions by means of a straightforward matching between the available magnetic cores, the operating conditions of the transformer to be designed and the design constraints to be fulfilled.

A critical re-examination of transformers design methods discussed in technical literature has been afforded to highlighting some common misleading assumptions which can hinder the minimization of the transformer. Thus, a new design approach has been investigated and discussed, which helps in easily identifying possible transformer solutions in critical custom designs for a given application, complying with losses and size constraints. The new method is aimed at quickly identifying possible combinations of magnetic cores and windings turns number when many possible design might be feasible and a fast comparative evaluation is needed for preliminary cores selection. Novel geometric form factors of magnetic core (K_f and K_c) have been introduced and a consequent classification procedure for magnetic cores has been obtained, showing the correlation between the characteristics of the core and the specific applications in which each

type of core offers major advantages in terms of minimizing losses and/or size.

A magneto-electro-thermal macro model of the transformer has been adopted in order to investigate the dependency of total transformer losses on the temperature and to analyze the temperature sensitivity of form factor constraints of magnetic cores for power loss compliance. In particular, temperature-dependent boundaries curves both for the core window area and cross-section and for the form factors Kf and Kc have been obtained, allowing quick identification of feasible design solutions, complying with all design constraints, included thermal issues.

Transformers and silicon devices do inextricably share the responsibility of major losses in isolated power supplies, and the optimization of the former normally impinges the one of the latter. As a consequence, the intimate correlation among these parts need to be jointly considered, regarding the way the characteristics of one device influence the losses of the other one. In order to achieve reliable comparative evaluations among different design set-up, a new versatile numerical model for commutations analysis of power MOSFETs has been developed. The model takes into account the non-linear behavior of the inter-electrode capacitances and has been conceived to work as with parameters and information contained in the devices datasheets as with more detailed models. A Modified Forward Euler (MFE) numerical technique has been specifically developed and adopted in the realization of a numerical algorithm which solves the non linear system of differential equations describing the effect of parasitic capacitances in whatever operating conditions, in order to overcome the limitation exhibited by ODEs techniques for stiff problems in this particular application. The new MFE technique allows to compare the switching characteristics of MOSFETs with a good level of reliability and to obtain a detailed analysis of capacitive currents paths circulating between MOSFETs in half-bridge configuration during commutations. The numerical device-level model of the MOSFETs couples has been first tested in the analysis of basic non isolated synchronous rectification buck converter and then used into an integrated model allowing the analysis of Active Clamp Forward converters. It has been also demonstrated that the model adopted for the switching cell can be implemented in circuit

simulators like Micro-Cap. The correlations existing between the parasitic parameters which characterize both transformer and MOSFETs and their impact on the switching behavior and the efficiency of such a conversion system can be effectively investigated by using such modeling approach, thus overcoming the limitations and unreliability of simplified analytical formulas for the prediction of the ZVS achievement. In particular, the integrated system model has been successfully used to determine the mutual constraint conditions between magnetic devices and solid state devices to achieve soft-switching, and their effects on the physical feasibility and design/selection of such power devices in order to achieve high efficiency.

Experimental activities have been done to validate the methods and models proposed, through the implementation of *on-line* losses measurements techniques for both magnetic and solid state devices. The high switching frequency, high slew rates, high current and low leakage devices make such measures extremely sensitive to the parasitic circuit layout parameters. In order to achieve reliable measurements, non-conventional measurement techniques have been investigated based on the use of current sensing MOSFETs, and applied in the development and implementation of new measuring circuits.

The overall body of models and methods investigated in this dissertation will be integrated with intelligent search algorithms and used as computational core for the future development of new WEB based isolated power supplies design tools.

Appendix A

Simplified models for switching losses evaluation

Switching power supplies designers mostly use simplified models for switching losses calculation presented in technical literature, including textbooks, papers and application notes [1]-[6]. Almost all simplified models are based on the assumption that the transition of the MOSFETs from the interdiction, through the saturation to the linear region, and vice-versa, is represented as a sequence of four different phases, each one taking a certain time, and the waveforms of drain-to-source current and voltage can be approximated as piece-wise linear functions over such intervals, as shown in Figure A1 and Figure A2.

Figure A1 shows a typical representation of hard commutation, occurring when the device turning ON exchanges the current with the body diode of the complementary device. Figure A2 shows a typical representation of soft commutation, occurring when the device turning ON exchanges the current with its own body diode. The plots of waveforms for turn OFF are merely obtained by mirroring the plots of Figures A1 and A2 with respect to vertical axes.

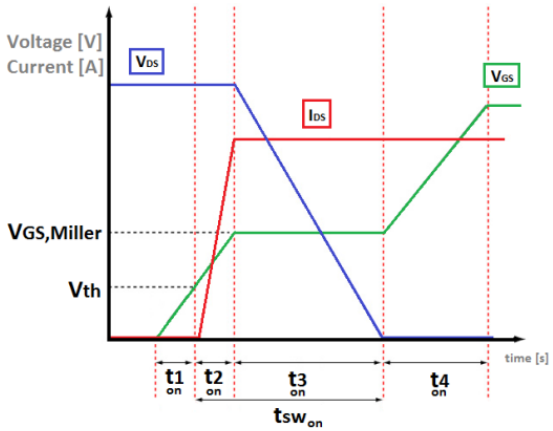

Figure A1. Hard turn-on typical waveform.

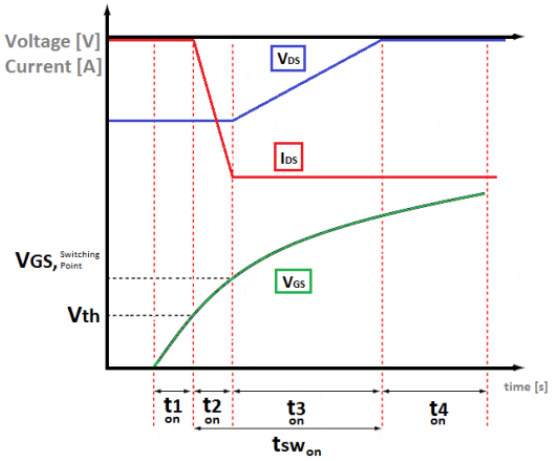

Figure A2. Soft turn-on typical waveform.

Simplified models share the following assumptions (see Figures A1 and A2):

1) the duration of the switching intervals is determined by assuming that the gate-to-source voltage is an exponential waveform, typical of linear time invariant RC circuits, except in Miller region, wherein it assumed to be flat;

2) the duration t_1 and t_2 of the first two intervals is determined by calculating the times where the exponential gate-to-source voltage crosses the threshold level V_{th} and switching point level $V_{sp}=V_{th}+I_{on}/g_{FS}$, where g_{FS} is the MOSFET trans-conductance,

using the product $R_g C_{iss}$ of the total gate resistance by the input capacitance as a time constant;

3) the duration of interval t_3 is obtained as the time required for the gate-drain voltage across the reverse capacitance C_{rss} drops off the V_{off} component under constant gate current due to Miller effect;

4) the duration of interval t_4 is obtained as the time required for the restarting exponential gate-to-source voltage reaches the gate-driver voltage;

5) the total switching losses are determined by calculating separately the following loss contributions:

   a. *overlapping*, obtained by applying elementary geometry rules to the drain-to-source voltage and current piece-wise linear waveforms in intervals t_2 and t_3 of Figures A1, A2:
      $\rightarrow \quad 0.5 V_{off} I_{on} (t_2 + t_3) f_s$
   b. *gate charge*, obtained as the product of the total gate charge by the gate driver voltage by the switching frequency:
      $\rightarrow \quad Q_g V_{dr} f_s$
   c. *output capacitance*, obtained as the energy stored in the output MOSFET capacitance when OFF multiplied by the switching frequency:
      $\rightarrow \quad 0.5 C_{oss} V_{off}^2 f_s$
   d. *dead-time*, obtained as the average power dissipated by the body-diode (or Schottky diode) while conducting during the dead times needed to avoid MOSFETs cross conduction:
      $\rightarrow \quad V_F I_{on} (t_{dtr} + t_{dtf}) f_s$
   e. *reverse recovery*, obtained as the average power loss caused by reverse recovery of the body-diode:
      $\rightarrow \quad Q_{RR} V_{dr} f_s$
   f. *Schottky diode* (used across LS MOSFET), obtained as the energy stored in the Schottky capacitance when LS MOSFET is OFF, multiplied by the switching frequency:
      $\rightarrow \quad 0.5 C_{Schottky} V_{off}^2 f_s$

Different assumptions characterize each simplified approach in describing the current rise and voltage fall times ($t_{2,on}$ and $t_{3,on}$) in the

turn on transition and the voltage rise and current fall times ($t_{2,off}$ and $t_{3,off}$) in the turn off transition. In [2] the total duration of the two intervals (t_2+t_3) is directly calculated as the time required for the total switching gate charge Q_{gsw}=0.5Q_{gs}+Q_{gd} is transferred to input and reverse capacitances C_{iss} and C_{rss}. In [3]-[6], instead, the durations of the two intervals t_2 and t_3 are determined separately: t_2 is calculated by considering the gate-to-source voltage exponential rise; t_3 is calculated as the time required for the gate-to-drain charge Q_{gd} is transferred to reverse capacitance C_{rss}. Another key point is the way the parameters are extracted from datasheets, where they are provided for given reference conditions. In [1]-[5] data regarding gate-to-source threshold voltage, charges, capacitances and trans-conductance are taken from datasheets tables for reference conditions and then adjusted by means of given scaling factors. In [6], instead, threshold voltage and trans-conductance are derived from the trans-characteristic curves I_{ds} vs V_{gs} in the saturation region, while capacitances are fixed at their values corresponding to the V_{off} voltage level. Moreover, while some authors [6] simply neglect switching losses of LS MOSFET, other ones [2] provide hints for their estimation. Some authors [6] ascribe output capacitance power loss to both HS and LS MOSFETs, whereas other ones [2] take them into account just for HS MOSFET. Simplified models normally analyze separately the losses of two MOSFETs of the synchronous couple, whereas during the commutations the two devices strongly interact, because of the crossed circulation of the currents through the body diodes, the channels and the capacitances. Using the different simplified models and parameters approximations may lead to much different switching time intervals and loss estimation.

Let us consider the case of a buck converter, whose operating parameters are: V_{in}=12V, V_{out}=3.3V, I_{out}=5A, f_s=300kHz, V_{dr}=5, $R_{dr,ON}$=3Ω, $R_{dr,OFF}$=2Ω. Figure A3 and Figure A4 show the HS MOSFET switching times calculated for various commercial MOSFETs. In particular, Figure A3 shows the $t_{sw,on}$=$t_{2,on}$+$t_{3,on}$ turn-on time, while Figure A4 shows the $t_{sw,off}$=$t_{2,off}$+$t_{3,off}$ turn-off time, both calculated using the formulas suggested in [1][2][3] and [6].
Evidently, a quite big difference affects the switching times and the resulting power loss predictions, depending on the simplification adopted. This may result in a serious impact on the reliability of

power devices selection, on the correct determination of maximum operable switching frequency and on the true achievement of high energy-efficiency and high power-density design goals.

The key problem in the design of high-efficiency high-power-density power supplies is to find a trade-off between MOSFETs *accurate physical models*, providing reliable losses predictions at the price of onerous simulations, and MOSFETs *approximated behavioral models*, providing quick losses prediction at the price of unpredictable reliability. Using PSPICE simulation is not practical for quick comparative tests among numerous couples of commercial devices, as well as it is not safe, for the same purposes, doing calculations based on simplified models yielding rough losses estimation. The main source of complexity in switching loss calculation is due to the non linearity of MOSFETs capacitances and of the channel and body diode currents with respect to the $v_{ds}(t)$ and $v_{gs}(t)$ voltages. The dependence of MOSFETs physical parameters, in particular of capacitances, on the terminal voltages, is approximately accounted for in some simplified models [1][3]. A more complete yet simplified representation is proposed in [7][8], where a physical analysis of charge location during switching transitions has been adopted to achieve a practical characterization of FETs model, according to an accurate description of the inter-electrodes capacitances. The use of detailed models assumes the knowledge of some specific physical parameters of commercial components, which are not available in datasheets, and which should be necessarily measured in switching operation.

The modeling and computation approach presented in this dissertation (see Chapter 4) are aimed at providing reliable switching loss evaluation with sustainable complexity and computing times.

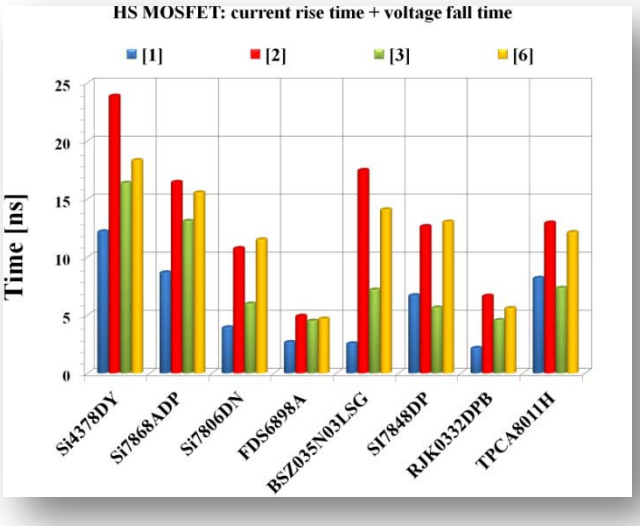

Figure A3. HS MOSFET switching time: turn-on.

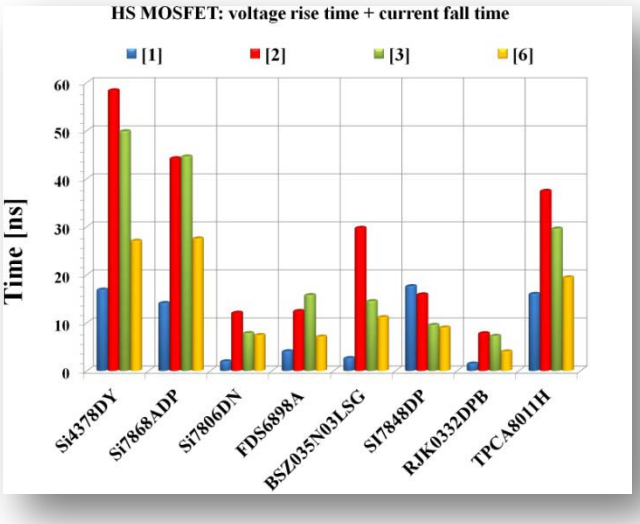

Figure A4. HS MOSFET switching time: turn-off.

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List of Symbols

A_c [m^2]	core cross-section area
W_A [m^2]	core window area for windings
L_m [m]	core magnetic path length
L_{MLT} [m]	core mean length per turn of windings
f_s [Hz]	switching frequency
B_{dc} [T]	dc component of core magnetic flux density
B_{ac} [T]	ac component of core magnetic flux density
β, K_{fe} [$Wm^{-2}T^{-\beta}$]	parameters of the core material
K_u	core window area utilization factor
W_{Au} [m^2] = $W_A K_u$	net core window area
A_{wj} [m^2]	cross-sectional area of the j-th winding
α_j	fraction of W_{Au} allocated to the j-th winding
I_j,I_{jrms} [A]	dc and rms output current of the j-th output
I_{tot} [A]	total equivalent rms windings current
D	PWM duty-cycle of converter main switch
$M(D)$	conversion ratio of the converter
n_0	primary winding turns number
ρ [Ωm]	copper resistivity
α_T	copper temperature coefficient
T_{Fe} [°C]	magnetic core temperature

T_{Cu} [°C]	windings temperature
$R_{\vartheta\_v,Fe}$, $R_{\vartheta\_h,Fe}$ [K/W]	core-ambient thermal resistances transferring heat by convection for vertical and horizontal surface of the magnetic core
$h_{v,Fe,}$ $h_{h,Fe}$ [W/m^{2}K]	core vertical and horizontal convection heat transfer coefficients
$A_{v,Fe,}$ $A_{h,Fe}$ [m^2]	total areas of the vertically and horizontally oriented open surfaces of the core
h_{Cu} [W/m^{2}K]	windings convection heat transfer coefficient
A_{Cu} [m^2]	area of the open surface of the windings
K_{Cu}[W/mK]	windings thermal conductivity
K_{cf} [W/mK]	coil former thermal conductivity
r_w [m]	mean radius of the windings
r_{cf} [m]	radius of the coil former
Δ_f [m]	coil former thickness;
h_w [m]	windings height
h_{cf} [m]	coil former height
LS, HS	Low Side**,** High Side
LSM, HSM	LS MOSFET**,** HS MOSFET
v_g [V]	gate voltage
v_{gd} [V]	gate-drain voltage
v_{gs} [V]	gate-source voltage
v_{ds} [V]	drain-source voltage
V_{dr} [V]	driver voltage
V_{th} [V]	threshold voltage

V_T [V]	body-diode thermal voltage
R_{gdx} [Ω]	gate driver resistance
R_{gi} [Ω]	gate internal resistance
i_g [A]	gate current
I_{DS} [A]	channel current
i_{ds} [A]	drain-source current
I_μ [A]	saturation current
i_d [A]	body-diode current
V_{off} [V]	input voltage
R_{off} [Ω]	input line resistance
i_{off} [A]	input current
I_{on} [A]	output current average value
β_x [A/V^2]	transconductance
Λ [V^{-1}]	channel-length modulation
i_{Cds} [A]	drain source capacitance current
i_{Cgd} [A]	gate drain capacitance current
i_{Cgs} [A]	gate source capacitance current
C_{ds} [F]	drain source capacitance
C_{gd} [F]	gate drain capacitance
C_{gs} [F]	gate source capacitance
i_{Cds} [A]	drain source capacitance current
i_{Cgd} [A]	gate drain capacitance current
i_{Cgs} [A]	gate-source capacitance current

C_{ds} [F]	drain-source capacitance
C_{gd} [F]	gate-drain capacitance
C_{gs} [F]	gate-source capacitance
C_{iss} [F]	input capacitance
C_{oss} [F]	output capacitance
C_{rss} [F]	transfer capacitance
Q_{gs} [C]	gate -source charge
Q_{gd} [C]	gate-drain charge
Q_{ds} [C]	drain-source charge
s_{Vds}	sign of voltage v_{ds}

List of Publications

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1) De Nardo, A.; Di Capua, G.; Femia, N.; "*Transformer Design for Isolated Switching Converters Based on Geometric Form Factors of Magnetic Cores*", IEEE Transaction on Industrial Electronics, vol. 60, no. 6, pp. 2158-2166, 2013.

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International Conference Proceedings

[1] De Nardo A.; Di Capua, G., Femia, N.; Zamboni W.; "*A Fast Analytical Method to Predict DC Operating Point of DC-DC Switching Regulators in Discontinuous Conduction Mode*", accepted at 2013 PCIM Europe, Nuremberg, Germany.

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