ABSTRACT

The organic electronic devices are finding a great consideration for applications where silicon limitations make this semiconductor unsuitable. Many properties of organic materials open new frontiers of the research; some example of applications are flexible displays, smart textiles, new lighting fixtures, intelligent packaging. Furthermore, an interesting attraction of organic devices is their being environmentally friendly. Organic materials provide also an inspiration for always new applications stimulated by the continuing efforts of characterization, fabrication, synthesis and design.

This thesis work wants to contribute to the comprehension of the properties of solution processed organic thin film transistors (OTFTs) that use a n-type semiconductor. These devices are the basic element of the driving circuits, where the n channel transistors still result poorly understood. In this PhD activity, it is studied the effect of surface treatments at SiO_2 dielectric layer and organic semiconductor interface to improve the OTFTs performance. These transistors, that are fabricated employing a specific combination of treatments before the deposition of a soluble semiconductor, are studied in order to analyze the relationship between the surface treatments and the devices electrical parameters; so to calculate one or more variables able to better adapt the conditions of the treatments to the performances of the device.

The devices are fabricated using as semiconductor the [6,6]-phenyl-C71-butyric acid methyl ester ($PC_{70}BM$) deposited from drop casting technique on a SiO_2 layer where a combination of ultraviolet/ozone cleaning (UV/O_3) and self-assembled monolayer (SAM) coating is previously carried out. The hexamethyldisilazane (HMDS) is the SAM used, and it is deposited at three different temperatures, 7°C, 25°C and 60°C. UV/O_3 cleaning allows to remove organic contaminations on the dielectric surface, thanks to the formation of hydroxyl groups (-OH) generated by the UV/O_3 ambient. While the HMDS can reduce the traps induced by Si-OH groups on the gate insulators, making layer treated hydrophobic. In this work, it is observed that different deposition temperatures of the SAM produce surfaces with different hydrophobic characters resulting in different electric performances of the devices.

The techniques of analysis employed to observe the effects of the treatments have been: contact angle measurements, AFM imaging of the organic semiconductor, *I vs. V* static characterization and admittance measurements.

Particular effort is given to evaluate the presence of electronic trap states in organic thin film transistors based on n-type semiconductor in bottom-gate bottom-contact configuration, thus it is proposed a new and accurate equivalent electrical, which is capable to model the properties of the semiconductor bulk and the conductive channel, through the calculation of the density of the trap states and the channel resistance.

From the performed analysis, the transistors treated at temperature of 25°C show a high roughness, a very inhomogeneous surface of the semiconductor layer and a higher degree of the SiO_2 surface hydrophobicity compared to the transistors processed at 7°C and 60°C. The HMDS behaving as a silane coupling reactant, provides a better tailored hydrophobic surface during the processes at 7°C and at 60°C, resulting in an improved surface energy, matching between the gate insulator and the organic semiconductor.

From DC measurements, it is observed that the samples at 60°C temperature for HMDS deposition show the best performances: the highest electron mobility of $13 \cdot 10^{-3}$ cm^2/Vs and the lowest threshold voltage of 12.0 V. While for the devices prepared at 7 °C and at 25 °C, the values of the mobility and the threshold voltage are $7.6 \cdot 10^{-3}$ cm^2/Vs - 13.6 V, and $2.8 \cdot 10^{-3}$ cm^2/Vs - 17.8 V, respectively.

The densities of the resulting trap states, calculated by admittance measurements and equivalent circuit, show the minimum quantity of the traps for the devices treated at 60°C compared to other devices, with a value of 1.48 10^{16} cm^{-3} eV^{-1}.

In conclusion, in this thesis it has been studied the effect of the deposition processing of HDMS layers on the behavior of $PC_{70}BM$ bottom-gate bottom-contacts OTFTs. In particular, the temperature of the HMDS process influences the quality of the semiconductor films and the devices performances. The hydrophobicity of the dielectric surface, induced by the HDMS process at 60°C, measured trough the value of the contact angle, which is of the order of 104.1° for this process, results in the formation of the highest quality of the $PC_{70}BM$ films, with homogeneous layers and a reduced quantity of traps, giving the OTFTs with the best performances. This results have allowed to develop a new equivalent electrical circuit, which, for the first time, models the AC behavior of bottom-gate bottom-contacts OTFTs with n-type semiconductors.