Abstract of the thesis

The main aim of the present research work is to project and develop very large scale electronic integrated circuits, with particular attention to the ones devoted to image processing applications and the related topics. In particular, the candidate has mainly investigated four topics, detailed in the following.

First, the candidate has developed a novel multiplier circuit capable of obtaining floating point (FP32) results, given as inputs an integer value from a fixed integer range and a set of fixed point (FI) values. The result has been accomplished exploiting a series of theorems and results on a number theory problem, known as Bachet's problem, which allows the development of a new Distributed Arithmetic (DA) based on 3's partitions. This kind of application results very fit for filtering applications working on an integer fixed input range, such in image processing applications, in which the pixels are coded on 8 bits per channel. In fact, in these applications the main problem is related to the high area and power consumption due to the presence of many Multiply and Accumulate (MAC) units, also compromising real-time requirements due to the complexity of FP32 operations. For these reasons, FI implementations are usually preferred, at the cost of lower accuracies. The results for the single multiplier and for a filter of dimensions 3x3 show respectively delay of 2.456 ns and 4.7 ns on FPGA platform and 2.18 ns and 4.426 ns on 90nm std_cell TSMC 90 nm implementation. Comparisons with state-of-the-art FP32 multipliers show a speed increase of up to 94.7% and an area reduction of 69.3% on FPGA platform.

Then, starting from this background on image filter theory, the candidate examined and improved the filtering stages of an inverse Tone Mapping (iTM) architecture, for the conversion of Low Dynamic Range (LDR) frames into High Dynamic Range (HDR) ones. This kind of operation is considered a computational intensive one, due to the high number of arithmetic operations involved. The proposed structure represents the first hardware design capable of performing iTM on images of different resolutions, from Digital8 (500x480 pixels) format up to 4K UHDTV (3840x2160 pixels) one. Hence, compared to the first architecture developed by the same research group, the new design results more fit for systems acquiring images at different resolutions, while not degrading its power consumption and area occupation performances. This is accomplished through a careful organization of the partial data transfer and storage in the dedicated memory structures of the design. The main drawback, due the additional logic required to implement the multiresolution feature, is represented by the increase of13.22% and 11.08% in the data arrival time, for the FPGA and std_cell TSMC 90 nm implementations respectively. Nevertheless, this is sufficient for real-time applications on frames up to Full-HD (1920x1080 pixels) resolution.

From considerations on the data transferring and storage in memories, the candidate has been interested in the study and the development of sense amplifier bit-line circuits for SRAMs, in order to obtain better performances of the memories in terms of overall speed and tolerance issues. The main problem in this case is the increase of the offset voltage, VOS, generated by the mismatch among the components of the sensing circuitry, which tends to worsen due to MOSFETs' scaling. The solution proposed is the development of a new voltage sense amplifier for the reading of a 6T memory cell, while several load cases have been considered to take into account the different number of cells that could be instantiated along a single bit-line. The design has been implemented using both TSMC 90nm and in TSMC 180nm technologies. The proposed sensing scheme uses a higher number of CMOS if compared to other schemes, but achieves a lower area occupation nonetheless, due to the dimensions of the required devices. Moreover, it shows halved sensing

delays and it is capable of rejecting an offset voltage more than doubled when compared to the state-of-the-art.

Then a further period has been dedicated to further image and video filtering applications. In particular, the candidate developed a hardware accelerator dedicated to edge detection using Gabor filters. This application is of particular interest in automatic driving systems, Visual Search applications and Internet-of-Things. Gabor filters have a particular importance in these fields, due to their tolerance to noise in the reference image and their robustness to scale changes and rotations of the image. The proposed Application Specific Image Processor is well-fit for Area-Delay-Power constrained applications, due to the exploitation of mathematical properties of the Gabor filters, used to obtain hardware simplifications, and to a careful project of the design. The architecture has been targeted both to a Xilinx Virtex 7 FPGA board and to TSMC CMOS 90nm std_cells. We obtain a maximum frequency of 172 MHz which allows to process 83 Full-HD (1920x1080 pixels) frame-per-second (fps) in the former case, while in the latter case the maximum frequency is 350 MHz allowing to process 168 Full- HD fps, improving the state-of-the-art both in terms of area consumption and maximum operating frequency. More work is being developed on this design in order to obtain better detection performances, while using higher number of orientations or targeting the design to more constrained devices, without loss in accuracy of the results.
The last year will be dedicated to further developments of the ASIP implementing the Gabor filter design and to the possible use and improvement of neural networks for pattern recognition and edge detection in multimedia processing.

Finally, the last year has been spent in Cornaredo, at STMicroelectronics, working on a project for the development of dedicated HW for neural networks applications. In particular, the candidate dedicated this time to the development of an HW implementation of a decompression scheme for Vector Quantization, in order to achieve lower memory occupation for the weights and a better organization of the operations between the memory and arithmetic units. The proposed HW accelerator is well-fit for Area-Delay-Power constrained applications, thanks to the exploitation of the peculiar properties of the Vector Quantization techniques.